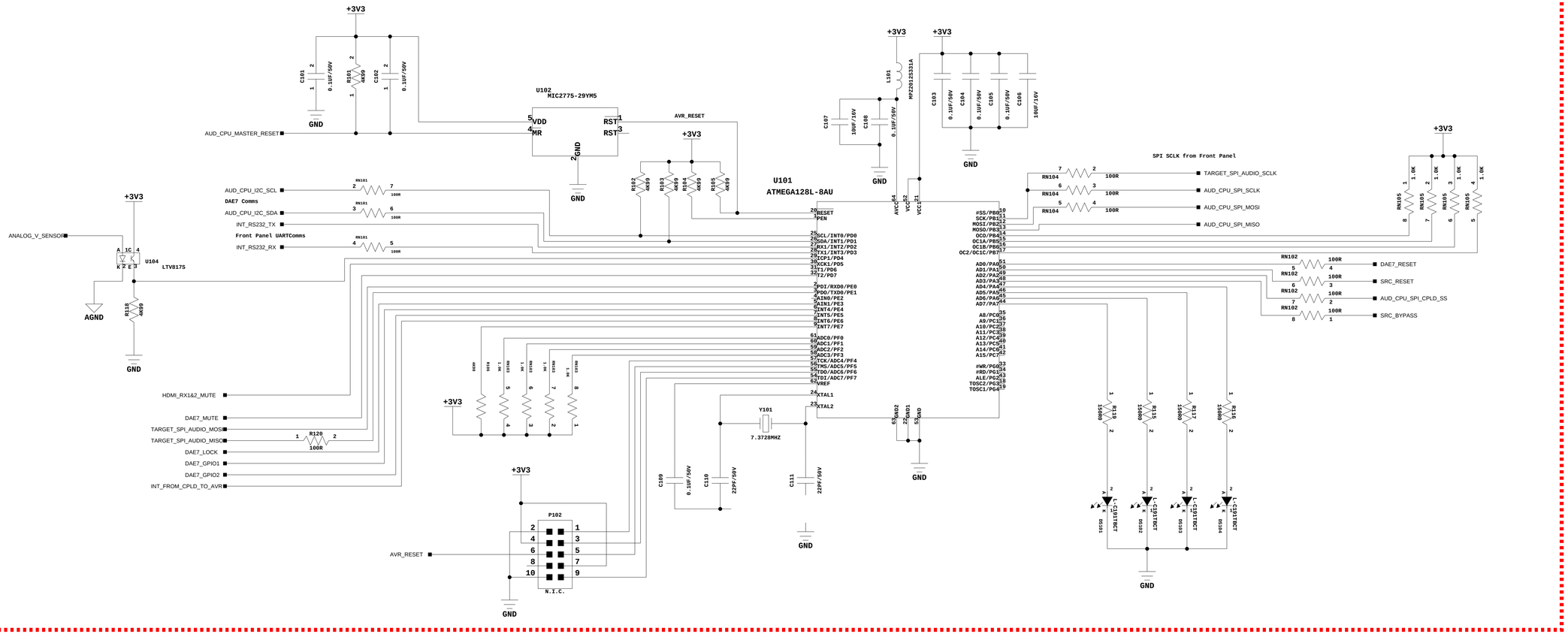
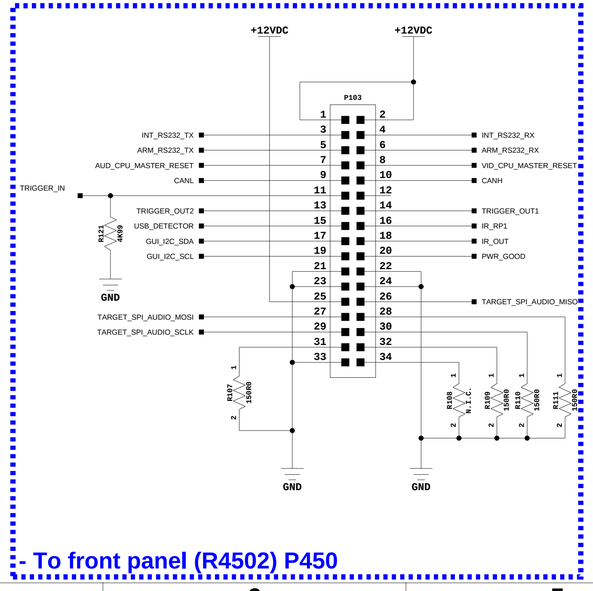
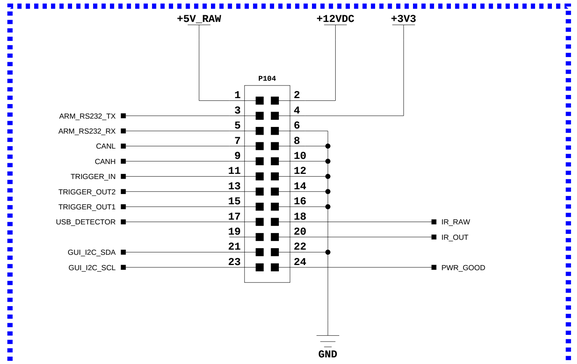
1. ATmega128 ucontroller for DAE / SRC / UART comms



1. +12VDC supply to front panel
2. +12VDC supply to front panel
3. TX from ARM to AVR for Communication
4. RX to ARM from AVR for Communication
5. ARM RS232 TX to RS232 and USB connectors.
6. ARM RS232 RX from RS232 and USB connectors.
7. Reset for AVR from ARM (ESA RST1)
8. USB_DETECTOR (Was ESA RST2)
9. CANL
10. CANH
11. Trigger_IN(notused)
12. NC
13. Trigger_OUT2
14. Trigger_OUT1
15. IR_RP2
16. IR_RP1
17. GUI_I2C_SDA (to Ac control board)
18. IR_OUT
19. GUI_I2C_SCL (to Ac control board)
20. PWRGOOD
21. GND
22. GND
23. GND
24. GND
25. +12VDC supply to front panel
26. TARGET_SPI_AUDIO_MISO
27. TARGET_SPI_AUDIO_MOSI
28. TARGET_SPI_AUDIO_SS
29. TARGET_SPI_AUDIO_SCLK
30. NC
31. NC
32. NC
33. GND
34. NC



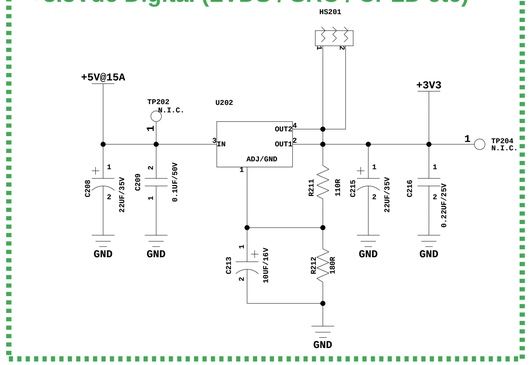
- To front panel (R4502) P450



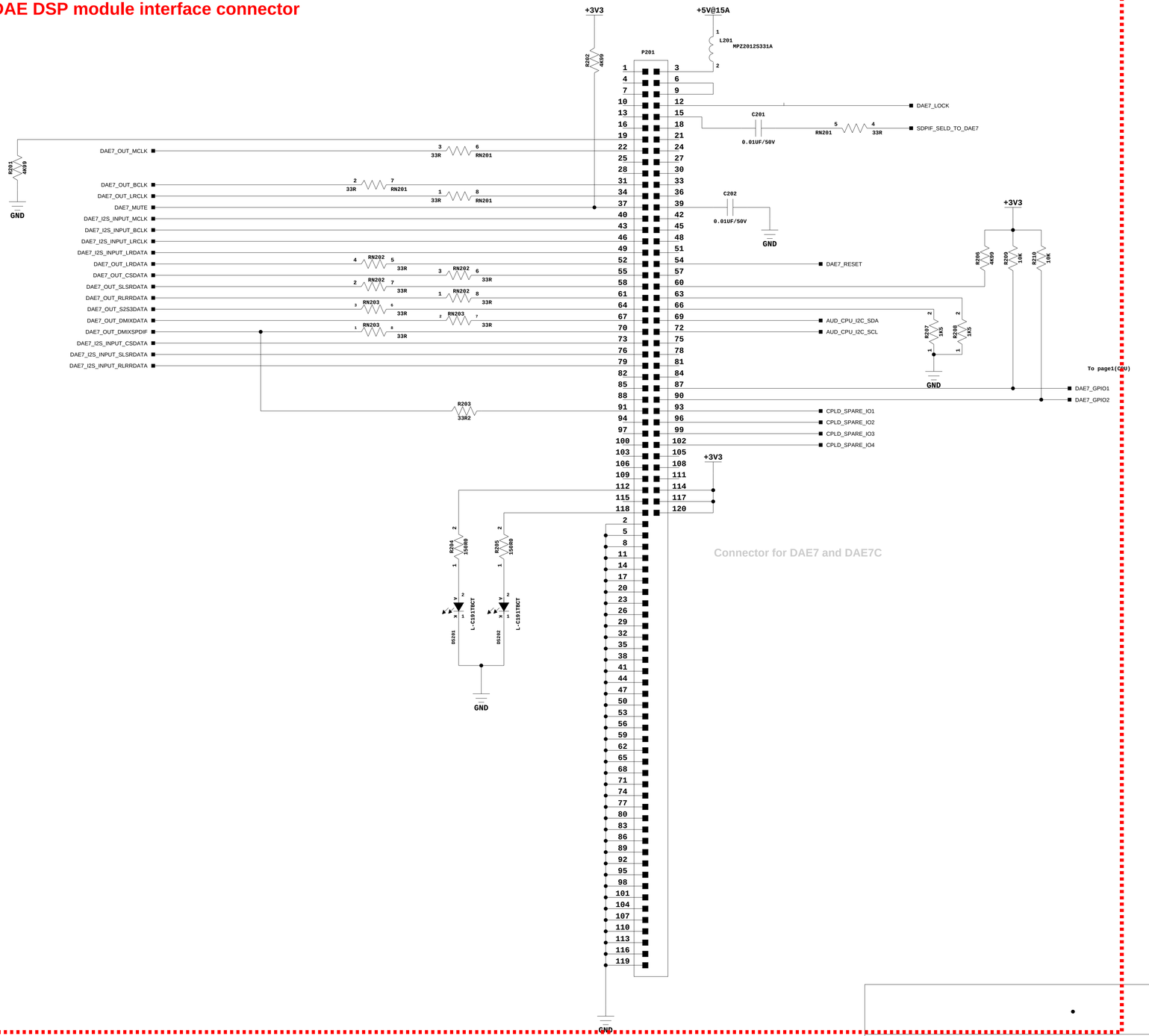
- To communication board (R6705) P106

TITLE: R6703-04-00S		
SIZE: D	DWG NO	REV: A
DRAWN BY: R.K.	SCALE	SHEET 1 of 17 — 6-19-2009_10:37

+3.3Vdc Digital (LVDS / SRC / CPLD etc)



2. DAE DSP module interface connector



NOTES:

RN201 - 1 element unused
RN202 - 1 element unused

DAE7 PIN ASSIGNEMENT

1.NC	2.GNDD	2.5VA
4.NC	5.GNDD	6.3.3VA
7.NC	8.GNDD	9.3.3VA_spdif
10.NC	11.GNDD	12.LOCK
13.CLKOUT	14.GNDD	15.SPDIF0_RXP0
16.KEY1	17.GNDD	18.SPDIF0_RXP1
19.AHCLK1>0	20.GNDD	21.SPDIF0_RXP2
22.MCLK_T1/R1	23.GNDD	24.SPDIF0_RXP3
25.SCLK_R1	26.GNDD	27.SPDIF0_RXP4
28.FCLK_R1	29.GNDD	30.SPDIF0_RXP5
31.SCLK_T1	32.GNDD	33.SPDIF0_RXP6
34.FCLK_T1	35.GNDD	36.SPDIF0_RXP7
37.MUTE	38.GNDD	39.SPDIF0_RXN
40.ALT0_MCLK	41.GNDD	42.SPDIF_TX0
43.ALT0_SCLK	44.GNDD	45.1.2VD
46.ALT0_FCLK	47.GNDD	48.1.2VD
49.ALT0_DATA	50.GNDD	51.1.2VD
52.AXR0[1]/AXR1[14]	53.GNDD	54.HOST_RST
55.AXR0[2]/AXR1[13]	56.GNDD	57.SELF_RST
58.AXR0[3]/AXR1[12]	59.GNDD	60.PWR_RST
61.AXR0[4]/AXR1[11]	62.GNDD	63.I2C_ADDR0
64.AXR0[5]/AXR1[10]	65.GNDD	66.I2C_ADDR1
67.AXR0[6]/AXR1[9]	68.GNDD	69.I2C1_SDA
70.AXR0[7]/AXR1[8]	71.GNDD	72.I2C1_SCL
73.AXR0[8]/AXR1[7]	74.GNDD	75.FSX1
76.AXR0[9]/AXR1[6]	77.GNDD	78.I2C0_SDA
79.AXR0[10]/AXR1[5]	80.GNDD	81.I2C0_SCL
82.AXR0[11]/AXR1[4]	83.GNDD	84.KEY
85.AXR0[12]/AXR1[3]	86.GNDD	87.I2C_ADDR0/GPO[1] NIC line
88.AXR0[13]/AXR1[2]	89.GNDD	90.I2C_ADDR1/GPO[2] NIC Line
91.AXR0[14]/AXR1[1]	92.GNDD	93.DAE_SCK_GPO[9]
94.AXR0[15]/AXR1[0]	95.GNDD	96.DAE_MOSI_GPO[10]
97.AHCLKX0	98.GNDD	99.DAE_MISO_GPO[11]
100.ACLKX0	101.GNDD	102.DAE_SS0_GPO[12]
103.AFSX0	104.GNDD	105.DAE_SS1_GPO[13]
106.AMUTEIN0	107.GNDD	108.DAE_SS2_GPO[14]
109.AMUTE0	110.GNDD	111.DAE_SS3_GPO[15]
112.AHCLK0	113.GNDD	114.3.3VD
115.ACLK0	116.GNDD	117.3.3VD
118.AFSR0	119.GNDD	120.3.3VD

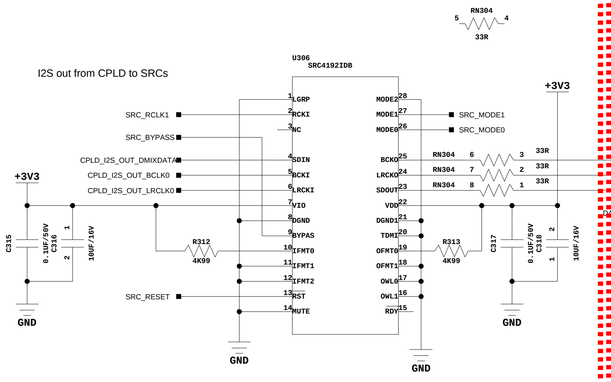
TITLE

R6703-04-00S

SIZE	DWG NO	REV
D		A

DRAWN BY: R.K. | SCALE | SHEET 2 of 17 | 6-19-2009_10:37

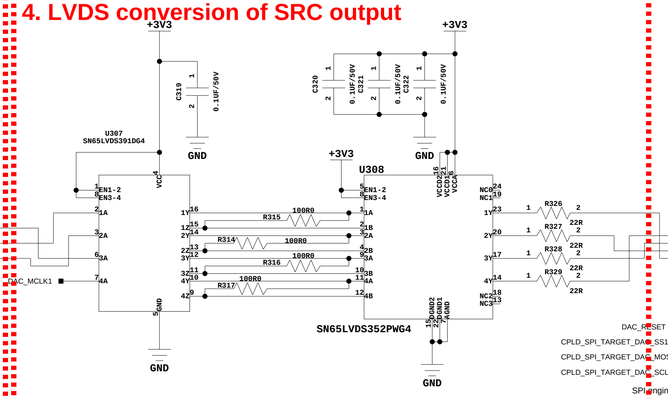
3. SRC circuit (Sample Rate Converter)



SRC4192 config

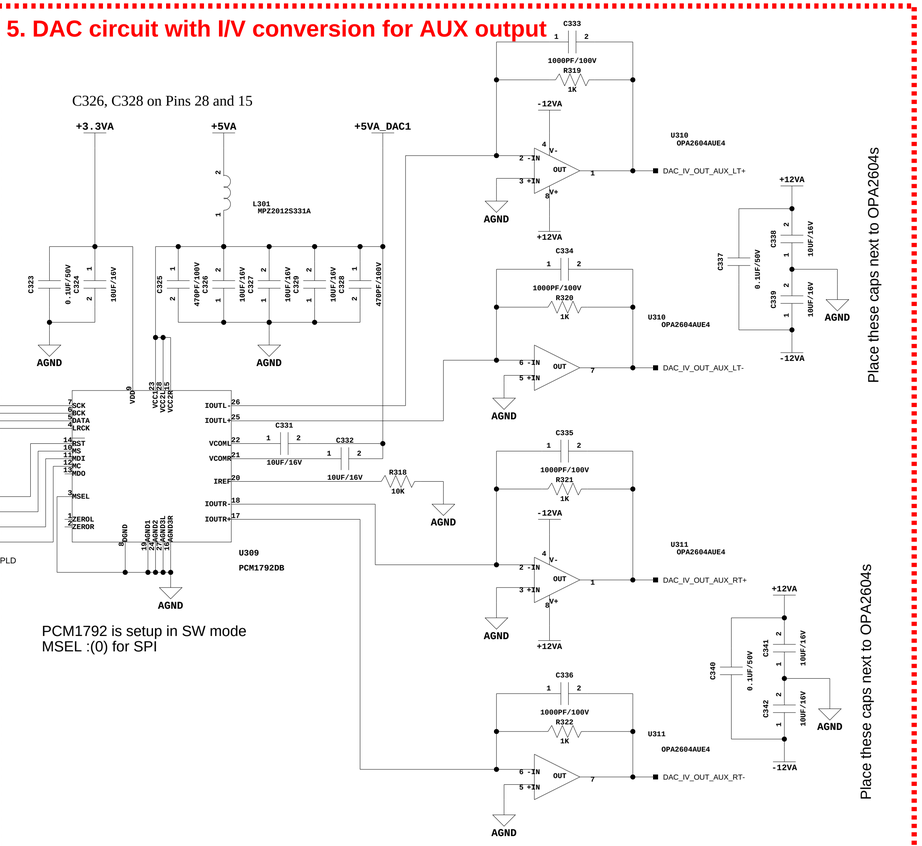
1. MODE(2:0): 0, variable : In Slave and out Master (variable)
2. IFMT(2:0) : 0, 0, 1: input format 24-bit I2S
3. OFMT(1:0) :0,1 : Output format I2S
4. OWL(1:0) 0,0: Output word length 24-bit
5. Bypas: SW control.
6: Mute: 0: OFF

4. LVDS conversion of SRC output



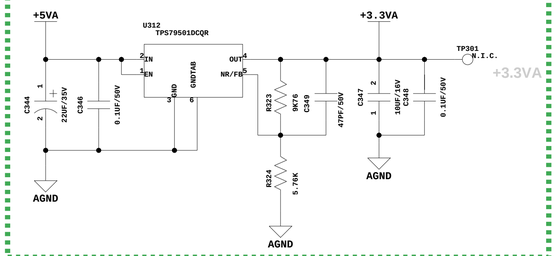
LVDS pairs
Place R315-R317 close to U308
These are matching length trace 5mm max
Impedant control 100 Ohm trace to trace (pair)

5. DAC circuit with I/V conversion for AUX output

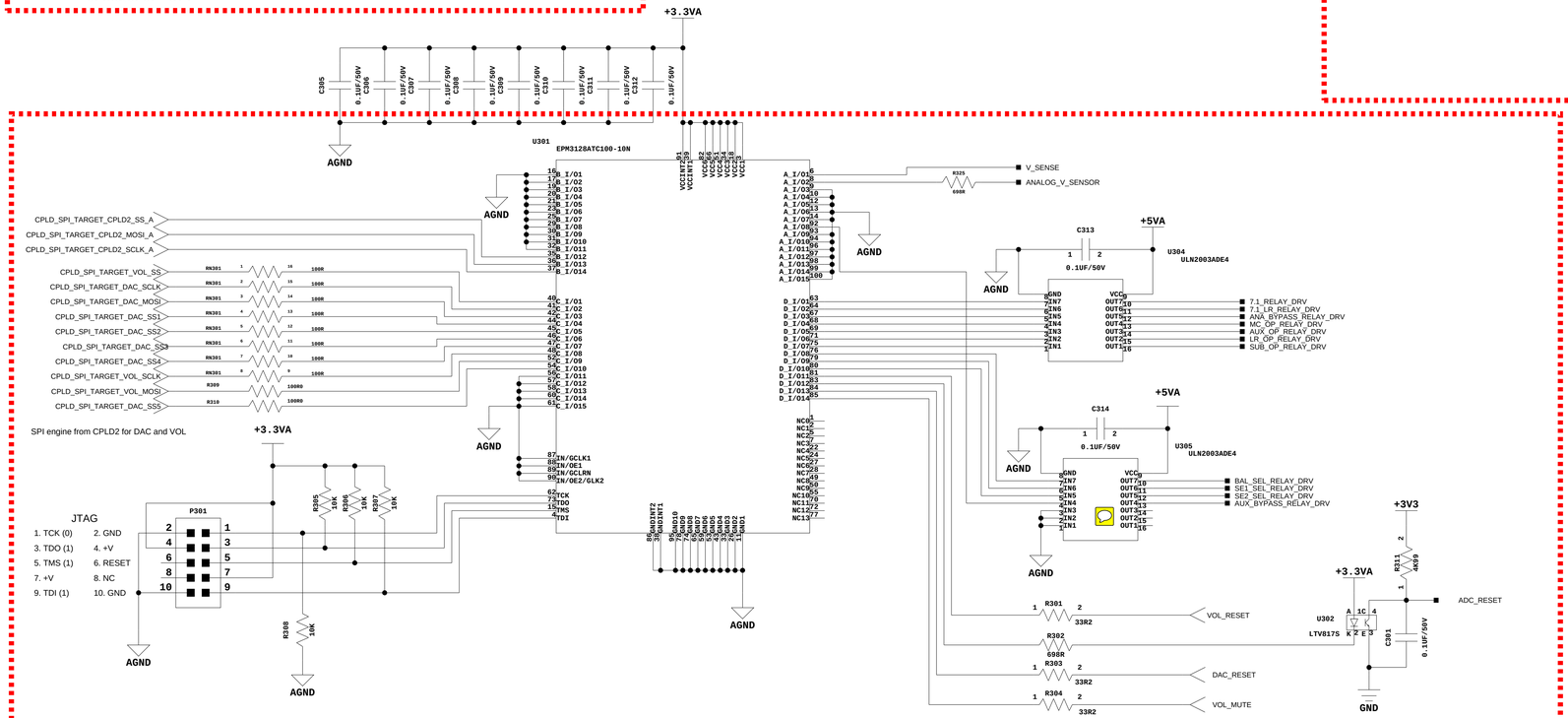


PCM1792 is setup in SW mode
MSEL :(0) for SPI

+3.3Vdc Analog (DACs / CPLD / Volume chip)

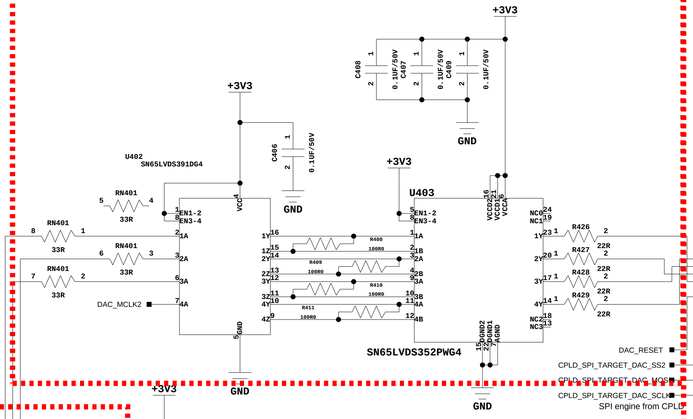


6. CPLD circuit used as a SPI engine for DACs and Volume chips and signal relay driver circuits

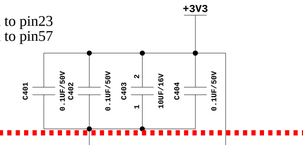


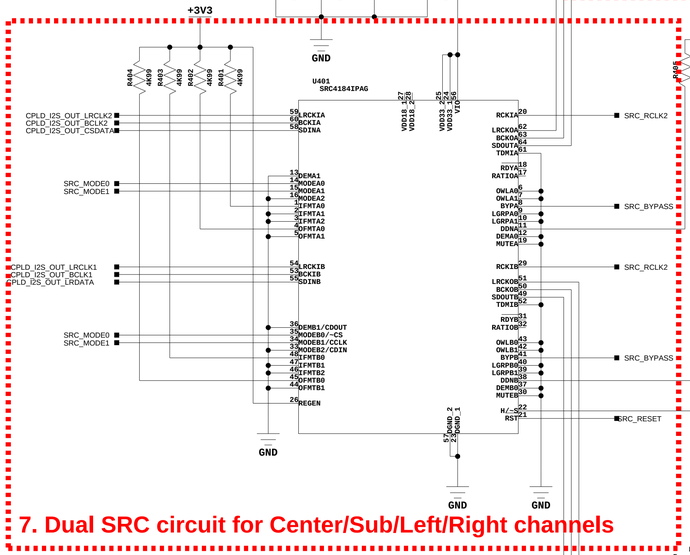
TITLE	R6703-04-00S		
SIZE D	DWG NO		REV A
DRAWN BY: R.K.	SCALE	SHEET 3 of 17	6-19-2009_10:37

8. LVDS conversion of SRC output (center/sub)



Connected to pin23
Connected to pin57



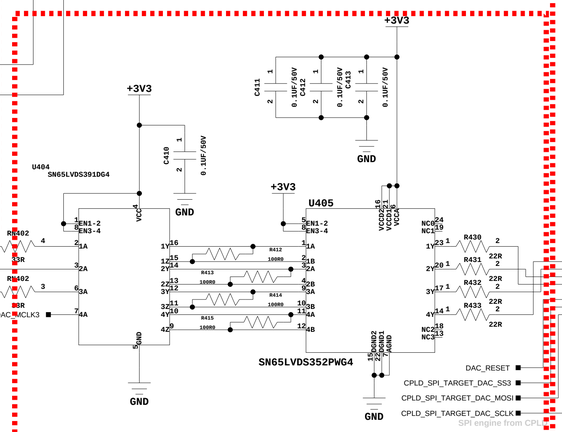


I2S out from CPLD to SRCs

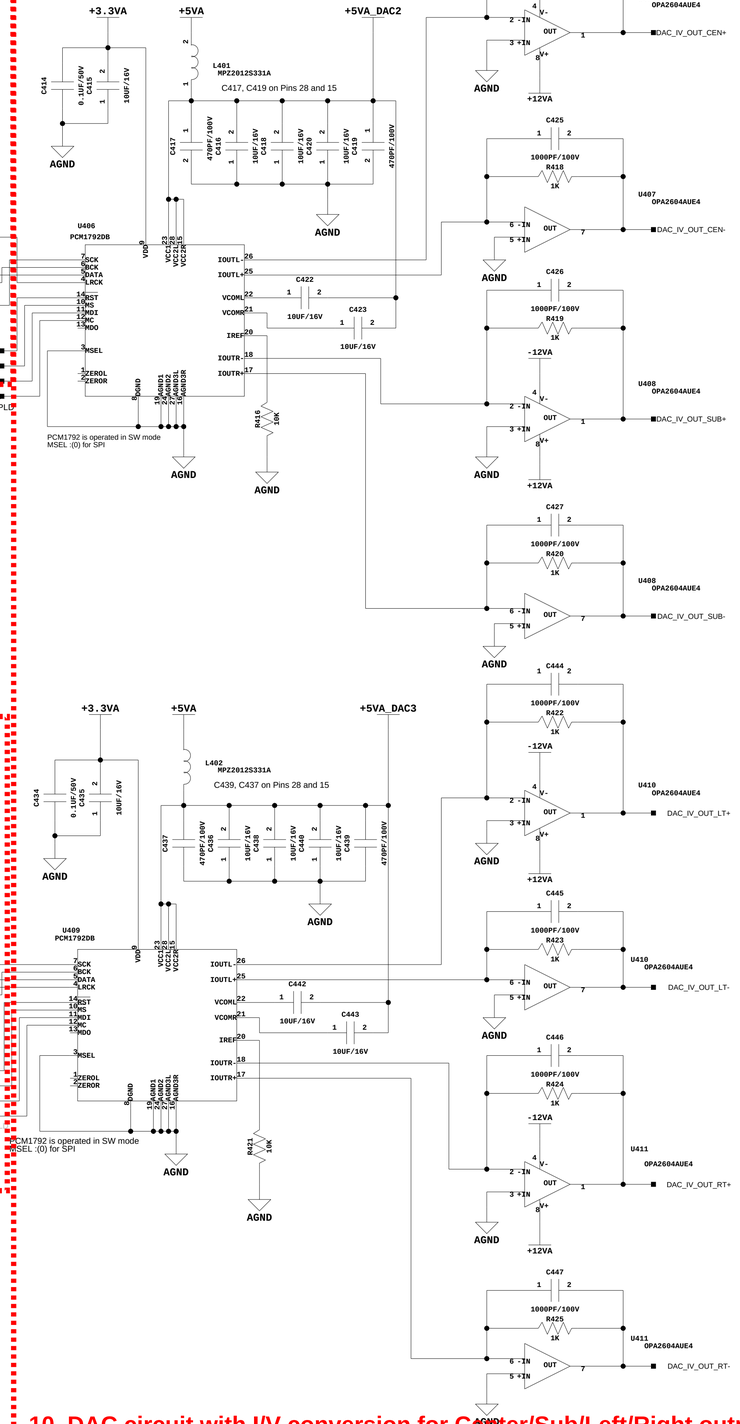
7. Dual SRC circuit for Center/Sub/Left/Right channels

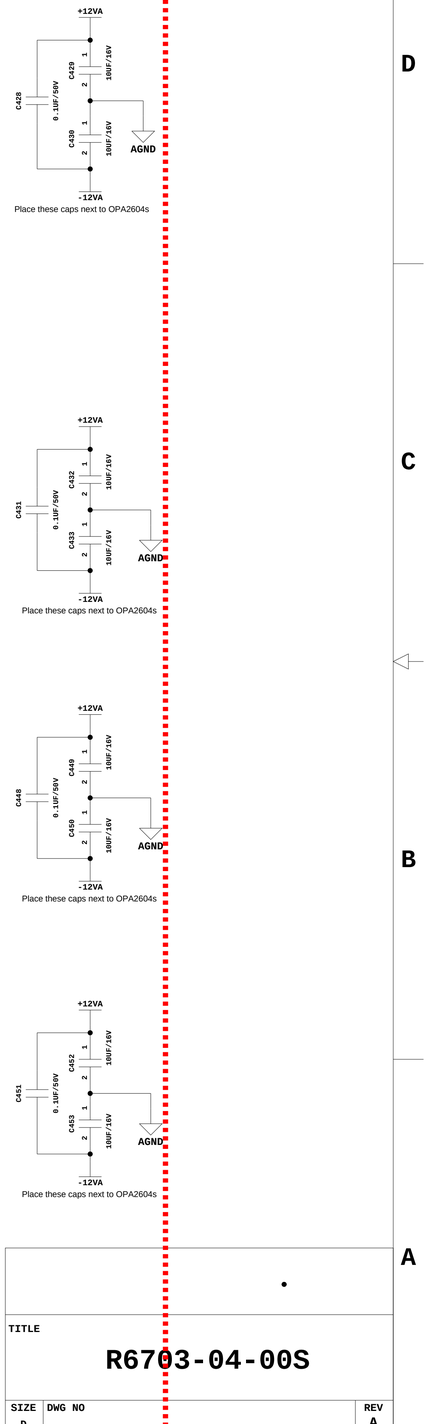
1. SRC4184 Hardware MODE
   1. MODE(2:0): 0, variable : In Slave and out Master (variable)
   2. IFMT(2:0) : 0, 0, 1: input format 24-bit I2S
   3. OFMT(1:0) :0,1 : Output format I2S
   4. OWL(1:0) 0,0: Output word length 24-bit
   5. LGRPX(1:0) : 0,0: 64 samples delay
   6. DDN: 1 : Direct Downsampler Enable
   7. DEMP(1:0) : 0, 0 : Disable
   8. Bypas: 0 : SW control mode
   9. MUTE: 0 : OFF
2. DO NOT CONNECT Pins 27 and 28

9. LVDS conversion of SRC output (Left/Right)



10. DAC circuit with I/V conversion for Center/Sub/Left/Right output





TITLE	R6703-04-00S	
SIZE D	DWG NO	REV A
SCALE	SHEET 4 of 17	6-19-2009_10:37

DRAWN BY: R.K.

11. LVDS conversion of SPI interface

SPI engine from CPLD to CPLD2 before LVDS

U502 SN65LVDS391DG4

U504 SN65LVDS352PWG4

- CPLD_SPI_TARGET_CPLD2_SS
- CPLD_SPI_TARGET_CPLD2_MOSI
- CPLD_SPI_TARGET_CPLD2_SCLK
- SRC_REAR_DATA

→ CPLD_SPI_TARGET_CPLD2_SS_A, CPLD_SPI_TARGET_CPLD2_MOSI_A, CPLD_SPI_TARGET_CPLD2_SCLK_A

13. LVDS conversion of SRC outputs (Surr/Rear)

U503 SN65LVDS391DG4

U505 SN65LVDS352PWG4

DAC_MCLK4

1. SRC4184 Hardware MODE
   1. MODEA(2:0): 0,0,0: In and out are Slave mode
   1. MODEB(2:0): 0, variable : In Slave and out Master (variable)
   2. IFMT(2:0) : 0, 0, 1: input format 24-bit I2S
   3. OFMT(1:0) :0,1 : Output format I2S
   4. OWL(1:0) 0,0: Output word length 24-bit
   5. LGRPX(1:0) : 0,0: 64 samples delay
   6. DDN: 1 : Direct Downsampler Enable
   7. DEMP(1:0) : 0, 0 : Disable
   8. Bypas: 0 : SW control mode
   9. MUTE: 0 : OFF
2. DO NOT CONNECT Pins 27 and 28

Connected to pin23
Connected to pin57

U501 SRC4184IPAG

I2S out from CPLD to SRCs

- CPLD_I2S_OUT_LRCLK4
- CPLD_I2S_OUT_BCLK4
- CPLD_I2S_OUT_SURRDATA
- CPLD_I2S_OUT_LRCLK3
- CPLD_I2S_OUT_BCLK3
- CPLD_I2S_OUT_REARDATA
- SRC_MODE0
- SRC_MODE1

→ SRC_RCLK3, SRC_BYPASS, SRC_RCLK3, SRC_REAR_DATA (33R2 R531), SRC_BYPASS, SRC_RESET

12. Dual SRC circuit for Surrounds L/R and Rears L/R

U506 PCM1796DB

U507 PCM1796DB

- CPLD_SPI_TARGET_DAC_SS4
- CPLD_SPI_TARGET_DAC_SCLK
- CPLD_SPI_TARGET_DAC_MOSI
- DAC_RESET

→ CPLD_SPI_TARGET_DAC_SS5, CPLD_SPI_TARGET_DAC_SCLK, CPLD_SPI_TARGET_DAC_MOSI, DAC_RESET

+5VA_DAC4, +5VA_DAC5, +5VA, +3.3VA, AGND

U508 OPA2604AU → DAC_IV_OUT_SURRLT+

U508 OPA2604AU → DAC_IV_OUT_SURRLT-

U509 OPA2604AU → DAC_IV_OUT_SURRRT+

U509 OPA2604AU → DAC_IV_OUT_SURRRT-

U510 OPA2604AU → DAC_IV_OUT_REARLT+

U510 OPA2604AU → DAC_IV_OUT_REARLT-

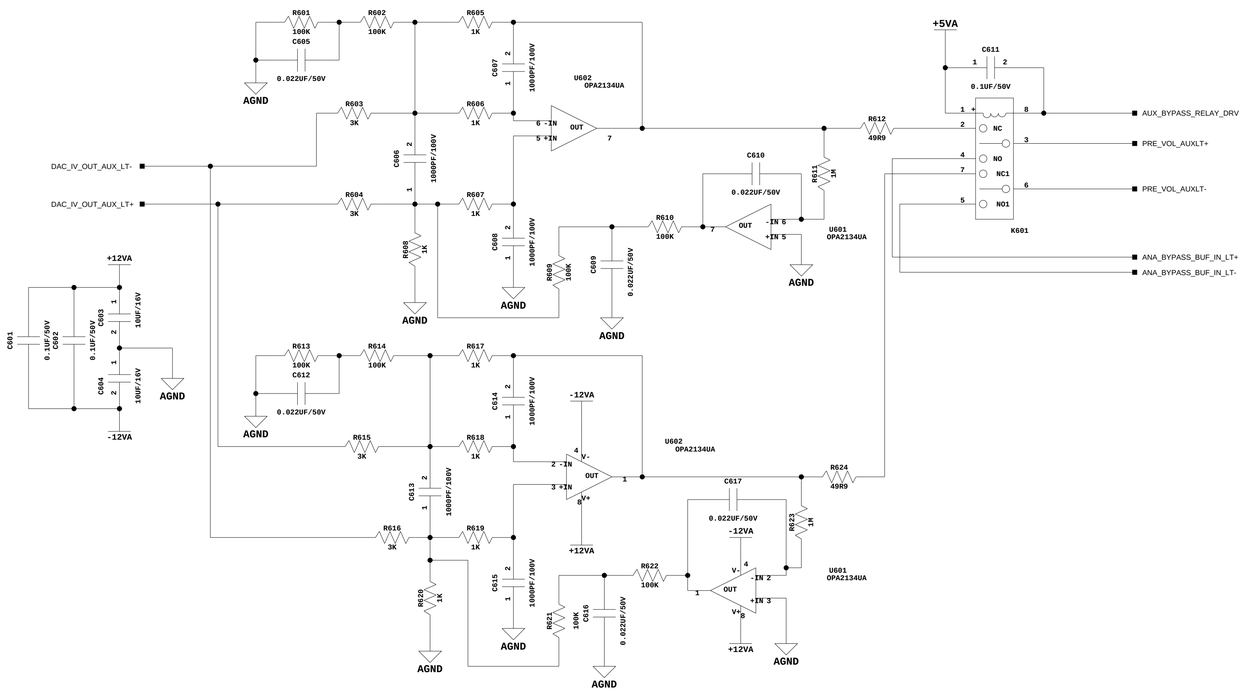
U511 OPA2604AU → DAC_IV_OUT_REARRT+

U511 OPA2604AU → DAC_IV_OUT_REARRT-

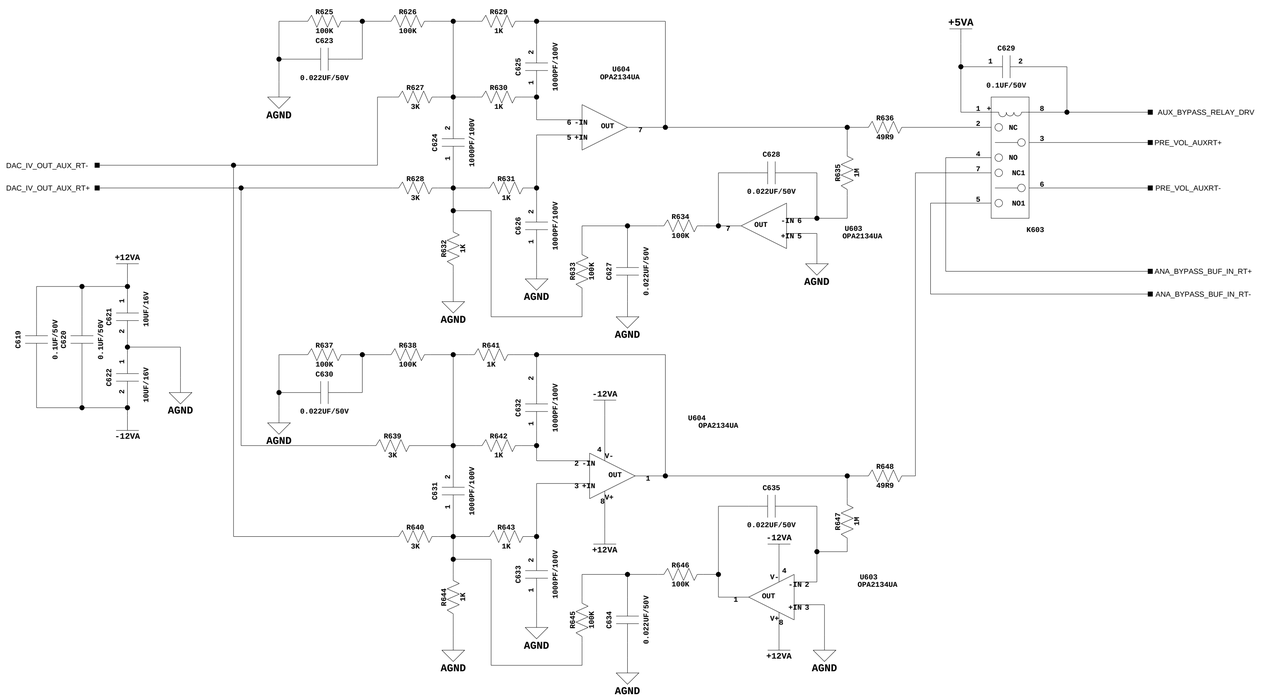
14. DAC circuit with I/V conversion for Surrounds/Rears output

TITLE	R6703-04-00S
SIZE	DWG NO / REV A
SCALE	SHEET 5 OF 17
DRAWN BY: RHK	6-19-2009_10:37

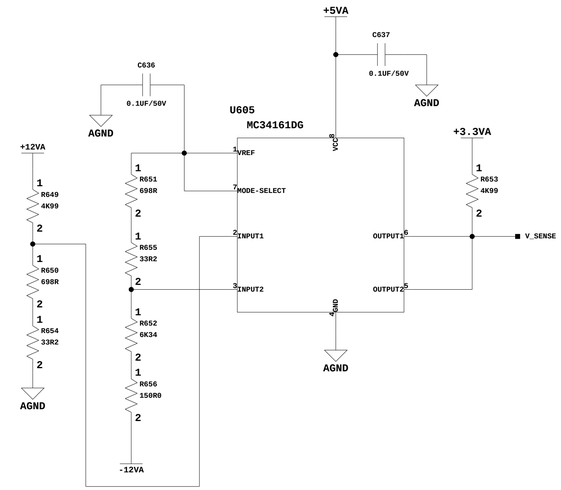
15. Audio buffers and DC Servo for Aux Left channels + 7.1 Bypass relays (Left output bi-amp)

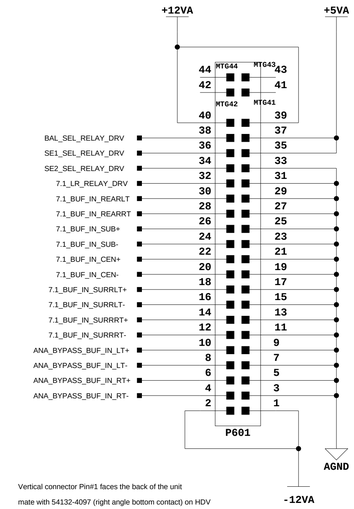


16. Audio buffers and DC Servo for Aux Right channels + 7.1 Bypass relays (Right output bi-amp)



17. Rail sensing circuit for power fail muting





Vertical connector Pin#1 faces the back of the unit
mate with 54132-4097 (right angle bottom contact) on HDV
Cable has to be same side of contact

-To I/O board (R6704) P301

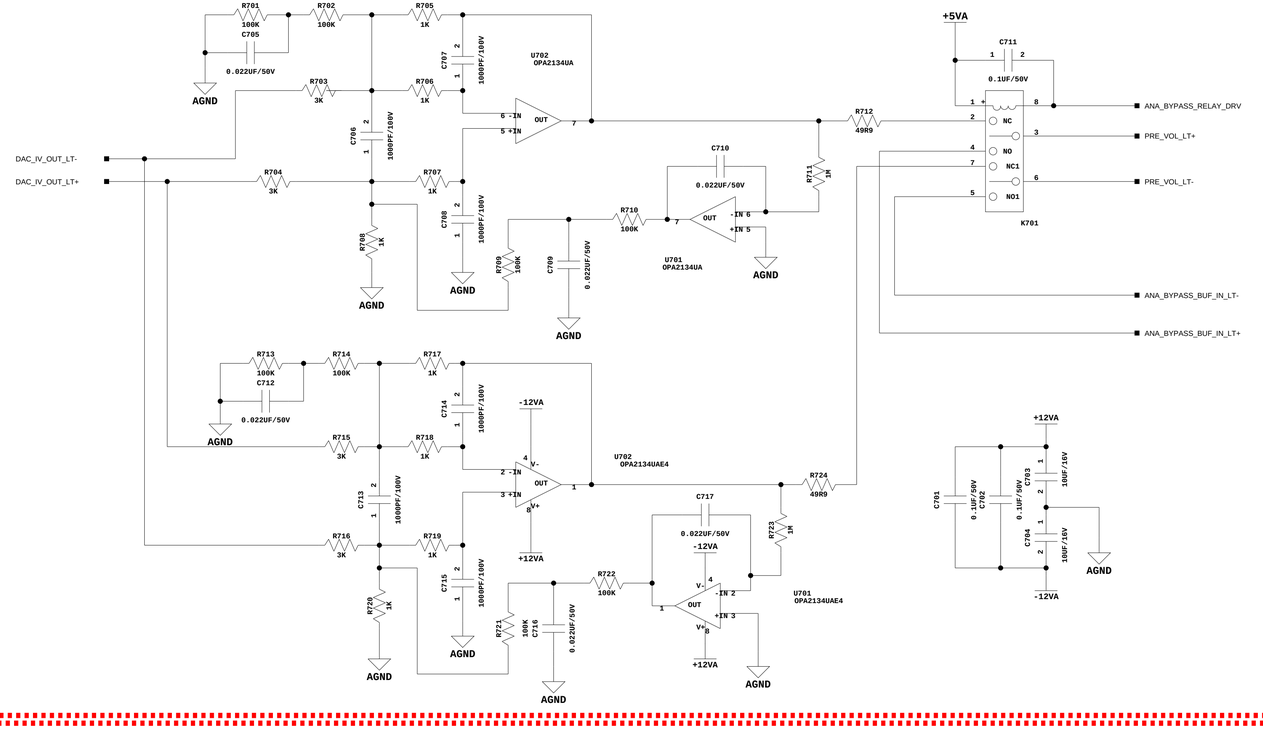
TITLE

R6703-04-00S

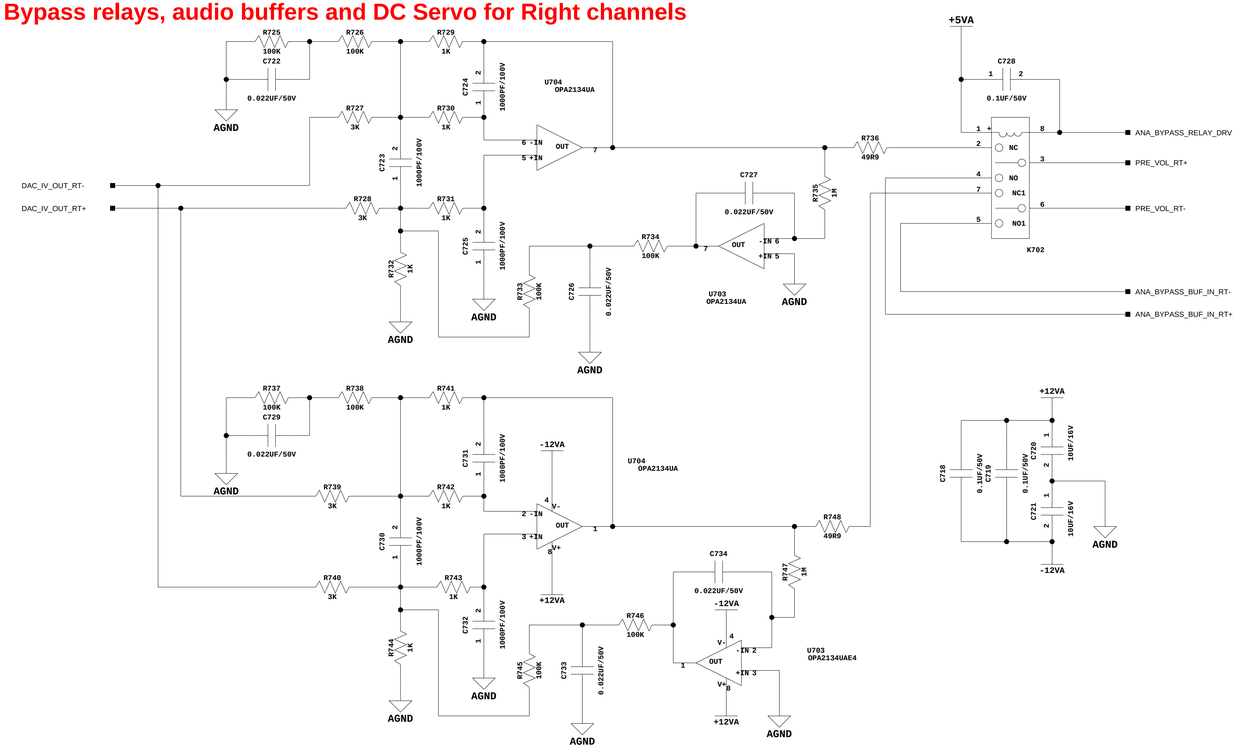
SIZE	DWG NO	REV
D		A

DRAWN BY: R.K. | SCALE | SHEET 6 of 17 | 6-19-2009_10:37

18. 7.1 Bypass relays, audio buffers and DC Servo for Left channels



19. 7.1 Bypass relays, audio buffers and DC Servo for Right channels



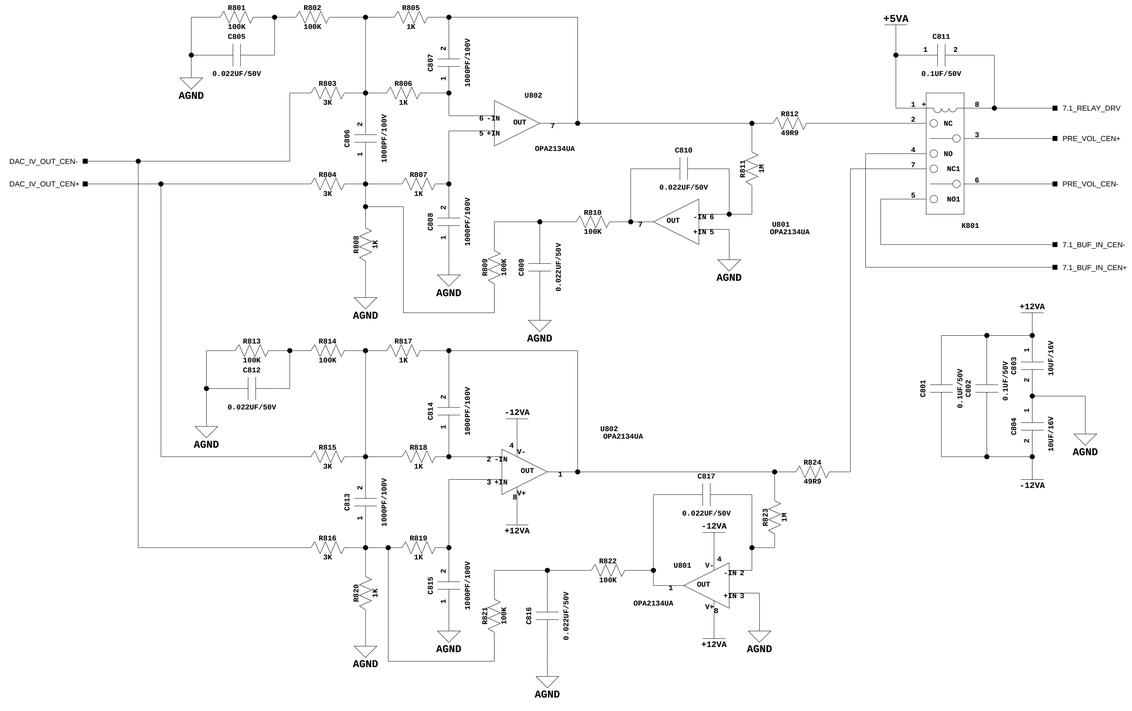
TITLE

R6703-04-00S

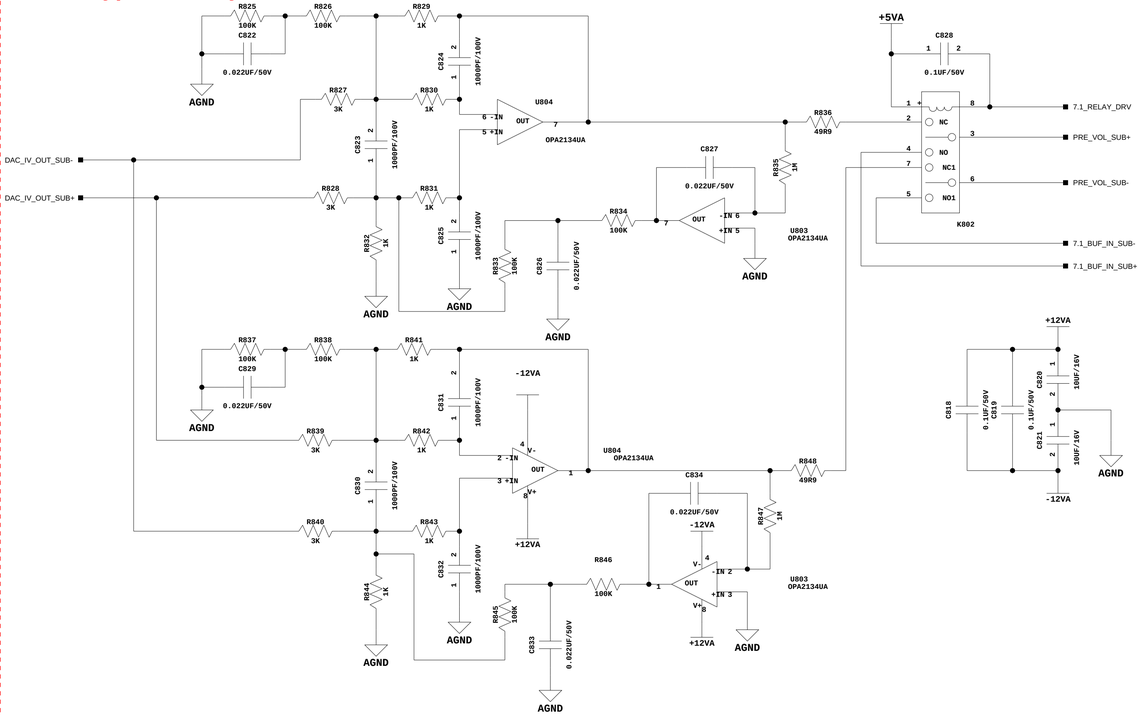
SIZE	DWG NO	REV
D		A

DRAWN BY: R.K. | SCALE | SHEET 7 of 17 | 6-19-2009_10:37

20. 7.1 Bypass realays, audio buffers and DC Servo for Center channels

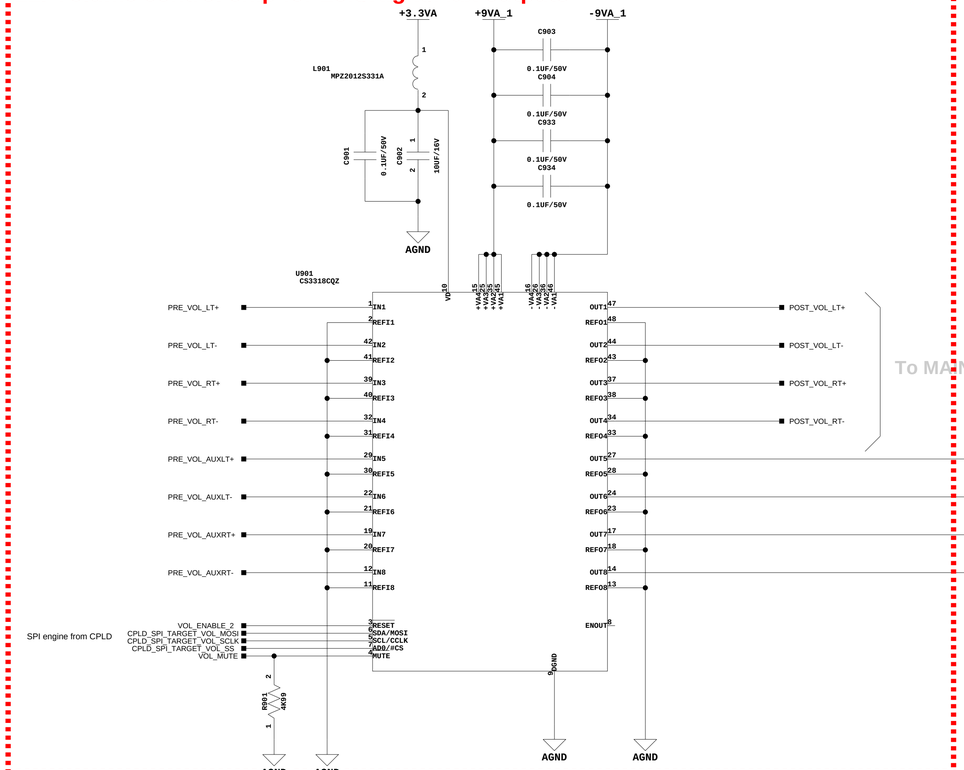


21. 7.1 Bypass realays, audio buffers and DC Servo for Sub channels

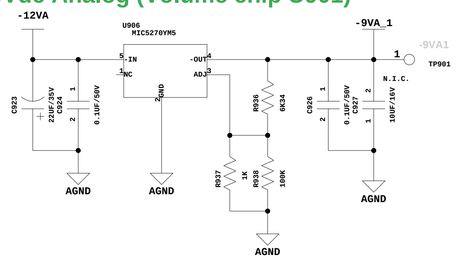


TITLE	R6703-04-00S	
SIZE D	DWG NO	REV A
DRAWN BY: R.K.	SCALE	SHEET 8 of 17 6-19-2009_10:37

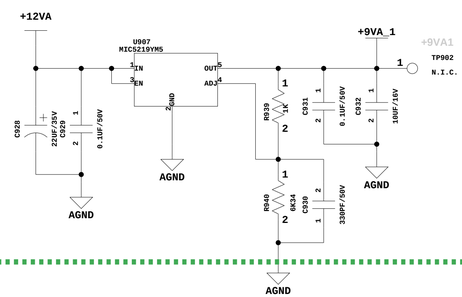
22. Volume control chip for Left/Right/Aux outputs



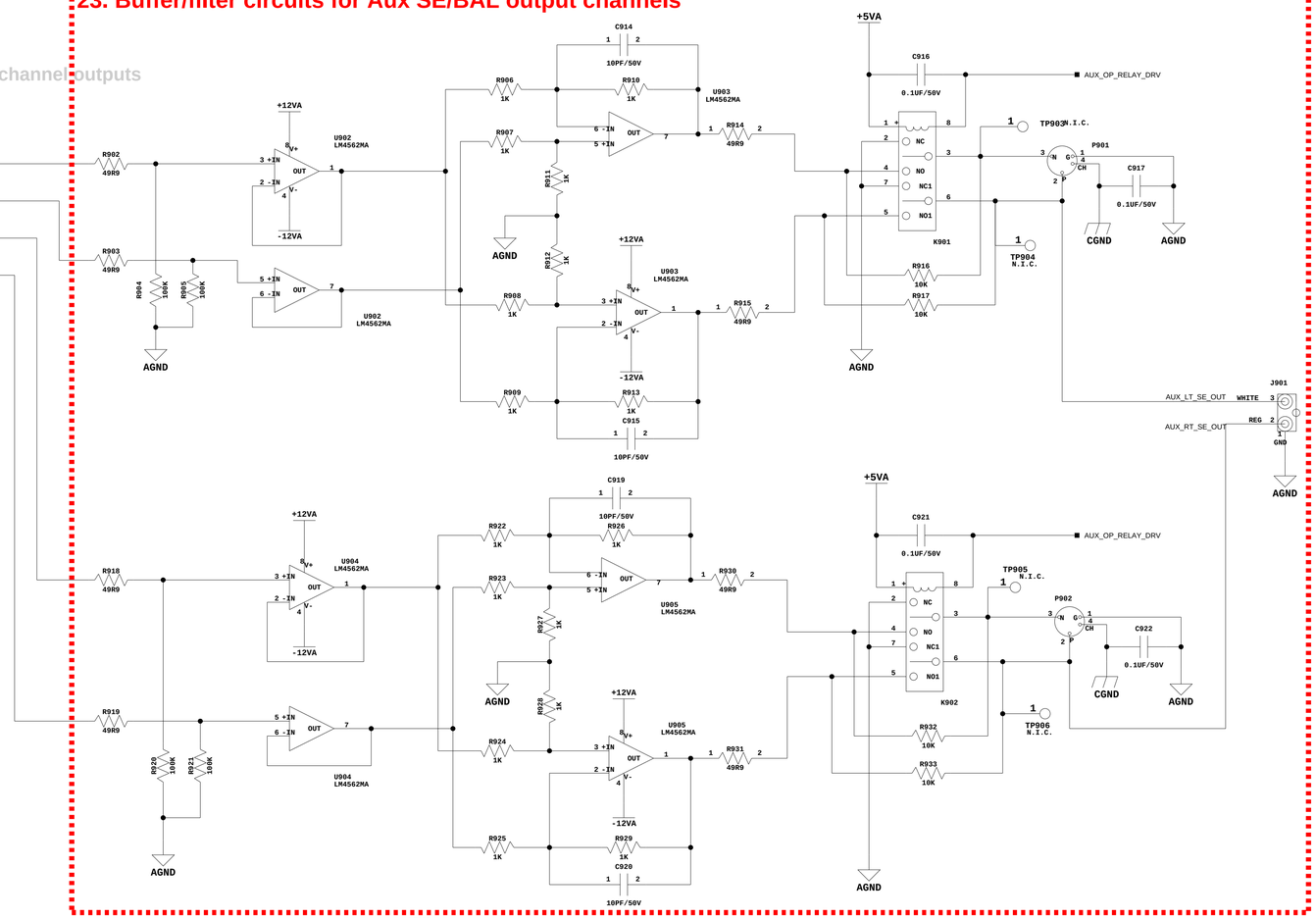
+9Vdc Analog (Volume chip U901)

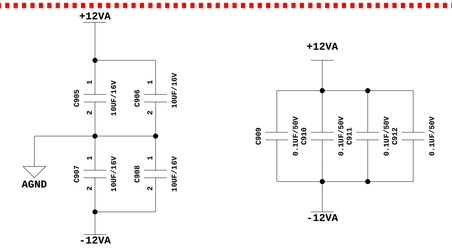


-9Vdc Analog (Volume chip U901)



23. Buffer/filter circuits for Aux SE/BAL output channels





TITLE

R6703-04-00S

SIZE	DWG NO	REV
D		A

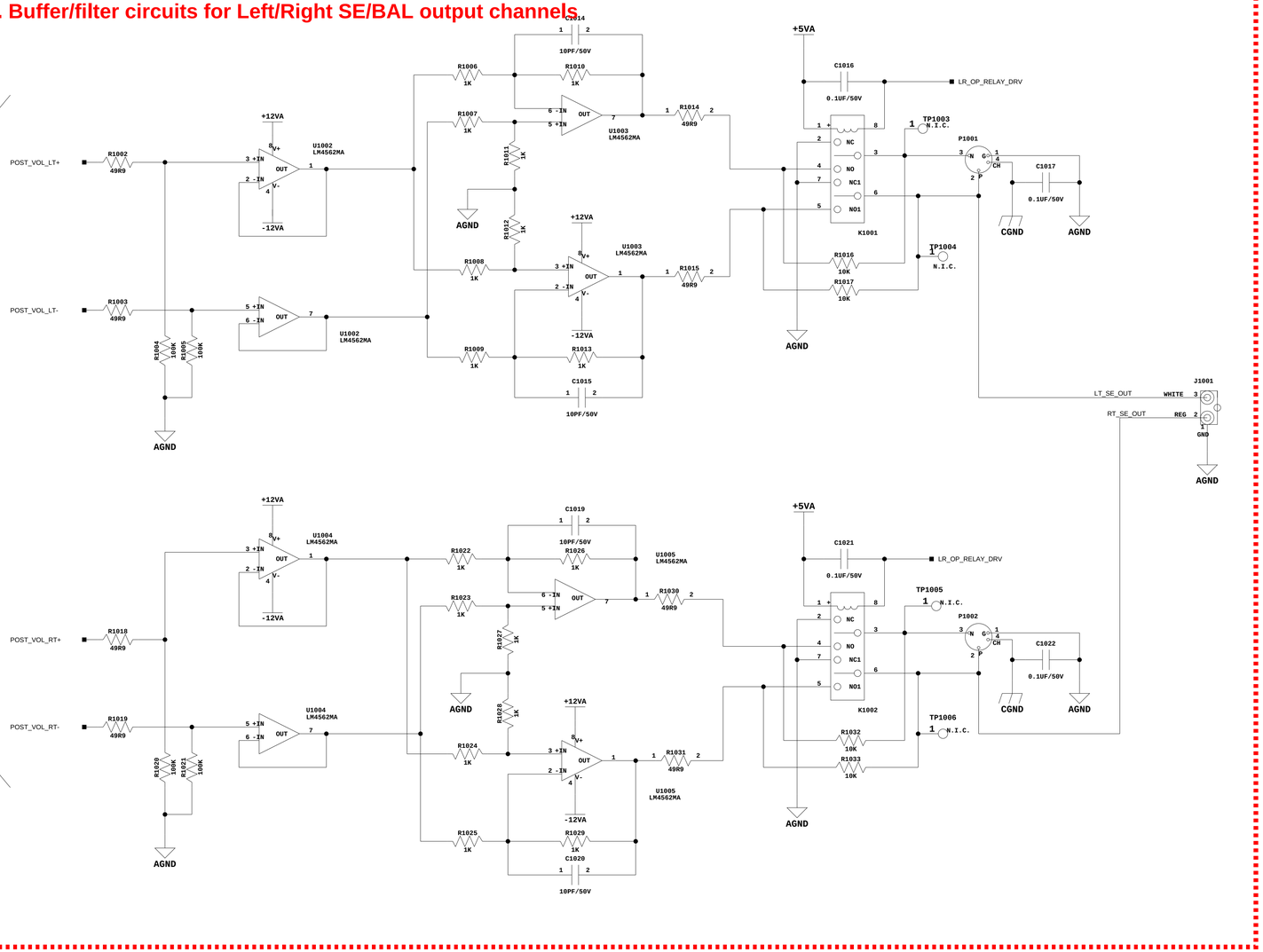
DRAWN BY: R.K.

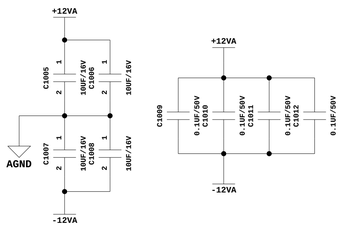
SCALE

SHEET 9 of 17

6-19-2009_10:37

24. Buffer/filter circuits for Left/Right SE/BAL output channels



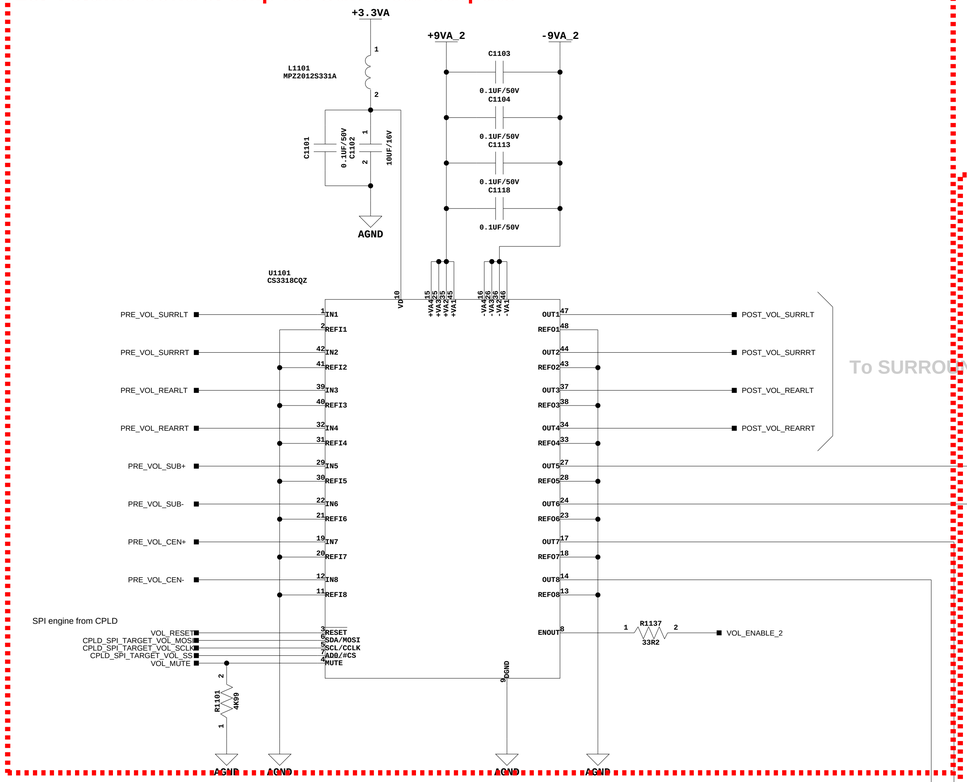


MAIN LT and RT channels from vol control Page 9

TITLE	R6703-04-00S	
SIZE D	DWG NO	REV A
DRAWN BY: R.K.	SCALE	SHEET 10 of 17

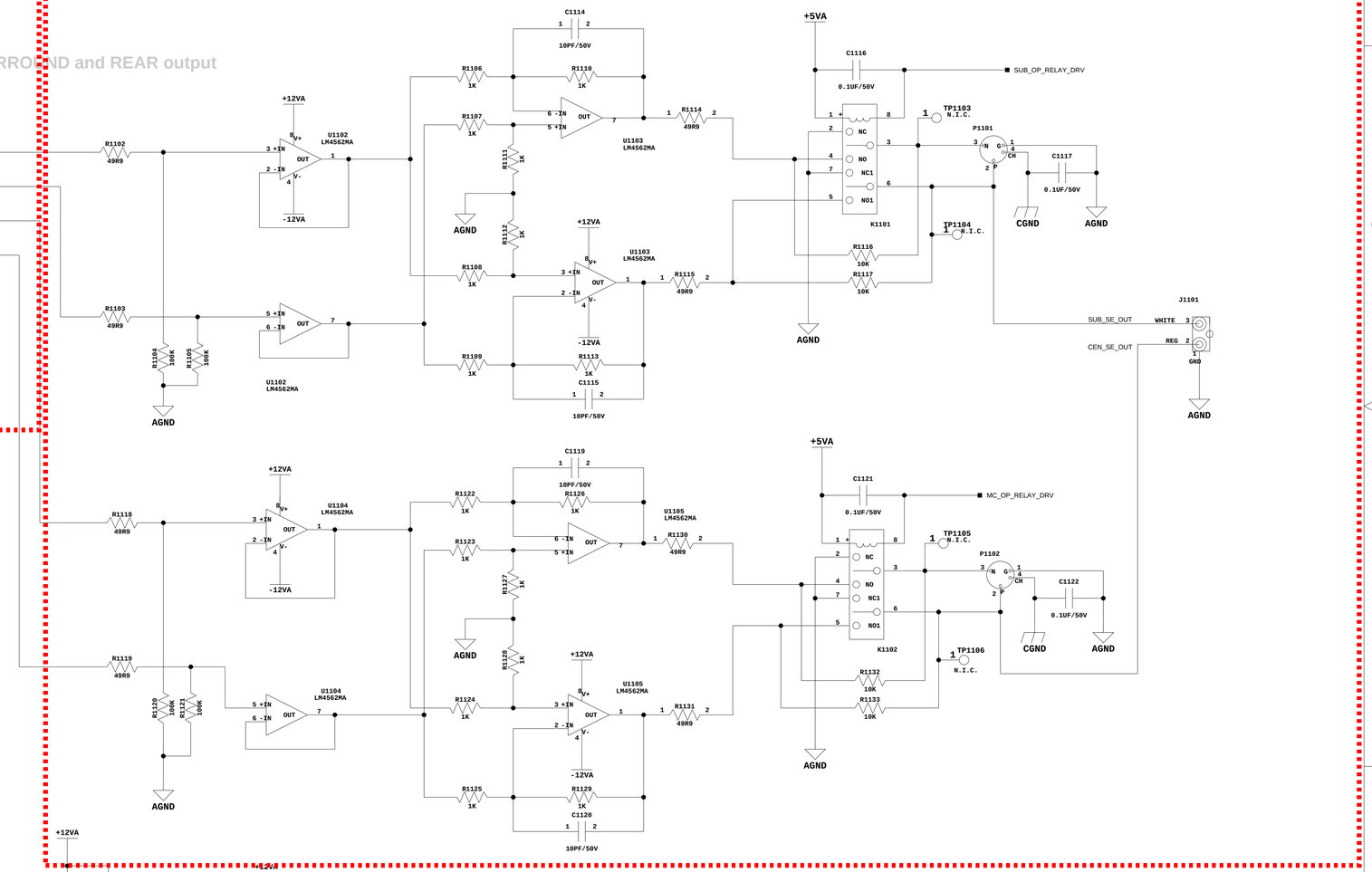
6-19-2009_10:37

25. Volume control chip for Surr/Rear outputs

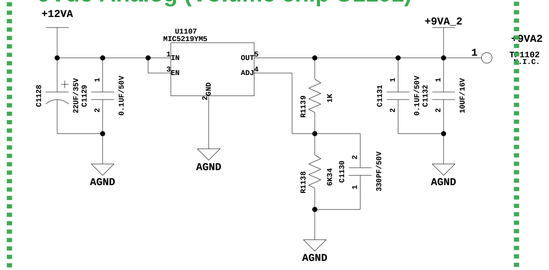


To SURROUND and REAR output

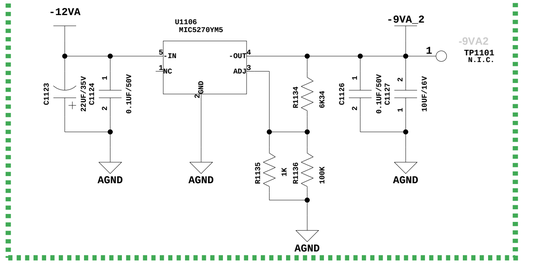
26. Buffer/filter circuits for Sub/Center SE/BAL output channels

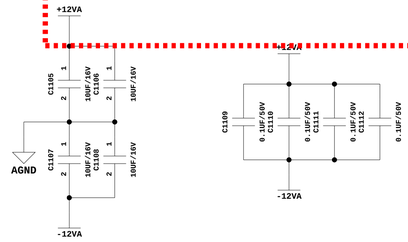


+9Vdc Analog (Volume chip U1101)



-9Vdc Analog (Volume chip U1101)

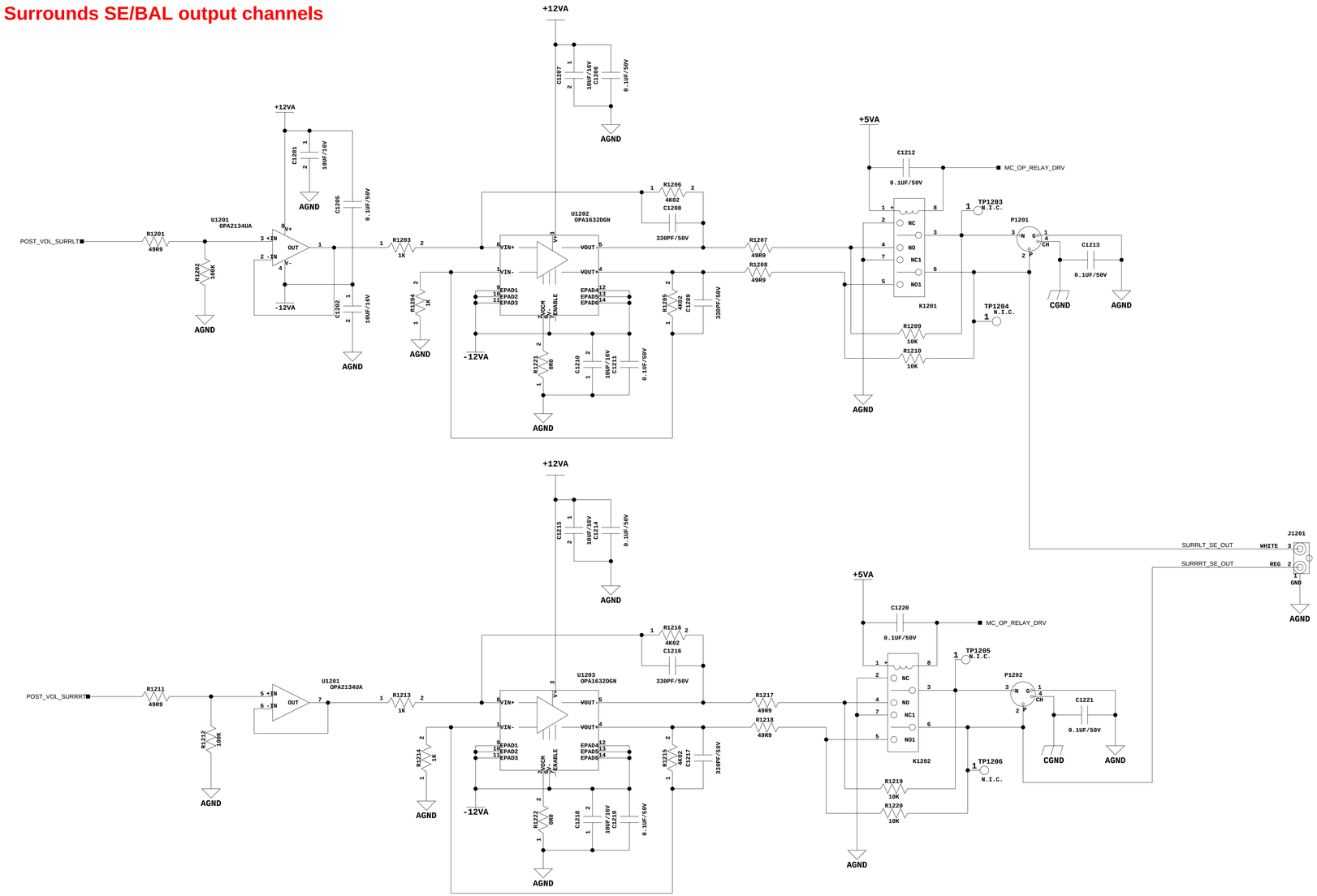




TITLE: R6703-04-00S		
SIZE: D	DWG NO	REV: A
DRAWN BY: R.K.	SCALE	SHEET 11 of 17

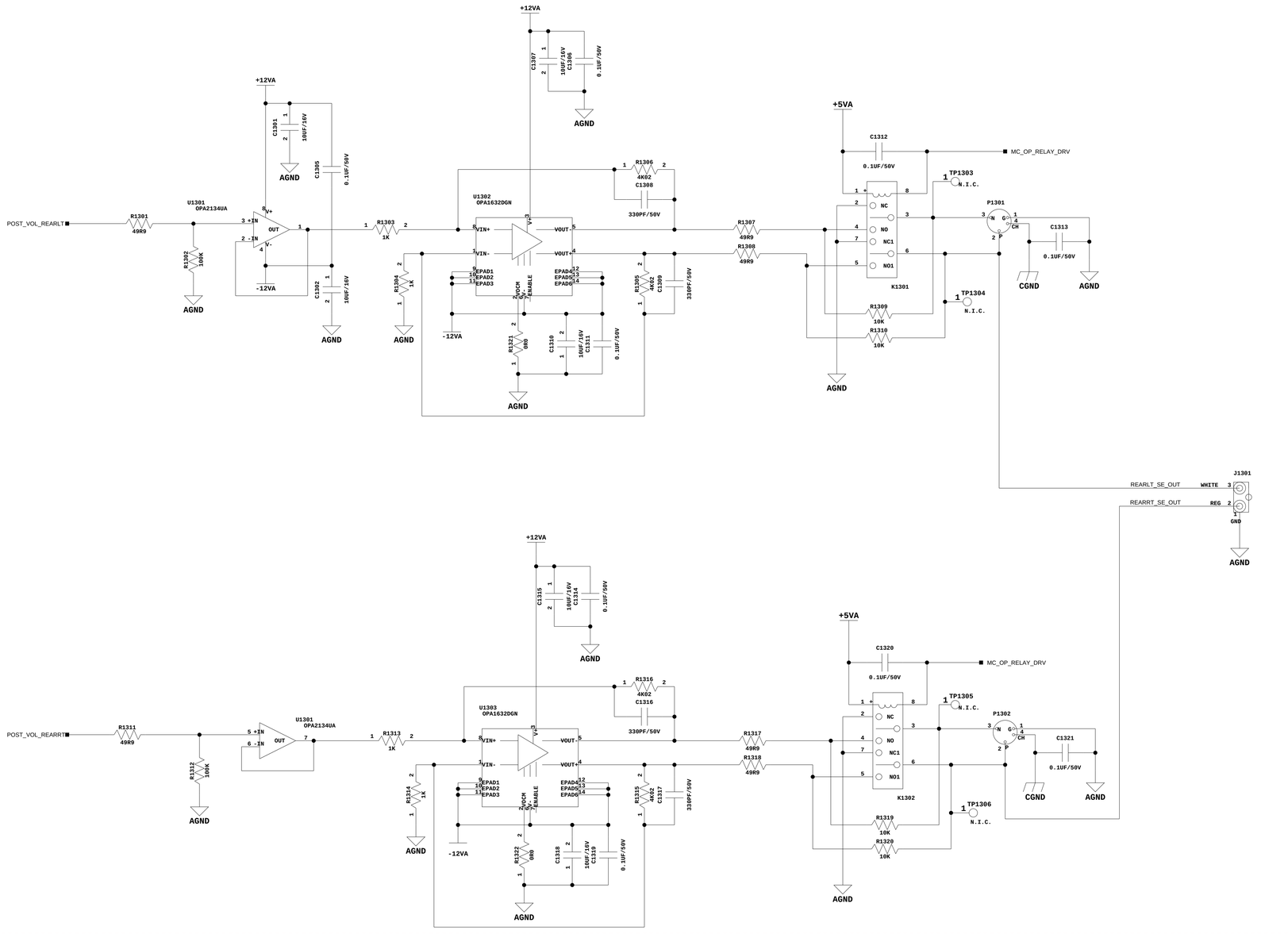
6-19-2009_10:37

27. Buffer/filter circuits for Surrounds SE/BAL output channels



TITLE	R6703-04-00S	
SIZE D	DWG NO	REV A
DRAWN BY: R.K.	SCALE	SHEET 12 of 17 — 6-19-2009_10:37

28. Buffer/filter circuits for Rears SE/BAL output channels



TITLE	R6703-04-00S	
SIZE D	DWG NO	REV A
DRAWN BY: R.K.	SCALE	SHEET 13 of 17 6-19-2009_10:37

AUD To HDMI_TX

HDMI_RX3&4_AUDIO

P1401

- From HDV Board J12

From ADC and digital inputs

P1406

- From I/O board (R6704) P101

U1401

EPM1270T144C5N

JTAG

1. TCK (0) 2. GND
3. TDO (1) 4. +V
5. TMS (1) 6. RESET
7. +V 8. NC
9. TDI (1) 10. GND

P1407

I2S from ADC

I2S out from CPLD to SRCs

HDMI_RX1&2_AUDIO

Audio clk

For 48KHz and multiple

For 44.1Khz and multiple

30. CPLD controller for global digital audio routing

U1402

SN65LVDS352PWG4

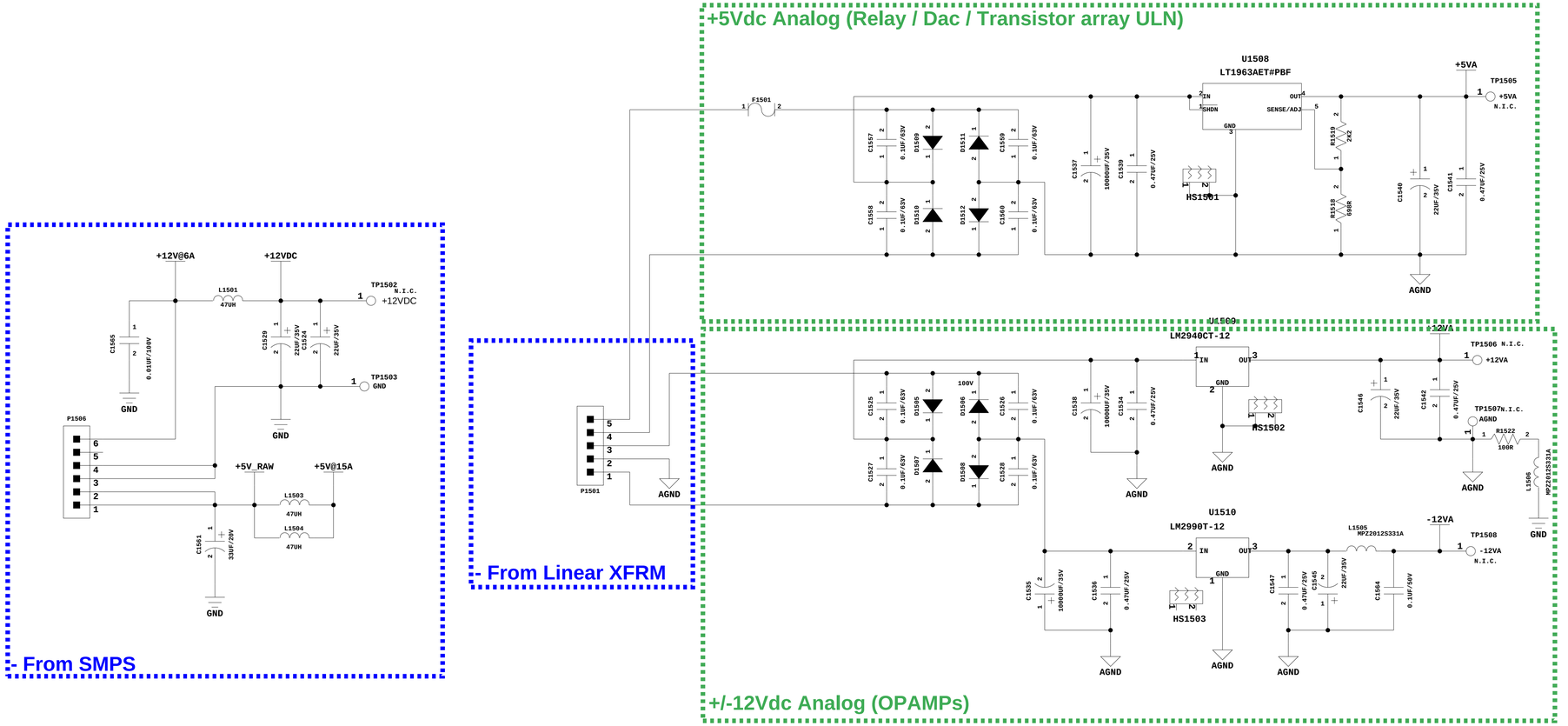
29. LVDS conversion of ADC digital audio output

TITLE

R6703-04-00S

SIZE	DWG NO	REV
D		A

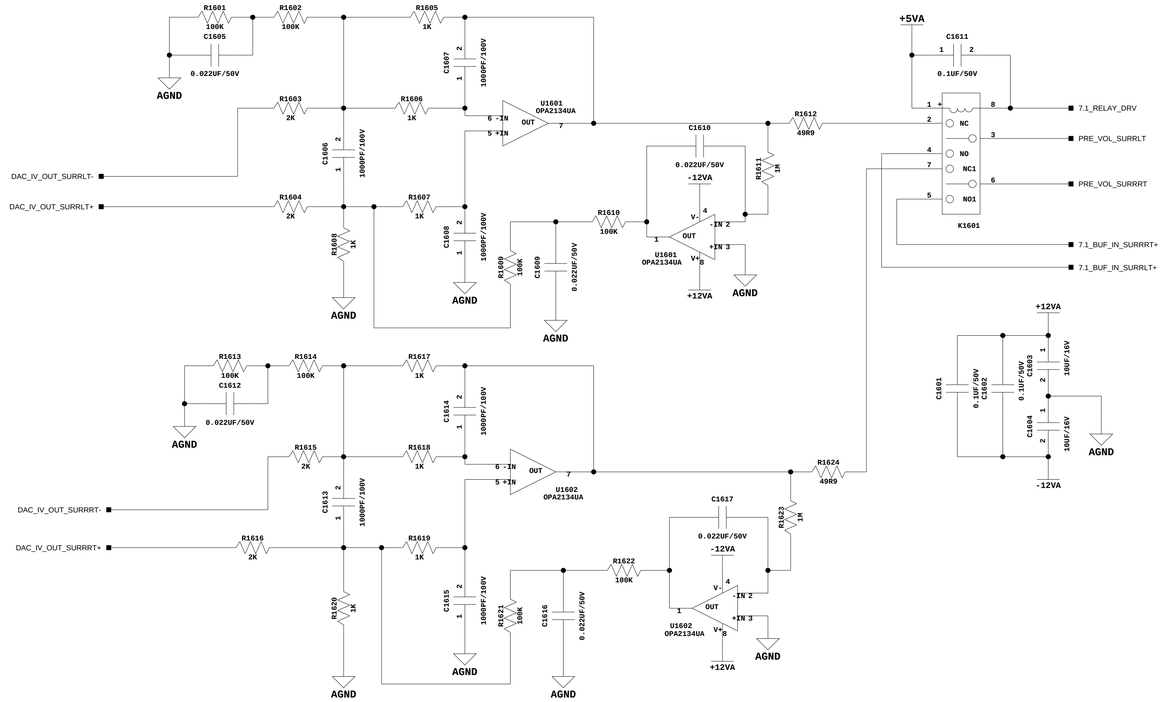
DRAWN BY: R.K. | SCALE | SHEET 14 of 17 | 6-19-2009_10:37



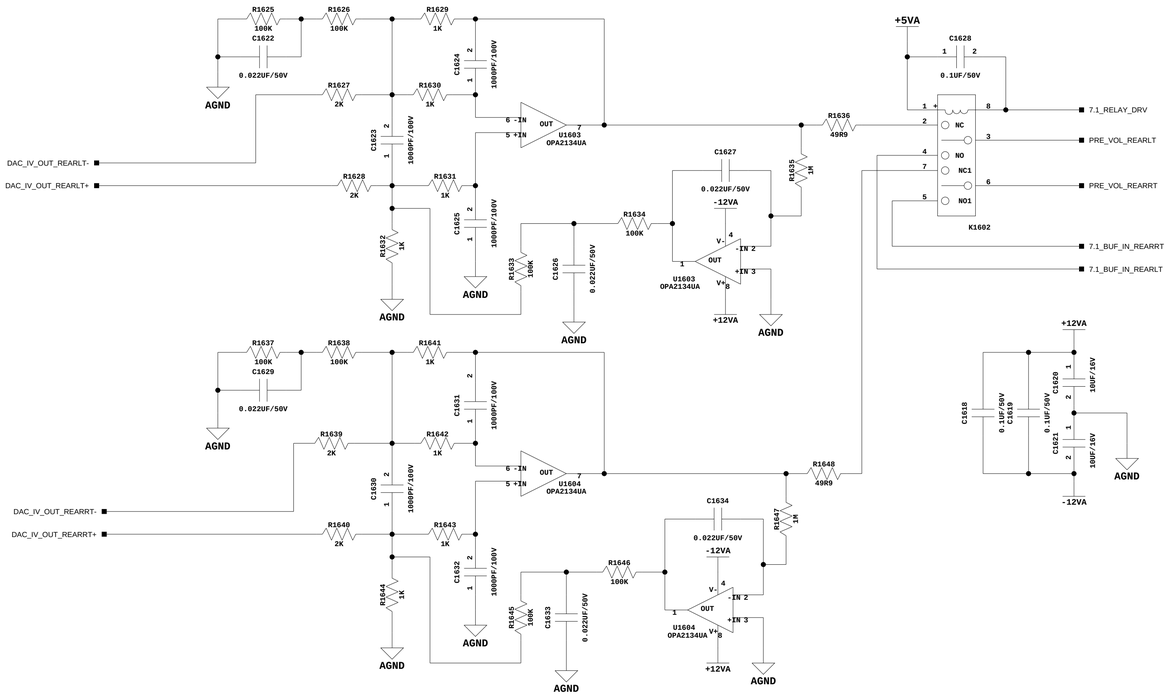
TITLE	R6703-04-00S	
SIZE D	DWG NO	REV A
DRAWN BY: R.K.	SCALE	SHEET 15 of 17

6-19-2009_10:37

31. 7.1 Bypass relays, audio buffers and DC Servo for Surrounds channels



32. 7.1 Bypass relays, audio buffers and DC Servo for Rears channels



	TITLE	
	R6703-04-00S	
SIZE D	DWG NO	REV A
DRAWN BY: R.K.	SCALE	SHEET 16 of 17 6-19-2009_10:37

ECN HISTORY:

ECN351 - 2007/12/18:
Rev. Document number to R6703-02-01S
Change all instances of G201-1367-XR00 (1000pF 100V 1%) to G201-1461-XR00 (1000pF 100V 2.5%).
Added missing Silpads (G307-1078-XR00) for BOM

ECN359 - 2008/01/11:
Rev. Document number to R6703-02-02S
Change U102 to G208-1407-XR00 (BOM Error).
Change R517 - R520 and R522 - R525 to G211-1764-XR00.
Change R1203, R1204, R1213, R1214, R1303, R1304, R1313, R1314 to G211-1728-XR00.
Change R1205, R1206, R1215, R1216, R1305, R1306, R1315, R1316 to G211-1926-XR00.

ECN368 - 2008/02/01:
Rev. Document number to R6703-02-03S
Change R108 to N.I.C.
Change R517 - R520 and R522 - R525 to G211-1944-XR00.
Change R319, R320, R321, R322, R417, R418, R419, R420, R422, R423, R424, R425 to G211-1837-XR00.
Change R603, R604, R615, R616, R627, R628, R639, R640 to G211-1736-XR00.
Change R703, R704, R715, R716, R727, R728, R739, R740 to G211-1736-XR00.
Change R803, R804, R815, R816, R827, R828, R839, R840 to G211-1736-XR00.
Change U902, U903, U904, U905, U1002, U1003, U1004, U1005, U1102, U1103, U1104, U1105 to 51150978-00.

ECN370 - 2008/02/05:
Rev. Document number to R6703-03-00S
Board revision for mechanical issues.
Added R1501 (NIC) as alternate for L1503, L1504 if required.

ECN396 - 2008/04/29:
Rev. Document number to R6703-03-01S
Revised for EMI issues.

ECN428 - 2008/08/27:
Rev. Document number to R6703-03-02S
Change C529-C532 and C542-C545 to G201-1461-XR00

ECN432 - 2008/10/06:
Change P102, P1505, TP202, TP204, TP301, TP901-906, TP1003-1006, TP1101-1106, TP1203-1206, TP1303-1306, TP1502, TP1505-1512, TP1514 to N.I.C.

ECN329 - 2008/12/02:
Change D1505 - D1512 to p/n 51096528-00.

ECN457 - 2009/01/14:
Rev. Document number to R6703-03-03S
Change C1413, C1414, C1415, C1436 to N.I.C.

ECN512 - 2009/06/19:
Rev. Document number to R6703-04-00S
Board revision for EMI and manufacturing issues. See ECN for details.

1. AVR
2. DAE-7 and PS
3. ANALOG CPLD, AUX LT/RT SRC and DAC
4. CEN, SUB, MAIN LR SRC and DAC
5. SURR, REAR, SRC and DAC
6. AUX LR LPF
7. MAIN LR LPF
8. CEN_SUB LPF
9. AUX, MAIN LR VOL and AUX OUTPUT
10. MAIN LR OUTPUT
11. SURR, REAR, SUB, CEN VOL and CEN, SUB OUTPUT
12. SURR OUTPUT
13. REAR OUTPUT
14. DIGITAL CPLD
15. ANALOG POWER SUPPLY
16. SURR, REAR LPF

PARTS FOR ACCOUNTING & BOM

PCB	51073832-04	R6703M04	PCB DELTA SSP800 MOTHER BOARD R6703M04
HS1	G307-1078-XR00	PS-09-2201-A	THERMAL PAD TO-220 SIL-PAD 1000
HS2	G307-1078-XR00	PS-09-2201-A	THERMAL PAD TO-220 SIL-PAD 1000
HS3	G307-1078-XR00	PS-09-2201-A	THERMAL PAD TO-220 SIL-PAD 1000

TITLE
R6703-04-00S

SIZE	DWG NO	REV
D		A

DRAWN BY: R.K. | SCALE | SHEET 17 of 17 | 6-19-2009_16:35