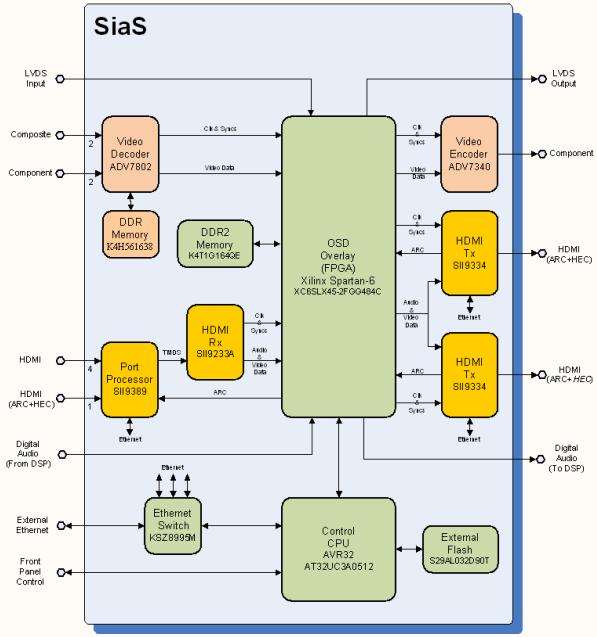
REVISION

REV	DESCRIPTION. / REF. ECN #	DATE	DWN. BY.	APPR.
00	REV 00 BOARD RELEASE	5-05-10	MAB	
01	REV 01 BOARD RELEASE	8-11-10	MAB	
02	ECN: 10002223	10-5-10	MAB	



U_P2-CONTROL INTERFACE
P2-CONTROL INTERFACE.SchDoc

U_P3- HDMI_INPUT
P3- HDMI_INPUT.SchDoc

U_P4-HDMI_INPUTS
P4- HDMI_INPUT.SchDoc

U_P5-HDMI 5:1 MUX
P5-HDMI 5 TO 1 MUX.SchDoc

U_P6-HDMI RECIEVER-SII9233A
P6-HDMI RECIEVER-SII9233A.SchDoc

U_P7_HDMI TX1
P7_HDMITX1_SII9334.SchDoc

U_P8_HDMI TX2
P8_HDMITX2_SII9334.SchDoc

U_P9 - FPGA
P9 - FPGA.SchDoc

U_P10 -FPGA
P10 -FPGA.SchDoc

U_P11 -FPGA_DDR
P11 -FPGA_DDR.SchDoc

U_P12-VIDEO INPUT
P12-VIDEO INPUT.SchDoc

U_P13-VIDEO_DECODER
P13-VIDEO_DECODER.SchDoc

U_P14 - VIDEO_DAC
P14 - VIDEO_DAC.SchDoc

U15_ETHERNET SWITCH
P15-ETHERNET SWITCH.SchDoc

U_P16 - POWER
P16 - POWER.SchDoc

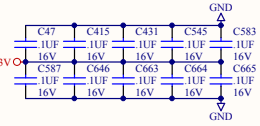
BOARD SILK

SERIAL NUMBER

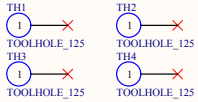
QC STAMP

BOARD INFORMATION

PLANE STITCHING CAPS

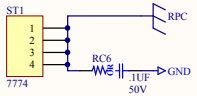


TOOLING HOLES

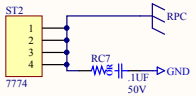


GLOBAL FIDUCIALS

HORIZONTAL SUPPORT BRACKET



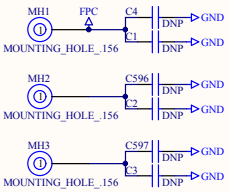
HORIZONTAL SUPPORT BRACKET



RPC Chassis strap across board, RP

LAYOUT NOTE GND or Chassis/FPC strap (TBD) across board, bottom side, above power wiring harness.

MOUNTING HOLES



EMI caps top and bottom PCB planes, 2X vias all

POWER TREE:

+5V, Power Main input, all PCB power; HDMI sink OR

+5V_H, HDMI source conn (only)

+5V: +3.3V, +2.5V, +1.8V/+1.8V_2, 5V-ANA (analog out), +V_AMP1 (analog in), misc

+3.3V: +1.2V, ADV7802, FPGA Banks 0/2/3, alt FPGA VCCAUX, Atmel uC, SII9334, SiI9233A, SiI9389, ADV7340, KSC8995, generic digital

+2.5V: ADV7802 & DDR, +1.25Vref/Vtt; alt FPGA VCCAUX

+1.8V: ADV7802, ADV7340, KS8995, FPGA Bank 1 & DDR2, alt uC Core

+1.2V: FPGA Core; SiI9334, SiI9233A, SiI9389 Cores

sequenced: +3.3V / +1.2V SiI9233A & SiI9389; +1.8V vs 3.3V ADV7340

I2C ADDRESS:

0xB2/B3, 0xBA/BB, 0xC0/C1*, 0xD0/D1*, & 0xE0/E1*, 0xE6/E7*, 0x64/65*, 0x66/67*, 0x68/69*, 0x90/91*	SiI9389 HDMI PORT PROC
0x60/61, 0x68/69, 0x64/65*, 0xC0/C1*, 0xE0/E1*, 0xE6/E7*, 0x90/91*	SII9233A HDMI RX
0x72/73, 0x7A/7B, 0xC0/C1, 0x90/91	SiI9334 HDMI TX 1
0x76/77, 0x7E/7F, 0xC4/C5, 0x94/95	SiI9334 HDMI TX 2
0x3A/0x3B XC3S1200E-5FGG400C FPGA**	
0xD6/D7	ADV7340 VIDEO DAC
0x58/59	THS7353 CH1 VIDEO BUFFER MUX
0x5A/5B	THS7353 CH2 VIDEO BUFFER MUX
0x42/43, 0x62/63*, 0x82/83*, 0x22/23*, 0x52/53	ADV7802 VIDEO

NOTES UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE LISTED IN OHMS AND ARE 5%, 0603 FORM FACTOR AT 1/10W MINIMUM.
2. ALL CAPACITORS ARE LISTED IN MICROFARADS AND ARE 10%, 50V, CERAMIC, 0603 FORM FACTOR.
3. ALL INDUCTORS ARE LISTED IN MICROHENRIES.
4. NET LABELS AND PORTS ARE GLOBAL AND ARE ALL CONNECTED THROUGH SHEET SYMBOLS.

ASSOCIATED DOCUMENTS

PCB: 10001940-B00
ASSEM DWG: 10001941-CXX
BOM: 10001941-DXX
PICK-N-PLACE: NA

PROPRIETARY AND CONFIDENTIAL

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INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)

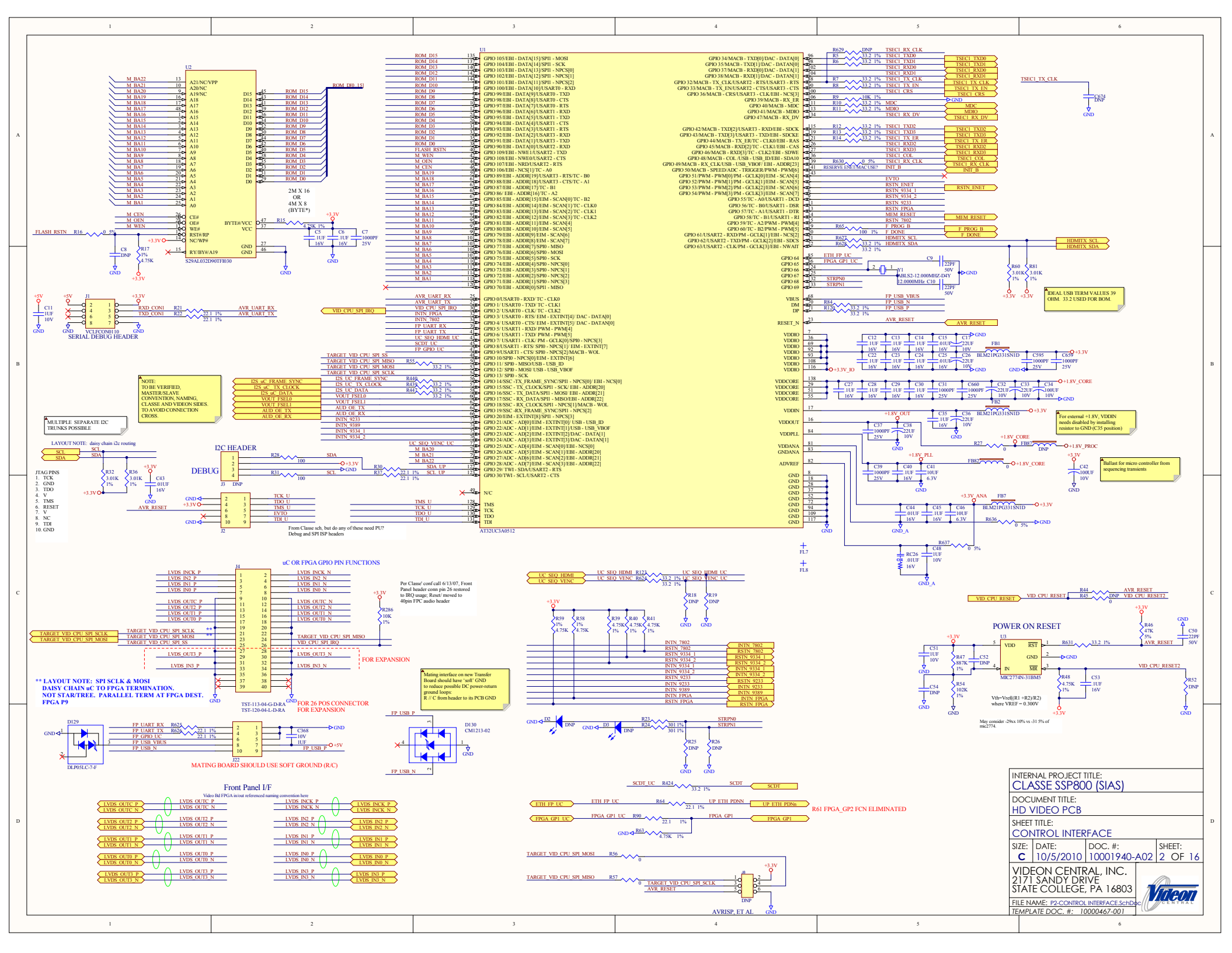
DOCUMENT TITLE:
HD VIDEO PCB

SHEET TITLE:
TOP LEVEL

SIZE:	DATE:	SCH. DOC. #:	SHEET:
B	10/5/2010	10001940-A02	1 OF 16

VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: 10001940-A.prj
TEMPLATE DOC. #: 10000465-001


U1
AT32UC3A0512
U2
S29AL032D90TFI030
2M X 16
OR
4M X 8
(BYTE*)
J1
SERIAL DEBUG HEADER
VCLFCON00110
J3
I2C HEADER
DEBUG
J2
J4
J22
D129
DLP05LC-7-F
D130
CM1213-02
U3
MIC2774N-31BM5
JTAG PINS
1. TCK
2. GND
3. TDO
4. V
5. TMS
6. RESET
7. V
8. NC
9. TDI
10. GND
MULTIPLE SEPARATE I2C TRUNKS POSSIBLE
LAYOUT NOTE: daisy chain i2c routing
NOTE:
TO BE VERIFIED,
MASTER/SLAVE
CONVENTION, NAMING,
CLASSE AND VIDEON SIDES.
TO AVOID CONNECTION
CROSS.
From Classe sch, but do any of these need PU?
Debug and SPI ISP headers
uC OR FPGA GPIO PIN FUNCTIONS
Per Classe' conf call 6/13/07, Front
Panel header conn pin 26 restored
to IRQ usage; Reset' moved to
40pin FPC audio header
** LAYOUT NOTE: SPI SCLK & MOSI
DAISY CHAIN uC TO FPGA TERMINATION.
NOT STAR/TREE. PARALLEL TERM AT FPGA DEST.
FPGA P9
FOR EXPANSION
FOR 26 POS CONNECTOR
FOR EXPANSION
TST-113-04-G-D-RA
TST-120-04-L-D-RA
MATING BOARD SHOULD USE SOFT GROUND (R/C)
Mating interface on new Transfer
Board should have 'soft' GND
to reduce possible DC power-return
ground loops:
R // C from header to its PCB GND
Front Panel I/F
Video Bd FPGA in/out referenced naming convention here
POWER ON RESET
Vth=Vref((R1 +R2)/R2)
where VREF = 0.300V
May consider -29xx 10% vs -31 5% of
mic2774.
R61 FPGA_GP2 FCN ELIMINATED
AVRISP_ET AL
IDEAL USB TERM VALUES 39
OHM. 33.2 USED FOR BOM.
For external +1.8V, VDDIN
needs disabled by installing
resistor to GND (C35 position)
Ballast for micro controller from
sequencing transients
INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)
DOCUMENT TITLE:
HD VIDEO PCB
SHEET TITLE:
CONTROL INTERFACE
SIZE: C
DATE: 10/5/2010
DOC. #: 10001940-A02
SHEET: 2 OF 16
VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803
FILE NAME: P2-CONTROL INTERFACE.SchDoc
TEMPLATE DOC. #: 10000467-001

HDMI IN
HEAC PORT (HEC AND ARC)

PLACE CLOSE TO ESD DEVICE

J5

TMDS-D2-P
D2-SHIELD
TMDS-D2-N
TMDS-D1-P
D1-SHIELD
TMDS-D1-N
TMDS-D0-P
D0-SHIELD
TMDS-D0-N
TMDS-CLK-P
CLK-SHIELD
TMDS-CLK-N
HDMI-CEC
TMDS-SCL
TMDS-SDA
DDC-GND
+5V_POWER
HOT-PLUG-DET
NC
CH_GND
CH_GND
CH_GND
CH_GND

R66 5.1 1% HDMI0_D2_P
R67 5.1 1% HDMI0_D2_N
R68 5.1 1% HDMI0_D1_P
R69 5.1 1% HDMI0_D1_N
R71 5.1 1% HDMI0_D0_P
R72 5.1 1% HDMI0_D0_N
R74 5.1 1% HDMI0_CLK_P
R75 5.1 1% HDMI0_CLK_N

HDMI0_D2_P
HDMI0_D2_N
HDMI0_D1_P
HDMI0_D1_N
HDMI0_D0_P
HDMI0_D0_N
HDMI0_CLK_P
HDMI0_CLK_N

HCEC0 CEC CEC
QSCL0 FB10 0
QSDA0

TBD: caution CEC, watch DC R ohm pt-pt, ATC compliance; all places/connectors
TBD: ATC compliance (multiple test cases/conditions), also see Sil ref sch; all places

HDMI-CEC
TMDS-SCL
TMDS-SDA
DDC-GND
+5V_POWER
HOT-PLUG-DET

FB3 BLM21PG300SN1D
+5V_CBL_0
C16 1UF 16V
D23 MMBZ5234BLT1G
R97 DNP
R107 0
BAT54C
D5
?BYP_0?
+5V_DDC0
+5V_CBL_0
R121 10 1% CLOSE TO 9389 PROBABLY?
+5V_RPWR0

TBD DDC i2c pullup to on-board +5V or on-board/off-board OR'ed 5V? Sil Image schematics show on board VCC5, rather than connector 5V or OR'ed version.

+5V_DDC0
R260 47K 5%
R76 47K 5%

QSCL0 FB6 0 DDC0_SCL DDC0_SCL
QSDA0 FB19 0 DDC0_SDA DDC0_SDA
HCEC0

C55 DNP C56 DNP

DLP05LC-7-F D6
DLP05LC-7-F D7
DLP05LC-7-F D8

HPDET0
RSVD_HDMI_HEAC
D25 CM1213-02

CH_GND
CH_GND
CH_GND
CH_GND
VCLFCON0593
RC1 .1UF
RPC

May 0-ohm 'direct' connect RX ports shell to PCB GND, all places.
Pref RC option ea side of connector shell.

TBD:
NEED ESD AND EMI ON HEAC(HEC/ARC), HPD, AND PIN 14

CM????
FB44 FB8 0
C57 DNP C58 DNP
HPDET0
RSVD_HDMI_HEAC

HEC_N HEC_N
HEC_P HEC_P
L7 L8 1UH 1UH
HPD0 HPD0
RSVD1 RSVD1

LAYOUT NOTE P3-1

LAYOUT NOTE P3-1
1UH INDUCTORS & HEC_P/N AC-COUPLING CAPS CLOSE TO SIl9389
SHORT STUBS FROM INDUCTORS TO OUTPUT SIDE OF COUPLING CAPS.

HDMI0_D2_P
HDMI0_D2_N
HDMI0_CLK_P
HDMI0_CLK_N
HDMI0_D1_P
HDMI0_D1_N
HDMI0_D0_P
HDMI0_D0_N

CG0402MLC-12LG
D4 D9 D10 D11 D14 D15 D18 D22

HDMI IN
HDMI 2

PLACE CLOSE TO ESD DEVICE

J6

R77 5.1 1% HDMI1_D2_P
R78 5.1 1% HDMI1_D2_N
R80 5.1 1% HDMI1_D1_P
R83 5.1 1% HDMI1_D1_N
R85 5.1 1% HDMI1_D0_P
R86 5.1 1% HDMI1_D0_N
R87 5.1 1% HDMI1_CLK_P
R88 5.1 1% HDMI1_CLK_N

HDMI1_D2_P
HDMI1_D2_N
HDMI1_D1_P
HDMI1_D1_N
HDMI1_D0_P
HDMI1_D0_N
HDMI1_CLK_P
HDMI1_CLK_N

HCEC1 CEC CEC
QSCL1 FB4 0
QSDA1

FB5 BLM21PG300SN1D
+5V_CBL_1
C18 1UF 16V
D16 MMBZ5234BLT1G
R124 DNP
R125 0
BAT54C
D13
?BYP_0?
+5V_DDC1
+5V_CBL_1
R155 10 1% CLOSE TO 9389 PROBABLY?
+5V_RPWR1

+5V_DDC1
R262 47K 5%
R89 47K 5%

QSCL1 FB45 0 DDC1_SCL DDC1_SCL
QSDA1 FB46 0 DDC1_SDA DDC1_SDA
HCEC1

C59 DNP C60 DNP

DLP05LC-7-F D17
DLP05LC-7-F D39
DLP05LC-7-F D40

CH_GND
CH_GND
CH_GND
CH_GND
VCLFCON0593
RC2 .1UF
RPC

FIX PACKAGE 16-24V

D12
VCLFD0158
HPDET1
FB47 0
HPD1 HPD1

TBD: Qty 1 ESD per CEC connector pin (6), or 2 per CEC interconnected net OA (Rx, Tx); all places/connectors

HDMI 1.3 CEC Line spec 150pF max, 5ohm max (4.2.10)

HDMI1_D2_P
HDMI1_D2_N
HDMI1_CLK_P
HDMI1_CLK_N
HDMI1_D1_P
HDMI1_D1_N
HDMI1_D0_P
HDMI1_D0_N

CG0402MLC-12LG
D26 D27 D28 D29 D30 D31 D32 D33

HDMI IN
HDMI 3

PLACE CLOSE TO ESD DEVICE

J7

R91 5.1 1% HDMI2_D2_P
R92 5.1 1% HDMI2_D2_N
R93 5.1 1% HDMI2_D1_P
R94 5.1 1% HDMI2_D1_N
R95 5.1 1% HDMI2_D0_P
R96 5.1 1% HDMI2_D0_N
R98 5.1 1% HDMI2_CLK_P
R109 5.1 1% HDMI2_CLK_N

HDMI2_D2_P
HDMI2_D2_N
HDMI2_D1_P
HDMI2_D1_N
HDMI2_D0_P
HDMI2_D0_N
HDMI2_CLK_P
HDMI2_CLK_N

HCEC2 CEC CEC
QSCL2 FB48 0
QSDA2

FB50 BLM21PG300SN1D
+5V_CBL_2
C19 1UF 16V
D58 MMBZ5234BLT1G
R156 DNP
R157 0
BAT54C
D57
?BYP_0?
+5V_DDC2
+5V_CBL_2
R160 10 1% CLOSE TO 9389 PROBABLY?
+5V_RPWR2

+5V_DDC2
R272 47K 5%
R101 47K 5%

QSCL2 FB49 0 DDC2_SCL DDC2_SCL
QSDA2 FB51 0 DDC2_SDA DDC2_SDA
HCEC2

C61 DNP C62 DNP

DLP05LC-7-F D59
DLP05LC-7-F D60
DLP05LC-7-F D61

CH_GND
CH_GND
CH_GND
CH_GND
VCLFCON0593
RC3 .1UF
RPC

D62
VCLFD0158
HPDET2
FBS2 0
HPD2 HPD2

HDMI2_D2_P
HDMI2_D2_N
HDMI2_CLK_P
HDMI2_CLK_N
HDMI2_D1_P
HDMI2_D1_N
HDMI2_D0_P
HDMI2_D0_N

CG0402MLC-12LG
D37 D38 D41 D49 D50 D52 D53 D54

LAYOUT NOTE:

ON HDMI TRACES RUN AS DIFFERENTIAL PAIRS AND FOLLOW HDMI RULES. MATCHED IMPEDANCE 3W ETC

INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)

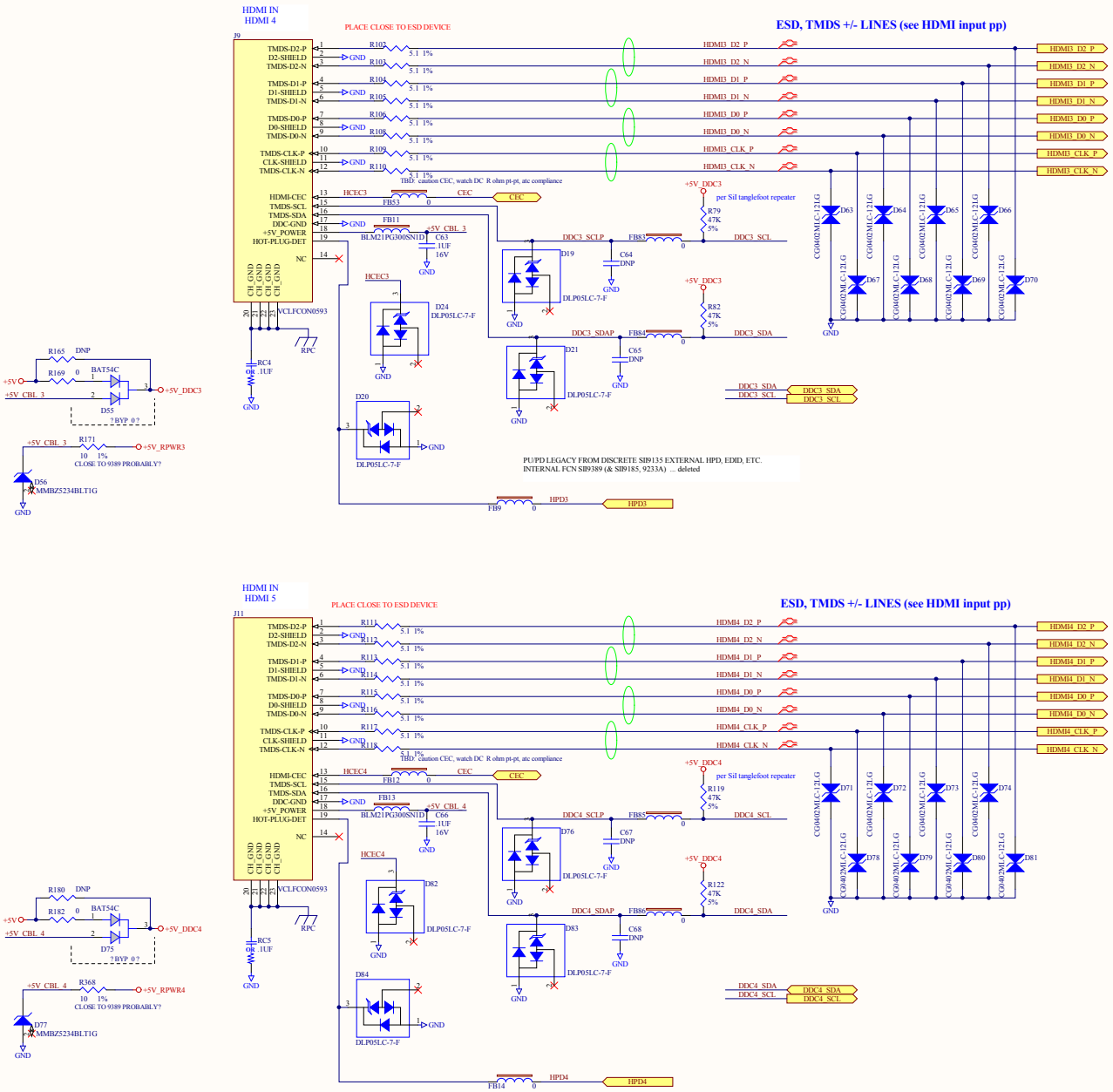
DOCUMENT TITLE:
HD VIDEO PCB

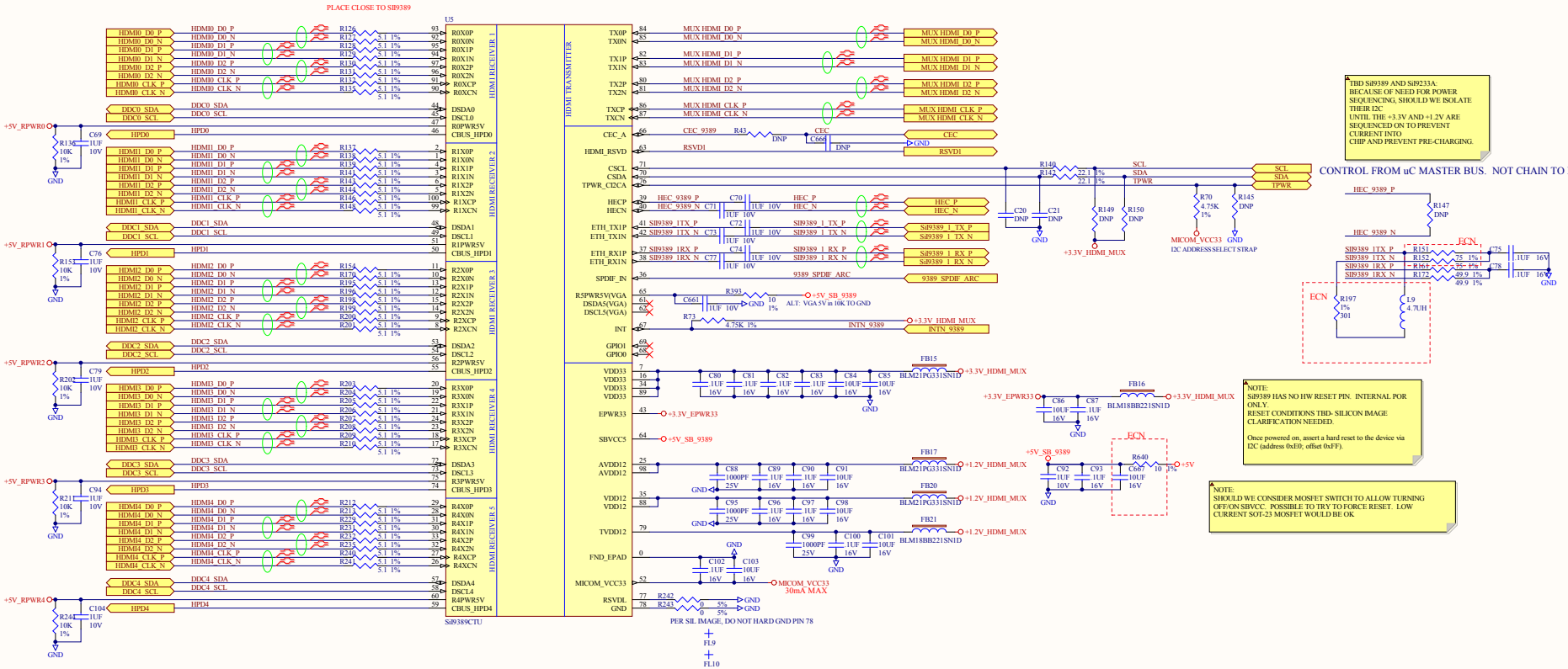
SHEET TITLE:
HDMI INPUTS

SIZE:	DATE:	DOC. #:	SHEET:
C	10/5/2010	10001940-A02	3 OF 16

VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: P3- HDMI_INPUT.SchDoc
TEMPLATE DOC. #: 10000467-001


HDMI IN
HDMI 4
J9
PLACE CLOSE TO ESD DEVICE
ESD, TMDS +/- LINES (see HDMI input pp)
TMDS-D2-P
D2-SHIELD
TMDS-D2-N
TMDS-D1-P
D1-SHIELD
TMDS-D1-N
TMDS-D0-P
D0-SHIELD
TMDS-D0-N
TMDS-CLK-P
CLK-SHIELD
TMDS-CLK-N
HDMI-CEC
TMDS-SCL
TMDS-SDA
DDC-GND
+5V_POWER
HOT-PLUG-DET
NC
CH_GND
CEC
HDMI3_D2_P
HDMI3_D2_N
HDMI3_D1_P
HDMI3_D1_N
HDMI3_D0_P
HDMI3_D0_N
HDMI3_CLK_P
HDMI3_CLK_N
TBD: caution CEC, watch DC R ohm pt-pt, atc compliance
per Sil tanglefoot repeater
DDC3_SCLP
DDC3_SDAP
DDC3_SCL
DDC3_SDA
VCLFCON0593
RPC
PU/PD LEGACY FROM DISCRETE SII9135 EXTERNAL HPD, EDID, ETC.
INTERNAL FCN SII9389 (& SII9185, 9233A) ... deleted
HPD3
+5V_CBL_3
+5V_DDC3
+5V_RPWR3
R165 DNP
R169 0
BAT54C
D55
?BYP 0?
R171
10 1%
CLOSE TO 9389 PROBABLY?
D56
MMBZ5234BLT1G
HDMI IN
HDMI 5
J11
HDMI4_D2_P
HDMI4_D2_N
HDMI4_D1_P
HDMI4_D1_N
HDMI4_D0_P
HDMI4_D0_N
HDMI4_CLK_P
HDMI4_CLK_N
DDC4_SCLP
DDC4_SDAP
DDC4_SCL
DDC4_SDA
HPD4
+5V_CBL_4
+5V_DDC4
+5V_RPWR4
R180 DNP
R182 0
D75
R368
D77
TBD: Qty 1 ESD per CEC connector pin (6), or 2 per CEC interconnected net OA (Rx, Tx); all places/connectors
HDMI 1.3 and HDMI 1.4 CEC Line spec 150pF max, 5ohm max (4.2.10)
HDMI 1.3 and HDMI 1.4 spec on DDC_SDA and DDC_SCL 50pF Max.
TBD DDC i2c pullup to on-board +5V or on-board/off-board OR'ed 5V? Sil Image schematics show on board VCC5, rather than connector 5V or OR'ed version.
LAYOUT NOTE:
ON HDMI TRACES RUN AS DIFFERENTIAL PAIRS AND FOLLOW HDMI RULES. MATCHED IMPEDANCE 3W ETC
INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)
DOCUMENT TITLE:
HD VIDEO PCB
SHEET TITLE:
HDMI INPUTS
SIZE: C
DATE: 10/5/2010
DOC. #: 10001940-A02
SHEET: 4 OF 16
VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803
FILE NAME: P4- HDMI_INPUT.SchDoc
TEMPLATE DOC. #: 10000467-001



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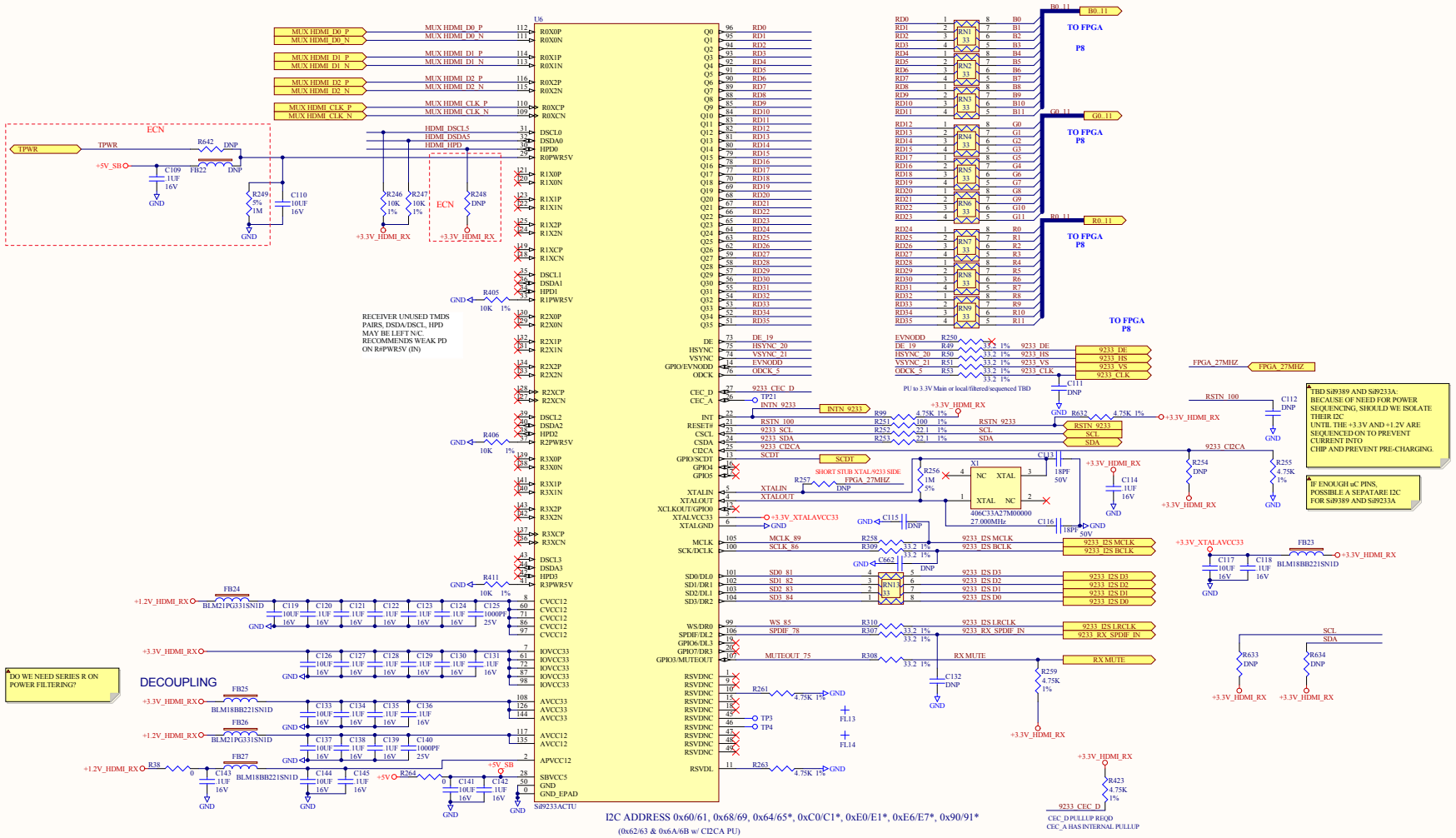
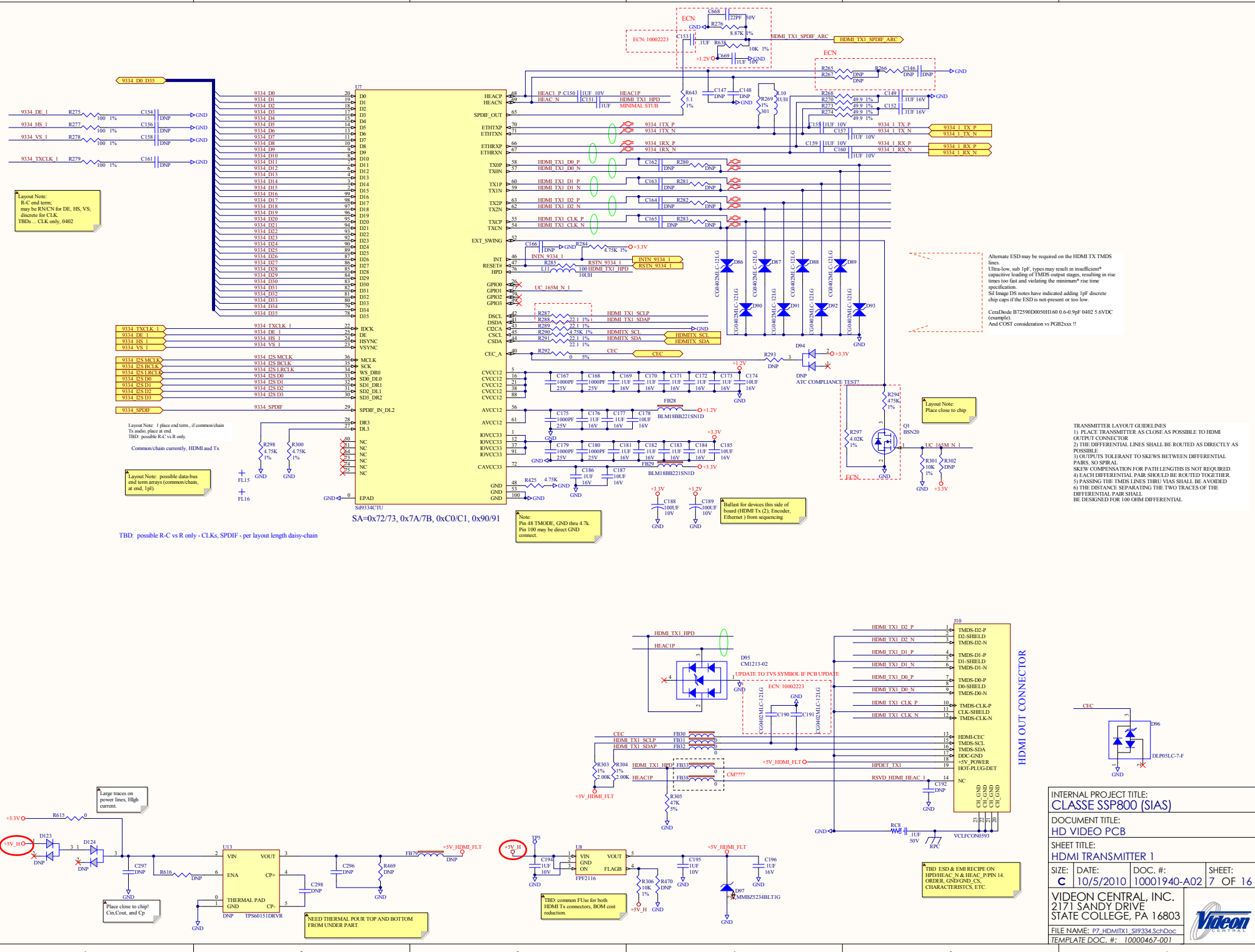
DOCUMENT TITLE:	HD VIDEO PCB
SHEET TITLE:	HDMI 3:1 MUX
SIZE: C	DATE: 10/5/2010
DOC. #:	10001940-A02
SHEET:	5 OF 16
VIDEON CENTRAL, INC. 2171 SANDY DRIVE STATE COLLEGE, PA 16803	
FILE NAME: P5-HDMI 5 TO 1 MUX.SchDoc	
TEMPLATE DOC. #: 10000467-001	

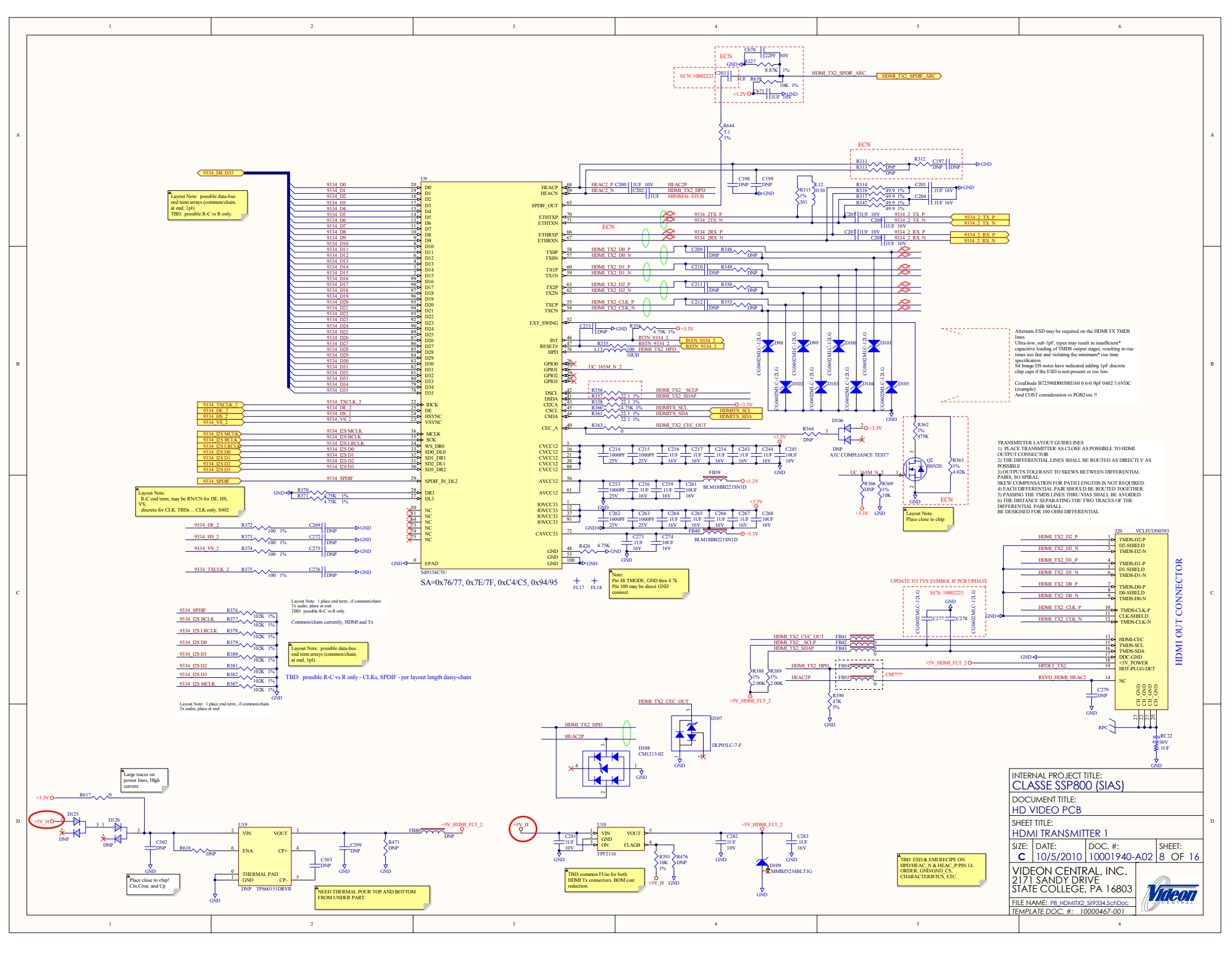


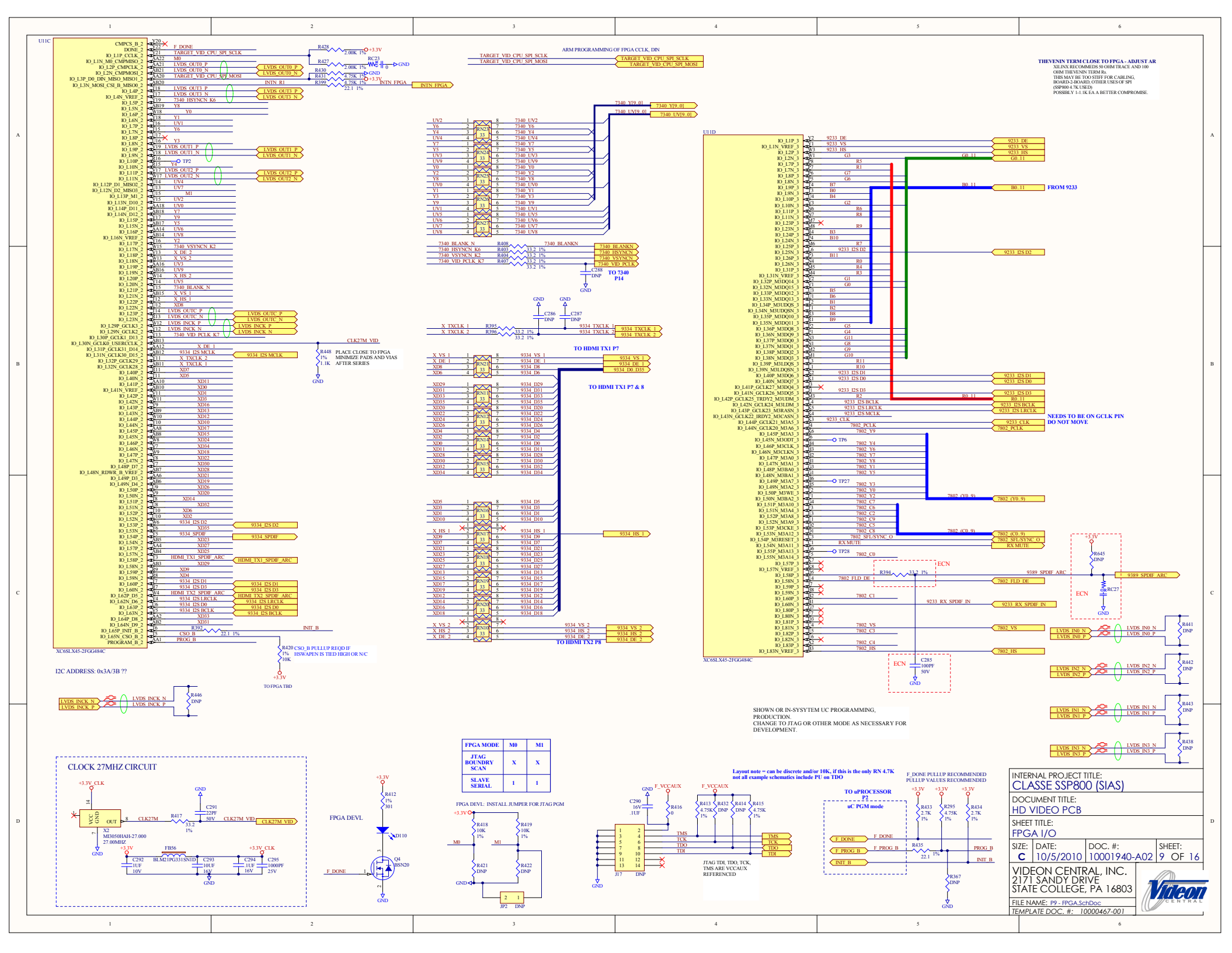
INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)			
DOCUMENT TITLE: HD VIDEO PCB			
SHEET TITLE: HDMI RECIEVER			
SIZE: C	DATE: 10/5/2010	DOC. #: 10001940-A02	SHEET: 6 OF 16

VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: P6-HDMI RECIEVER-SII9233A.SchDoc
TEMPLATE DOC. #: 10000467-001


U7
Sil9334CTU
SA=0x72/73, 0x7A/7B, 0xC0/C1, 0x90/91
TBD: possible R-C vs R only - CLKs, SPDIF - per layout length daisy-chain
Layout Note:
R-C end term;
may be RN/CN for DE, HS, VS;
discrete for CLK.
TBDs ... CLK only, 0402
Layout Note: 1 place end term., if common/chain
Tx audio, place at end.
TBD: possible R-C vs R only.
Common/chain currently, HDMI aud Tx
Layout Note: possible data-bus
end term arrays (common/chain,
at end, 1pl).
Note:
Pin 48 TMODE, GND thru 4.7k.
Pin 100 may be direct GND
connect.
Ballast for devices this side of
board (HDMI Tx (2), Encoder,
Ethernet) from sequencing
ECN
ECN: 10002223
HDMI_TX1_SPDIF_ARC
ATC COMPLIANCE TEST?
Alternate ESD may be required on the HDMI TX TMDS
lines.
Ultra-low, sub 1pF, types may result in insufficient*
capacitive loading of TMDS output stages, resulting in rise
times too fast and violating the minimum* rise time
specification.
Sil Image DS notes have indicated adding 1pF discrete
chip caps if the ESD is not-present or too low.
CeraDiode B72590D0050H160 0.6-0.9pF 0402 5.6VDC
(example).
And COST consideration vs PGB2xxx !!
TRANSMITTER LAYOUT GUIDELINES
1) PLACE TRANSMITTER AS CLOSE AS POSSIBLE TO HDMI
OUTPUT CONNECTOR
2) THE DIFFERENTIAL LINES SHALL BE ROUTED AS DIRECTLY AS
POSSIBLE
3) OUTPUTS TOLERANT TO SKEWS BETWEEN DIFFERENTIAL
PAIRS, SO SPIRAL
SKEW COMPENSATION FOR PATH LENGTHS IS NOT REQUIRED.
4) EACH DIFFERENTIAL PAIR SHOULD BE ROUTED TOGETHER.
5) PASSING THE TMDS LINES THRU VIAS SHALL BE AVOIDED
6) THE DISTANCE SEPARATING THE TWO TRACES OF THE
DIFFERENTIAL PAIR SHALL
BE DESIGNED FOR 100 OHM DIFFERENTIAL
HDMI OUT CONNECTOR
J10
D95
CM1213-02
UPDATE TO TVS SYMBOL IF PCB UPDATE
ECN: 10002223
D96
DLP05LC-7-F
Large traces on
power lines, High
current.
Place close to chip!
Cin,Cout, and Cp
NEED THERMAL POUR TOP AND BOTTOM
FROM UNDER PART.
U13
TPS60151DRVR
U8
FPF2116
TBD: common FUse for both
HDMI Tx connectors, BOM cost
reduction.
TBD ESD & EMI RECIPE ON
HPD/HEAC_N & HEAC_P/PIN 14.
ORDER, GND/GND CS,
CHARACTERISTCS, ETC.
INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)
DOCUMENT TITLE:
HD VIDEO PCB
SHEET TITLE:
HDMI TRANSMITTER 1
SIZE: C
DATE: 10/5/2010
DOC. #: 10001940-A02
SHEET: 7 OF 16
VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803
FILE NAME: P7_HDMITX1_SII9334.SchDoc
TEMPLATE DOC. #: 10000467-001


U9
SI9934CTU
SA=0x76/77, 0x7E/7F, 0xC4/C5, 0x94/95
ECN
ECN: 10002223
HDMI_TX2_SPDIF_ARC
9334_D0..D35
Layout Note: possible data-bus end term arrays (common/chain, at end, 1pl). TBD: possible R-C vs R only.
Layout Note: R-C end term; may be RN/CN for DE, HS, VS; discrete for CLK. TBDs ... CLK only, 0402
Layout Note: 1 place end term., if common/chain Tx audio, place at end. TBD: possible R-C vs R only.
Common/chain currently, HDMI aud Tx
TBD: possible R-C vs R only - CLKs, SPDIF - per layout length daisy-chain
Note: Pin 48 TMODE, GND thru 4.7k. Pin 100 may be direct GND connect.
Alternate ESD may be required on the HDMI TX TMDS lines.
Ultra-low, sub 1pF, types may result in insufficient* capacitive loading of TMDS output stages, resulting in rise times too fast and violating the minimum* rise time specification.
Sil Image DS notes have indicated adding 1pF discrete chip caps if the ESD is not-present or too low.
CeraDiode B72590D0050H160 0.6-0.9pF 0402 5.6VDC (example).
And COST consideration vs PGB2xxx !!
TRANSMITTER LAYOUT GUIDELINES
1) PLACE TRANSMITTER AS CLOSE AS POSSIBLE TO HDMI OUTPUT CONNECTOR
2) THE DIFFERENTIAL LINES SHALL BE ROUTED AS DIRECTLY AS POSSIBLE
3) OUTPUTS TOLERANT TO SKEWS BETWEEN DIFFERENTIAL PAIRS, SO SPIRAL SKEW COMPENSATION FOR PATH LENGTHS IS NOT REQUIRED.
4) EACH DIFFERENTIAL PAIR SHOULD BE ROUTED TOGETHER.
5) PASSING THE TMDS LINES THRU VIAS SHALL BE AVOIDED
6) THE DISTANCE SEPARATING THE TWO TRACES OF THE DIFFERENTIAL PAIR SHALL BE DESIGNED FOR 100 OHM DIFFERENTIAL
UPDATE TO TVS SYMBOL IF PCB UPDATE
ECN: 10002223
HDMI OUT CONNECTOR
Large traces on power lines, HIgh current.
Place close to chip! Cin,Cout, and Cp
NEED THERMAL POUR TOP AND BOTTOM FROM UNDER PART.
TBD: common FUse for both HDMI Tx connectors, BOM cost reduction.
TBD ESD & EMI RECIPE ON HPD/HEAC_N & HEAC_P/PIN 14. ORDER, GND/GND_CS, CHARACTERISTCS, ETC.
INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)
DOCUMENT TITLE:
HD VIDEO PCB
SHEET TITLE:
HDMI TRANSMITTER 1
SIZE: C
DATE: 10/5/2010
DOC. #: 10001940-A02
SHEET: 8 OF 16
VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803
FILE NAME: P8_HDMITX2_SII9334.SchDoc
TEMPLATE DOC. #: 10000467-001



FPGA MODE	M0	M1
JTAG BOUNDRY SCAN	X	X
SLAVE SERIAL	1	1

INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)

DOCUMENT TITLE: HD VIDEO PCB

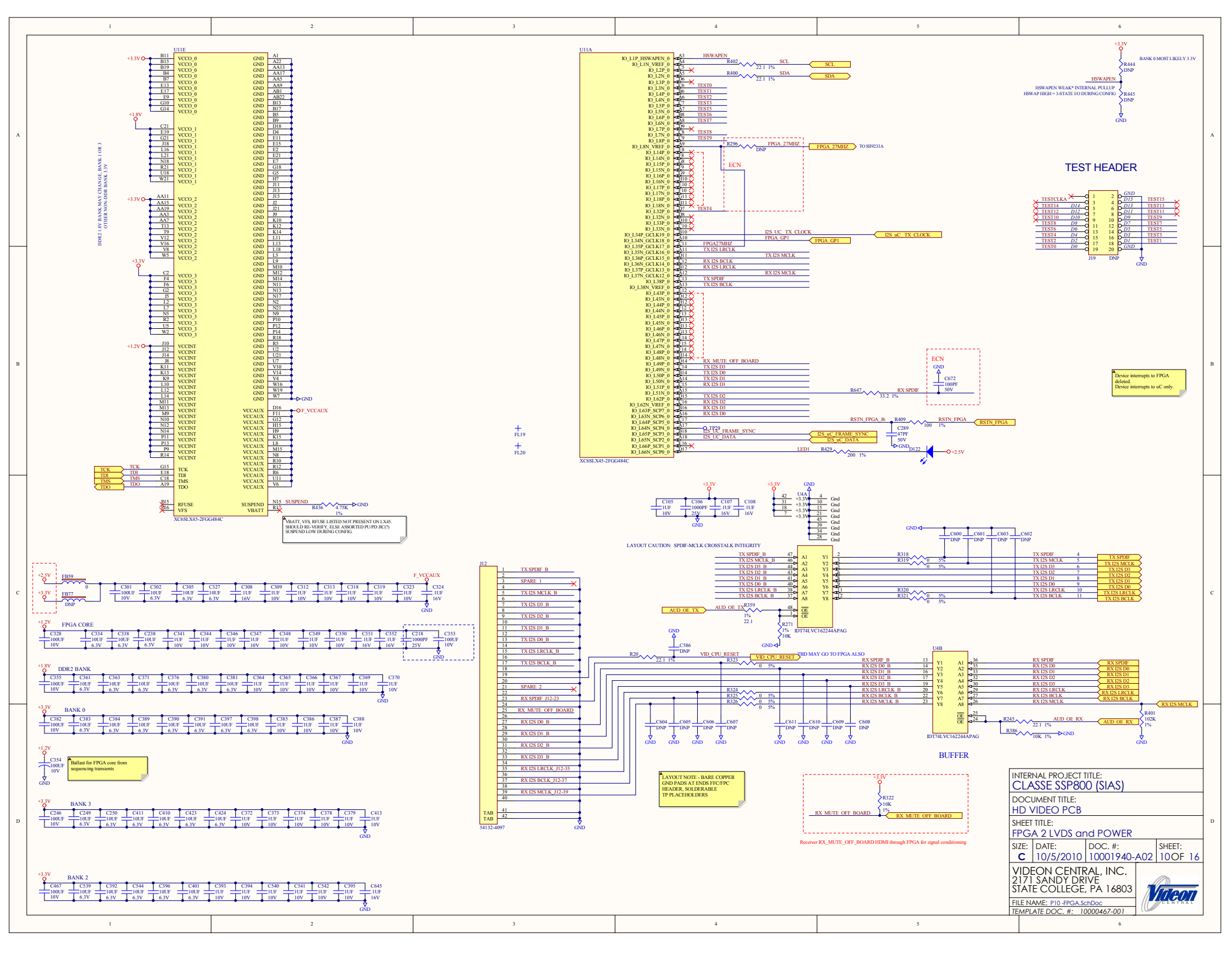
SHEET TITLE: FPGA I/O

SIZE:	DATE:	DOC. #:	SHEET:
C	10/5/2010	10001940-A02	9 OF 16

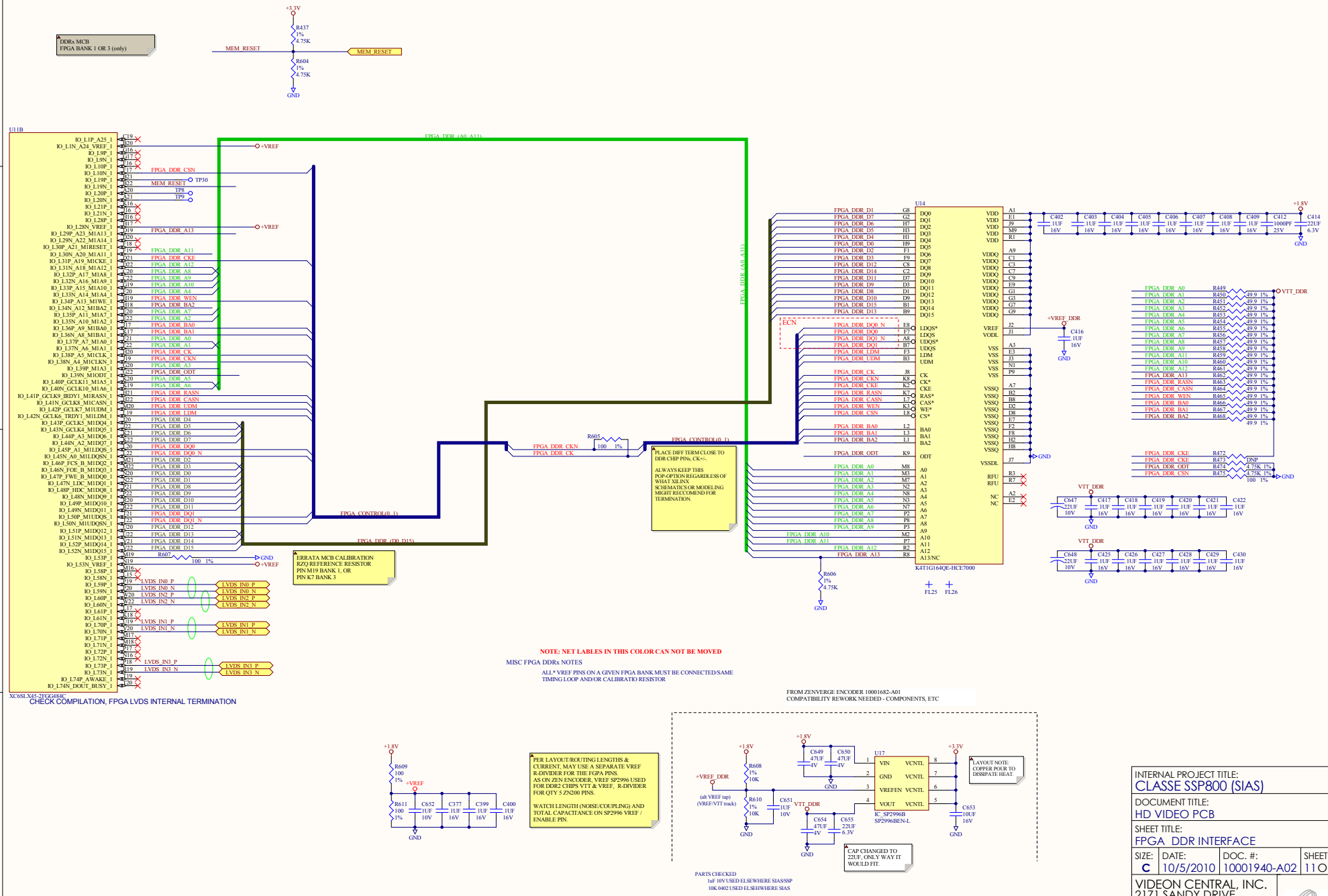
VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: P9 - FPGA.SchDoc

TEMPLATE DOC. #: 10000467-001



INTERNAL PROJECT TITLE:	CLASSE SSP800 (SIAS)
DOCUMENT TITLE:	HD VIDEO PCB
SHEET TITLE:	FPGA 2 LVDS and POWER
SIZE: C	DATE: 10/5/2010
DOC. #:	10001940-A02
SHEET:	10OF 16
VIDEON CENTRAL, INC. 2171 SANDY DRIVE STATE COLLEGE, PA 16803	
FILE NAME: P10 -FPGA.SchDoc	
TEMPLATE DOC. #: 10000467-001	

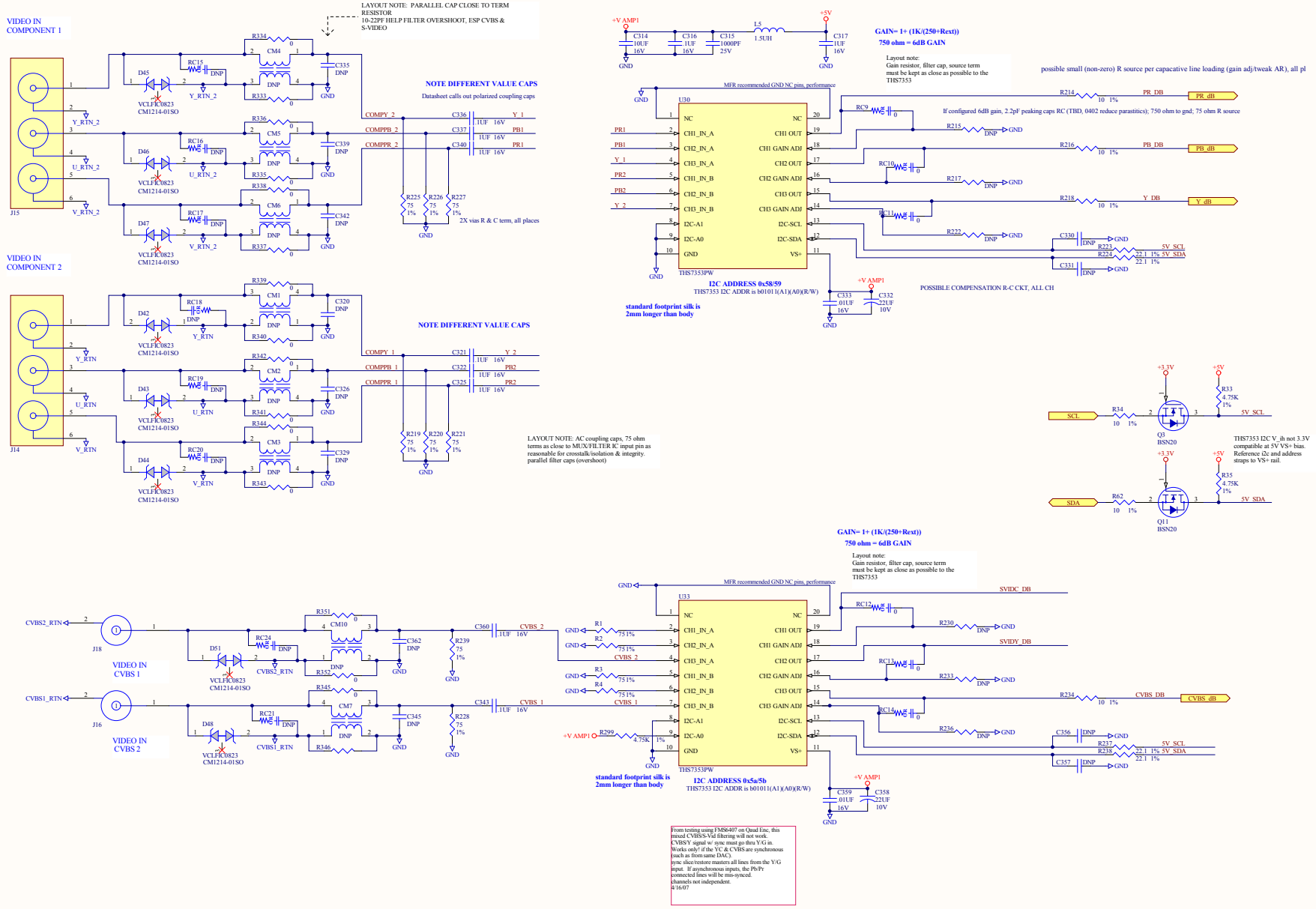


INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)			
DOCUMENT TITLE: HD VIDEO PCB			
SHEET TITLE: FPGA_DDR INTERFACE			
SIZE: C	DATE: 10/5/2010	DOC. #: 10001940-A02	SHEET: 11 OF 16

VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: P11 -FPGA_DDR.SchDoc

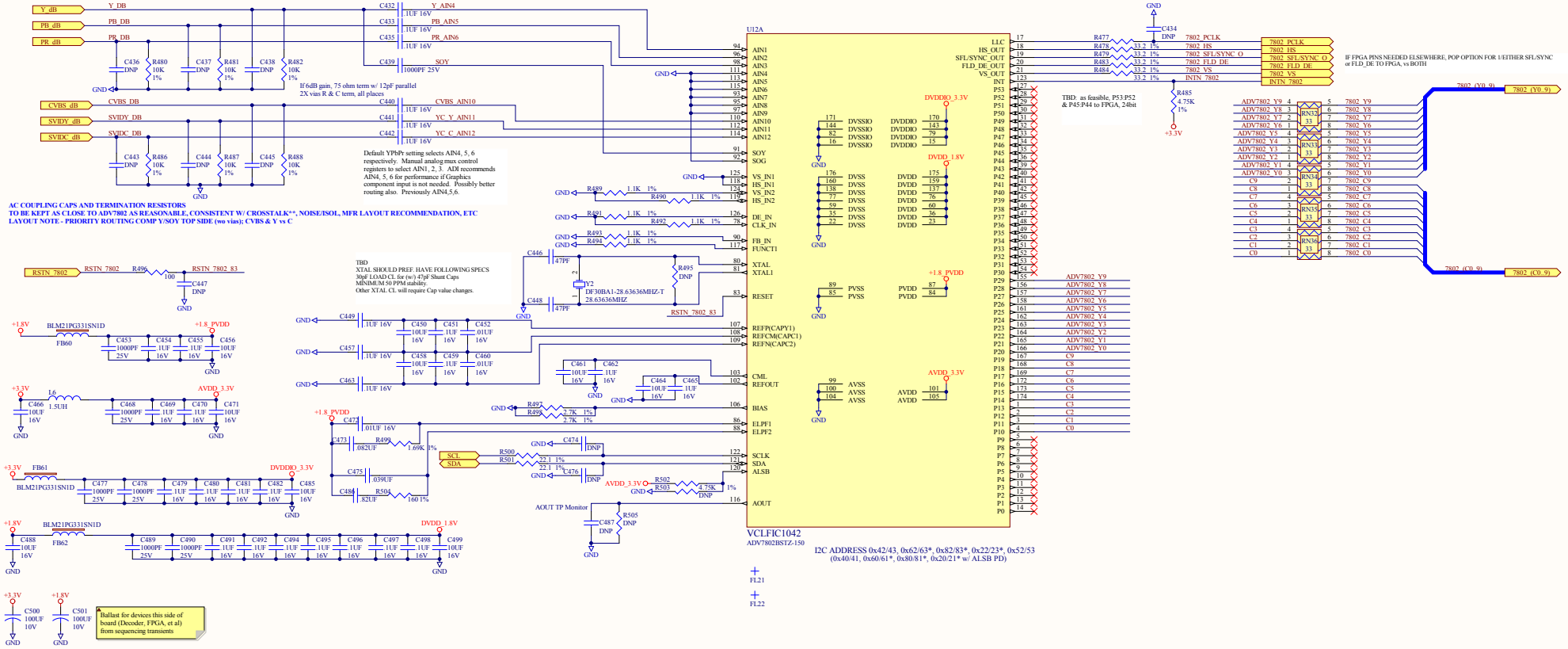
TEMPLATE DOC. #: 10000467-001



INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)			
DOCUMENT TITLE: HD VIDEO PCB			
SHEET TITLE: VIDEO INPUT			
SIZE: C	DATE: 10/5/2010	DOC. #: 10001940-A02	SHEET: 12OF 16

VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: P12-VIDEO INPUT.SchDoc
TEMPLATE DOC. #: 10000467-001



The ADV780x supports a DDR SDRAM memory interface for 3D comb, 3D DNR, and frame synchronizer operations as follows:

- 128 Mb and 256 Mb DDR SDRAM memory are supported
- Required memory architecture is four banks of 2 Mb x16 (8M16)
- Speed grade of 133 MHz at CAS Latency (CL) 2.5 is required
- Examples of 128 Mb compatible memory include (not necessarily Pb-free PN):

?? Samsung K4H281638B-TCB0
?? Micron MT46V8M16-TGP-75
?? Infineon HYB25D128160CE-6

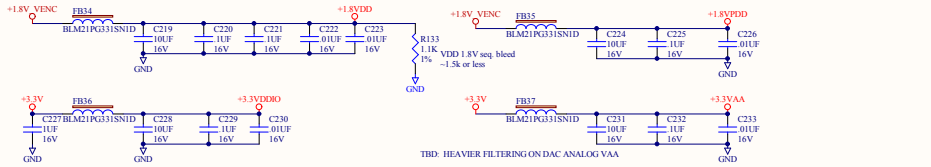
- Termination resistors are not recommended for this configuration

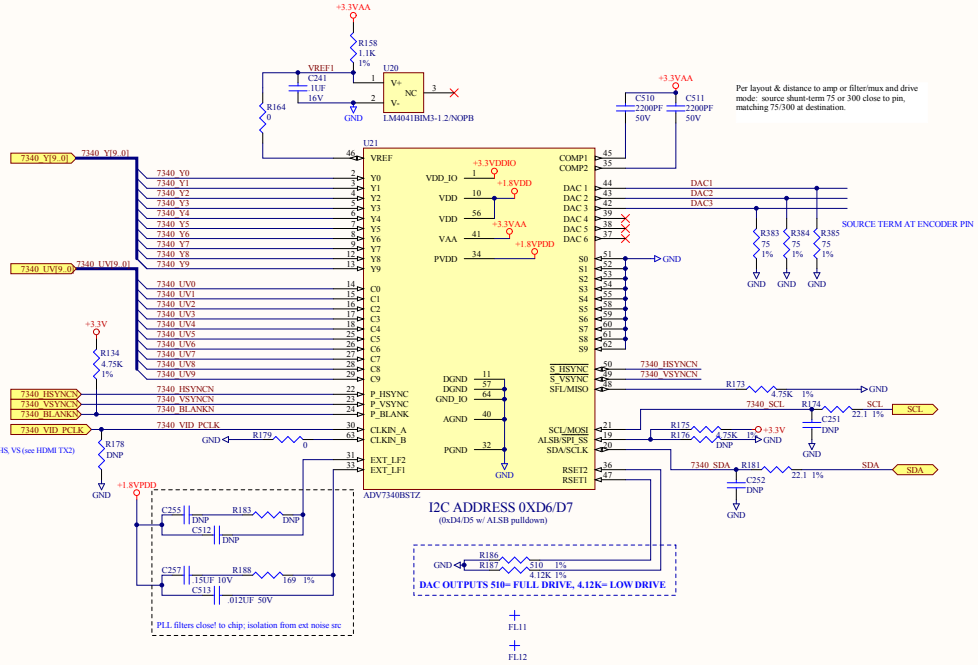
The specific layout requirements for external memory placement are provided in Figure 98.

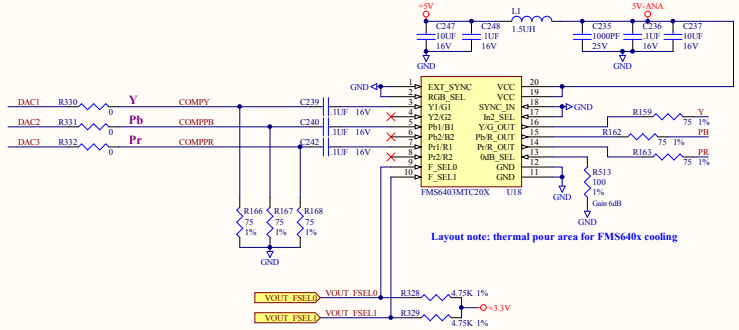
INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)			
DOCUMENT TITLE: HD VIDEO PCB			
SHEET TITLE: VIDEO DECODER ADV7802			
SIZE: C	DATE: 10/5/2010	DOC. #: 10001940-A02	SHEET: 13OF 16
VIDEON CENTRAL, INC. 2171 SANDY DRIVE STATE COLLEGE, PA 16803			
FILE NAME: P13-VIDEO_DECODER.SchDoc			
TEMPLATE DOC. #: 10000467-001			

NOTE: 3.3 VDDIO - 1.8 VDD PWR SEQUENCING

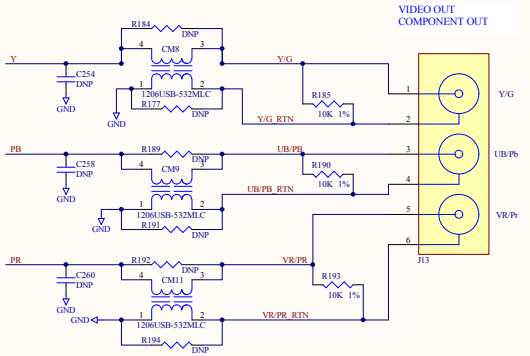
NOTE: MAY AS WELL SEQUENCE THE +1.8VPDD FROM THE DELAYED +1.8V_VENC RAIL W/ 1.8VDD, THO ONLY REQ'D



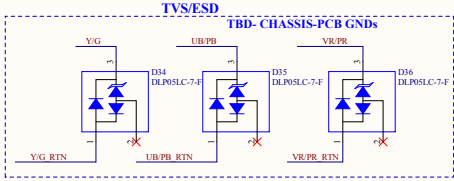




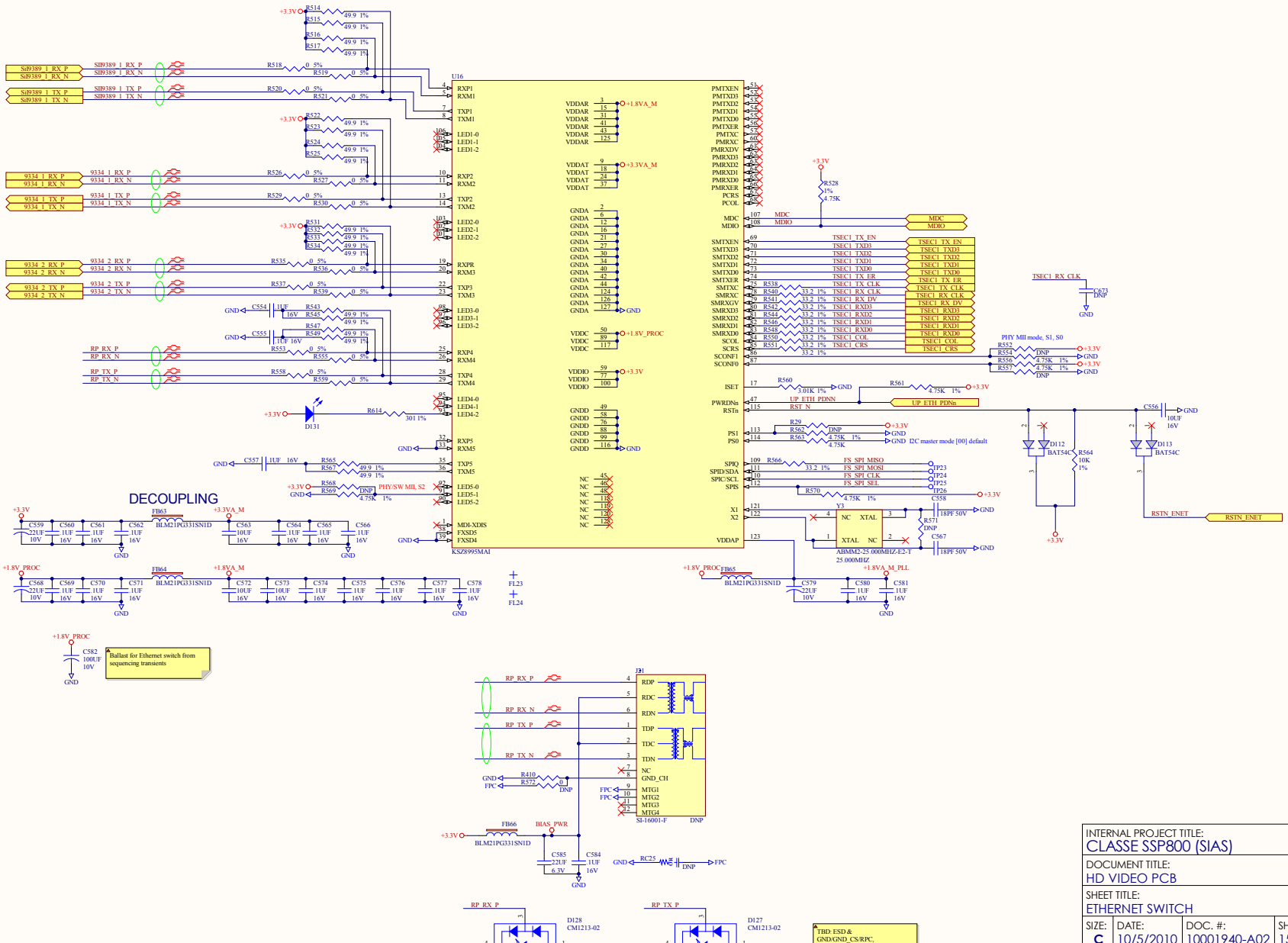
TBD esd &/or emi chassis-gnd-rtn connectivity per TBD connector shield/cover/facing



TVS/ESD



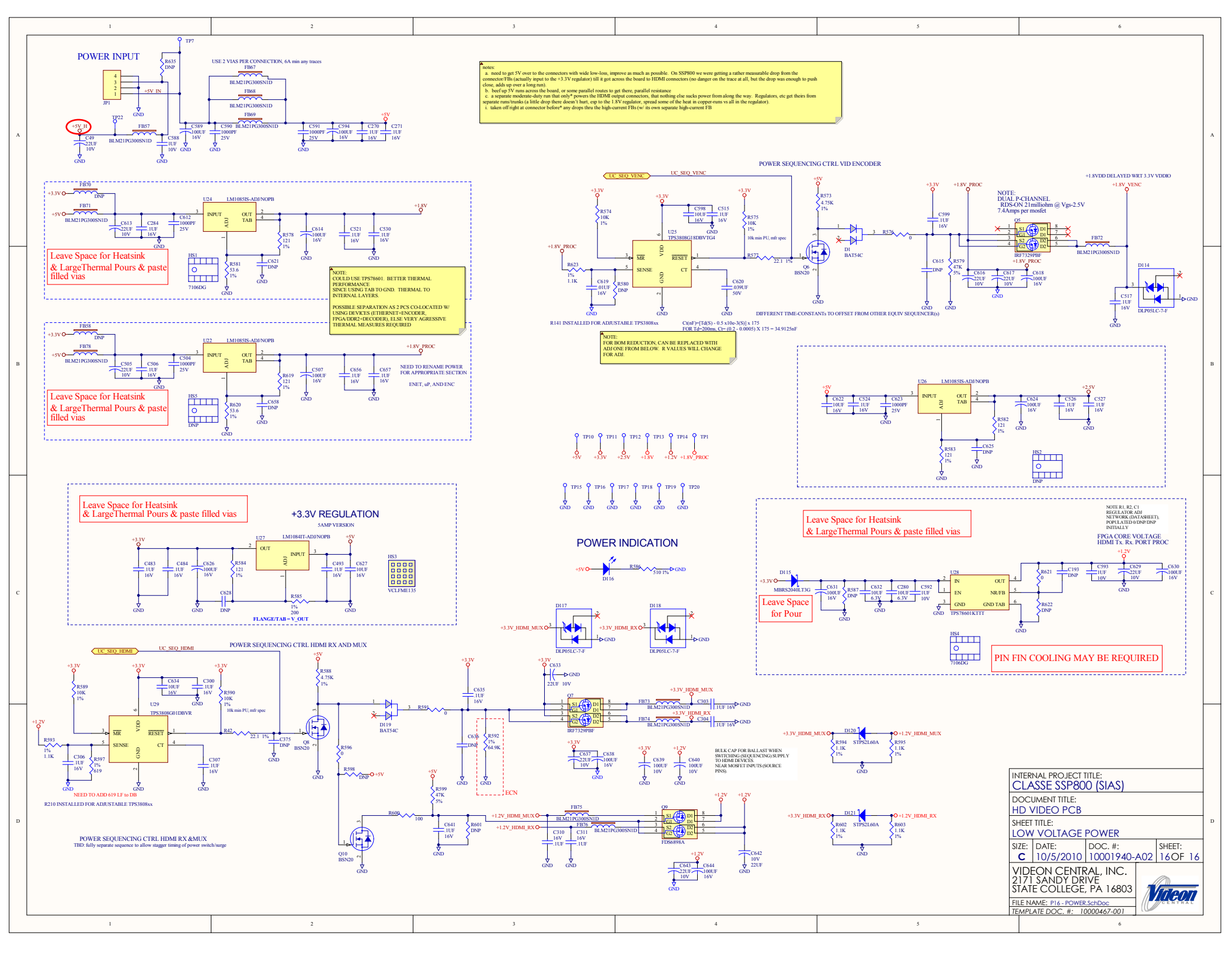
INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)			
DOCUMENT TITLE: HD VIDEO PCB			
SHEET TITLE: VIDEO ENCODER			
SIZE: C	DATE: 10/5/2010	DOC. #: 10001940-A02	SHEET: 14OF 16
VIDEON CENTRAL, INC. 2171 SANDY DRIVE STATE COLLEGE, PA 16803			
FILE NAME: P14 - VIDEO_DAC.Schdoc			
TEMPLATE DOC. #: 10000467-001			



INTERNAL PROJECT TITLE: CLASSE SSP800 (SIAS)			
DOCUMENT TITLE: HD VIDEO PCB			
SHEET TITLE: ETHERNET SWITCH			
SIZE: C	DATE: 10/5/2010	DOC. #: 10001940-A02	SHEET: 15OF 16

VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803

FILE NAME: P15-ETHERNET SWITCH.SchDoc
TEMPLATE DOC. #: 10000467-001


POWER INPUT
USE 2 VIAS PER CONNECTION, 6A min any traces
notes:
a. need to get 5V over to the connectors with wide low-loss, improve as much as possible. On SSP800 we were getting a rather measurable drop from the connector/FBs (actually input to the +3.3V regulator) till it got across the board to HDMI connectors (no danger on the trace at all, but the drop was enough to push close, adds up over a long run).
b. beef up 5V runs across the board, or some parallel routes to get there, parallel resistance
c. a separate moderate-duty run that only* powers the HDMI output connectors, that nothing else sucks power from along the way. Regulators, etc get theirs from separate runs/trunks (a little drop there doesn't hurt, esp to the 1.8V regulator, spread some of the heat in copper-runs vs all in the regulator).
i. taken off right at connector before* any drops thru the high-current FBs (w/ its own separate high-current FB
POWER SEQUENCING CTRL VID ENCODER
UC_SEQ_VENC
+1.8VDD DELAYED WRT 3.3V VDDIO
NOTE:
DUAL P-CHANNEL
RDS-ON 21milliohm @ Vgs-2.5V
7.4Amps per mosfet
Leave Space for Heatsink
& LargeThermal Pours & paste
filled vias
NOTE:
COULD USE TPS78601. BETTER THERMAL PERFORMANCE
SINCE USING TAB TO GND. THERMAL TO INTERNAL LAYERS.
POSSIBLE SEPARATION AS 2 PCS CO-LOCATED W/ USING DEVICES (ETHERNET+ENCODER, FPGA/DDR2+DECODER), ELSE VERY AGRESSIVE THERMAL MEASURES REQUIRED
R141 INSTALLED FOR ADJUSTABLE TPS3808xx
C(nF)=[Td(S) - 0.5 x10e-3(S)] x 175
FOR Td=200ms, Ct= (0.2 - 0.0005) X 175 = 34.9125nF
NOTE:
FOR BOM REDUCTION, CAN BE REPLACED WITH ADJ ONE FROM BELOW. R VALUES WILL CHANGE FOR ADJ.
DIFFERENT TIME-CONSTANTs TO OFFSET FROM OTHER EQUIV SEQUENCER(s)
NEED TO RENAME POWER FOR APPROPRIATE SECTION
ENET, uP, AND ENC
Leave Space for Heatsink
& LargeThermal Pours & paste filled vias
+3.3V REGULATION
5AMP VERSION
FLANGE/TAB = V_OUT
POWER INDICATION
Leave Space for Heatsink
& LargeThermal Pours & paste filled vias
NOTE R1, R2, C1
REGULATOR ADJ NETWORK (DATASHEET), POPULATED 0/DNP/DNP INITIALLY
FPGA CORE VOLTAGE
HDMI Tx. Rx. PORT PROC
Leave Space for Pour
PIN FIN COOLING MAY BE REQUIRED
POWER SEQUENCING CTRL HDMI RX AND MUX
UC_SEQ_HDMI
NEED TO ADD 619 LF to DB
R210 INSTALLED FOR ADJUSTABLE TPS3808xx
POWER SEQUENCING CTRL HDMI RX &MUX
TBD: fully separate sequence to allow stagger timing of power switch/surge
ECN
BULK CAP FOR BALLAST WHEN SWITCHING (SEQUENCING) SUPPLY TO HDMI DEVICES NEAR MOSFET INPUTS (SOURCE PINS).
INTERNAL PROJECT TITLE:
CLASSE SSP800 (SIAS)
DOCUMENT TITLE:
HD VIDEO PCB
SHEET TITLE:
LOW VOLTAGE POWER
SIZE: C
DATE: 10/5/2010
DOC. #: 10001940-A02
SHEET: 16OF 16
VIDEON CENTRAL, INC.
2171 SANDY DRIVE
STATE COLLEGE, PA 16803
FILE NAME: P16 - POWER.SchDoc
TEMPLATE DOC. #: 10000467-001