

A Appendix

A.1 JavaScript Well-formedness

$$\begin{aligned}
\text{range}_r(E : \text{event}) &\triangleq [E.\text{index} \dots E.\text{index} + |E.\text{reads}|) & \text{read}(E : \text{event}) &\triangleq (E.\text{reads} \neq []) \\
\text{range}_w(E : \text{event}) &\triangleq [E.\text{index} \dots E.\text{index} + |E.\text{writes}|) & \text{write}(E : \text{event}) &\triangleq (E.\text{writes} \neq []) \\
\text{range}(E : \text{event}) &\triangleq \text{range}_r(E) \cup \text{range}_w(E) & \text{rmw}(E : \text{event}) &\triangleq \text{read}(E) \wedge \text{write}(E) \\
\text{overlap}(E_1, E_2 : \text{event}) &\triangleq E_1.\text{block} = E_2.\text{block} \wedge & \text{read}(Es : \text{set event}) &\triangleq \{E \mid E \in Es \wedge \text{read}(E)\} \\
& \quad \text{range}(E_1) \cap \text{range}(E_2) \neq \emptyset & \text{write}(Es : \text{set event}) &\triangleq \{E \mid E \in Es \wedge \text{write}(E)\} \\
\\
\text{well-formed}(k : \text{nat}, E_w : \text{event}, E_r : \text{event}) &\triangleq \\
& \quad k \in \text{range}_w(E_w) \wedge k \in \text{range}_r(E_r) \wedge E_w.\text{block} = E_r.\text{block} \wedge \\
& \quad (E_w.\text{writes})!(k - E_w.\text{index}) = (E_r.\text{reads})!(k - E_r.\text{index}) \wedge E_w \neq E_r \\
\\
\text{well-formed}(\text{rbf} : \text{set}(\text{nat} \times \text{event} \times \text{event}), Es : \text{set event}) &\triangleq & \text{well-formed}(CE : \text{candidate_execution}) &\triangleq \\
& \quad (\forall E_r \in Es, k \in \text{range}_r(E_r). \exists! E_w. \langle k, E_w, E_r \rangle \in \text{rbf}) \wedge & CE.\text{total-order} &\text{is a strict total order on } CE.\text{evs} \wedge \\
& \quad (\forall E_r \in Es, k \notin \text{range}_r(E_r). \nexists E_w. \langle k, E_w, E_r \rangle \in \text{rbf}) \wedge & \text{well-formed}(CE.\text{reads-byte-from}, CE.\text{evs}) \\
& \quad \forall \langle k, E_w, E_r \rangle \in \text{rbf}. \text{well-formed}(k, E_w, E_r)
\end{aligned}$$

Figure 14. Candidate Execution Well-formedness

A.2 Comparison to Prose JavaScript Specification

The model as presented by the paper is intended to be a faithful rendering in logic of the model as it is described in the JavaScript specification. However, we sometimes factor or name definitions differently for the sake of a simpler presentation or to match standard terminology in the literature. Noticeable differences are highlighted here.

- The prose specification refers to written values as an event’s “payload”. Read events do not contain a payload field, but their read value is contained in a separate “chosen value record”. We simply make both of these fields part of the event as explicit read/write fields.
- The prose specification uses the term memory-order to refer to what we call total-order, but this invites confusion with the C/C++11 memory model: there a “memory order” is what JavaScript calls a “consistency mode”, and “mo” refers to “modification order”, a per-location-total order on writes [9].
- In addition, the prose specification existentially quantifies **tot** as part of its validity conditions. We make this a field of the candidate execution.
- The prose specification does not make a distinction between well-formedness conditions (which are purely invariants of the thread-local semantics), and validity conditions, which are semantic conditions imposed by the axiomatic memory model. We separate well-formedness from validity in our rendering of the model because in later sections we explicitly want to reason about executions which are well-formed but nevertheless not valid.
- In the prose specification our Happens-Before Consistency (2-3) conditions are collectively named the “Coherent Reads” condition.
- In several cases, the prose specification defines predicates using a pseudocode algorithm. For example, the prose specification’s “Coherent Reads” condition is defined as an explicit iteration over the set of events, accumulating a boolean result, instead of as a more abstract universal quantification. Our Happens-Before Consistency (1) condition is instead given as a component of Sequentially Consistent Atomics.
- The prose specification describes an additional condition that all atomic writes must have a finite prefix in total-order. This condition is vacuously true in real candidate executions, since total-order must be well-founded (every thread must have a first event in sequenced-before-order). This condition is occasionally included in formal relaxed memory models as a well-formedness condition that is implied by the thread-local semantics [9]. However, we never need to use it, so we simply elide it here.

A.3 Comparison to Alloy/Coq models

As previously detailed, our proofs assume that all initialization happens “before time”. The Coq model undergoes two minor refactorings in order to better interface with the existing IMM models. First, validity conditions have individual edges reversed so that they can be expressed as equivalent acyclicity constraints. Second, RMW events are equivalently represented as two events which are always adjacent in **sb** and **tot**. Both of these transformations are analogous to the transformations made to other models (such as C/C++11) in previous works in order to simplify formal proofs [28, 35]

B ARMv8 model

<i>mode</i>	::=	ReadAcquire ReadWeakAcquire WriteRelease DMB.SY DMB.LD DMB.ST ISB
<i>addr</i>	::=	$\alpha \dots$ an infinite set of abstract names
<i>event</i>	::=	{ ord : <i>mode</i> index : <i>nat</i> reads : <i>list byte</i> writes : <i>list byte</i>
<i>candidate_execution</i>	::=	{ evs : <i>set event</i> IW : <i>event</i> program-order // po : <i>set (nat × event × event)</i> reads-byte-from // rbf : <i>set (nat × event × event)</i> bitwise-coherence // cob : <i>set (nat × event × event)</i> address-dependency-pre // addrP : <i>set (event × event)</i> data-dependency-pre // dataP : <i>set (event × event)</i> control-dependency-pre // ctrlP : <i>set (event × event)</i> read-modify-write // rmw : <i>set (event × event)</i> }

Following herd [6], we define relational composition “;” the identity relation “[A]” on a set A :

$$R; S \triangleq \{ \langle A, B \rangle \mid \exists C. \langle A, C \rangle \in R \wedge \langle C, B \rangle \in S \}$$

$$[E] \triangleq \{ \langle E, E \rangle \mid E \in A \}$$

Then, $[A]; R; [B]$ is the relation R restricted to elements from A on the left and elements from B from the right:

$$[A]; R; [B] = \{ \langle a, b \rangle \mid \langle a, b \rangle \in R \wedge a \in A \wedge b \in B \}$$

Derived auxiliary relations (with respect to a candidate execution)

same-thread // sthd	$\triangleq \{ \langle A, B \rangle \mid \langle A, B \rangle \in \mathbf{po} \vee \langle B, A \rangle \in \mathbf{po} \}$
reads-from // rf	$\triangleq \{ \langle A, B \rangle \mid \exists k. \langle k, A, B \rangle \in \text{reads-byte-from} \}$
coherence // co	$\triangleq \{ \langle A, B \rangle \mid \exists k. \langle k, A, B \rangle \in \text{bitwise-coherence} \}^+$
reads-from-internal // rfi	$\triangleq \text{reads-from} \cap \text{same-thread}$
reads-from-external // rfe	$\triangleq \text{reads-from} \setminus \text{reads-from-internal}$
coherence-internal // coi	$\triangleq \text{coherence} \cap \text{same-thread}$
coherence-external // coe	$\triangleq \text{coherence} \setminus \text{coherence-internal}$
bitwise-from-reads // frb	$\triangleq \{ \langle k, A, B \rangle \mid \exists C. \langle k, C, A \rangle \in \text{reads-byte-from} \wedge \langle k, C, B \rangle \in \text{bitwise-coherence} \}^+$
from-reads // fr	$\triangleq \{ \langle A, B \rangle \mid \exists k. \langle k, A, B \rangle \in \text{bitwise-from-reads} \}^+$
from-reads-internal // fri	$\triangleq \text{from-reads} \cap \text{same-thread}$
from-reads-external // fre	$\triangleq \text{from-reads} \setminus \text{from-reads-internal}$
program-order-same-byte-location // polocb	$\triangleq \{ \langle k, A, B \rangle \mid \langle A, B \rangle \in \mathbf{po} \wedge k \in \text{range}(A) \wedge k \in \text{range}(B) \}$

$$\begin{aligned}
R &\triangleq \{E \mid E.\text{reads} \neq []\} \\
W &\triangleq \{E \mid E.\text{writes} \neq []\} \\
A &\triangleq \{E \mid E.\text{ord} = \mathbf{ReadAcquire}\} \\
Q &\triangleq \{E \mid E.\text{ord} = \mathbf{ReadWeakAcquire}\} \\
L &\triangleq \{E \mid E.\text{ord} = \mathbf{WriteRelease}\} \\
\text{DMB.SY} &\triangleq \{E \mid E.\text{ord} = \mathbf{DMB.SY}\} \\
\text{DMB.LD} &\triangleq \{E \mid E.\text{ord} = \mathbf{DMB.LD}\} \\
\text{DMB.ST} &\triangleq \{E \mid E.\text{ord} = \mathbf{DMB.ST}\} \\
\text{ISB} &\triangleq \{E \mid E.\text{ord} = \mathbf{ISB}\} \\
B &\triangleq \text{DMB.SY} \cup \text{DMB.LD} \cup \text{DMB.ST} \cup \text{ISB}
\end{aligned}$$

address-dependency // **addr** $\triangleq [R]; \mathbf{addrP}$

data-dependency // **data** $\triangleq [R]; \mathbf{dataP}$

control-dependency // **ctrl** $\triangleq [R]; \mathbf{ctrlP}$

coherence-after // **ca** $\triangleq \mathbf{co} \cup \mathbf{fr}$

observed // **obs** $\triangleq \mathbf{rfe} \cup \mathbf{fre} \cup \mathbf{coe}$

dependency-ordered-before // **dob** $\triangleq \mathbf{addr} \cup$
 $\mathbf{data} \cup$
 $(\mathbf{ctrl}; [W]) \cup$
 $((\mathbf{ctrl} \cup \mathbf{addr}; \mathbf{po}); [\text{ISB}]; \mathbf{po}; [R]) \cup$
 $(\mathbf{addr}; \mathbf{po}; [W]) \cup$
 $((\mathbf{ctrl} \cup \mathbf{data}); \mathbf{coi}) \cup$
 $((\mathbf{addr} \cup \mathbf{data}); \mathbf{rfi})$

atomic-ordered-before // **aob** $\triangleq \mathbf{rmw} \cup (\mathbf{rmw}; [R]; \mathbf{rfi}; [A \cup Q])$

barrier-ordered-before // **bob** $\triangleq \mathbf{po}; [\text{DMB.SY}]; \mathbf{po} \cup$
 $([L]; \mathbf{po}; [A]) \cup$
 $([R]; \mathbf{po}; [\text{DMB.LD}]; \mathbf{po}) \cup$
 $([A \cup Q]; \mathbf{po}) \cup$
 $([W]; \mathbf{po}; [\text{DMB.ST}]; \mathbf{po}; [W]) \cup$
 $(\mathbf{po}; [L]) \cup$
 $(\mathbf{po}; [L]; \mathbf{coi}) \cup$

initial-ordered-before // **iob** $\triangleq \{(IW, E) \mid E \in \text{EV} \setminus IW\}$

ordered-before // **ob** $\triangleq \mathbf{obs} \cup \mathbf{dob} \cup \mathbf{aob} \cup \mathbf{bob}$

Well-formedness conditions

Let R_k , for some relation $R : \text{set}(\text{nat} \times \text{event} \times \text{event})$, denote the relation $\{\langle A, B \rangle \mid \langle k, A, B \rangle \in R\} : \text{set}(\text{event} \times \text{event})$.

- The initial write is not a release write:

$$IW \subseteq W \setminus L$$

- In our fragment, reads and writes are disjoint, and reads, writes, and barriers are disjoint:

$$R \cap W \cap \text{DMB.SY} \cap \text{DMB.LD} \cap \text{DMBST} \cap \text{ISB} = \emptyset$$

- Barriers don't read or write memory:

$$\{\text{range}(E) \mid E \in B\} = \emptyset$$

- For all locations k , cob_k is a strict total order on $\{W \mid k \in W.\text{writes}\} \dots$
- \dots and only includes writes that write to k :

$$\forall k, W, W'. \langle W, W' \rangle \in \text{cob}_k \implies k \in W.\text{writes} \cap W'.\text{writes}$$

- coherence is a strict partial order.
- read-modify-write, address-dependency, data-dependency, and control-dependency are subsets of program-order:

$$\text{rmw} \cup \text{addr} \cup \text{data} \cup \text{ctrl} \subseteq \text{po}$$

Candidate execution validity**Single-copy atomicity**

(**rf**; **fr**) irreflexive

Coherence/internal

$\forall k. (\text{polocb}_k \cup \text{frb}_k \cup \text{cob}_k \cup \text{rbf}_k)$ acyclic

External

ob acyclic

Exclusives/Atomic

$\text{rmw} \cap (\text{fre}; \text{coe}) = \emptyset$