Single Device Neuron

Schematics

The neuron schematic is shown in Figure 1. The output signal is the current going through D1. The operation principle is described as following.

The memristor is positions in such a way that when current go from node 4 to node 3, its resistance increases, and vice versa. Since Vdd drives current go through r3 and memristor-r2, memristor is in a high resistance state when there is no signal input. Even the memristor changes to a relatively low resistance state, the current will drive the memristor back to high resistance state gradually. This process resembles the charge leakage of a neuron.

The neuron can behave in two ways when there is an input. If the input is high enough to break D2 down, current through memristor will flow from node 3 to node 4, reducing the resistance of memristor. This input will be considered as excitatory. If the input is small and D2 is not broken, current through the memristor will go from node 4 to node 3, increasing the resistance of the memristor. Such input will be considered inhibitory. An input type can also be predefined by replacing D2 with a resistor (rd). If rd let current go from 3 to 4, it is an excitatory input. Otherwise it is inhibitory.

When the memristor is in a high resistance state the D1 is not broken down and the current going through D1 is low. A neuron in such a state is considered in rest state. If the resistance of memristor is low enough and D1 is broken down, the current going through D1 will be high and the neuron is firing.

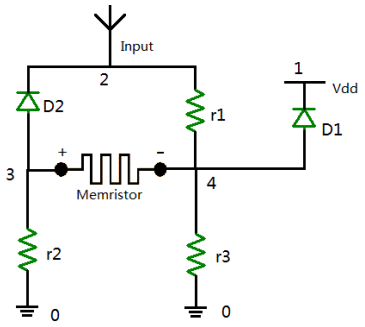

Figure 1 Neuron Schematic

In short, the whole circuit is operating as shown in Figure 2. When the resistance of PMem is high (between a and b), the circuit is open and only show low current. When the resistance of PMen is low (at c) the circuit is shorted and the current high.

The characteristics of resistors and diodes in Figure 1 must be set carefully. Rules like r3 should not break down D1, r2 mustn't break down D2 must be followed. Value of r2 should also be small enough to be able to break D1 down. But such rules are not explored in detail yet. Some odd behavior appears during simulation. And it may take me some time to figure those problems out.

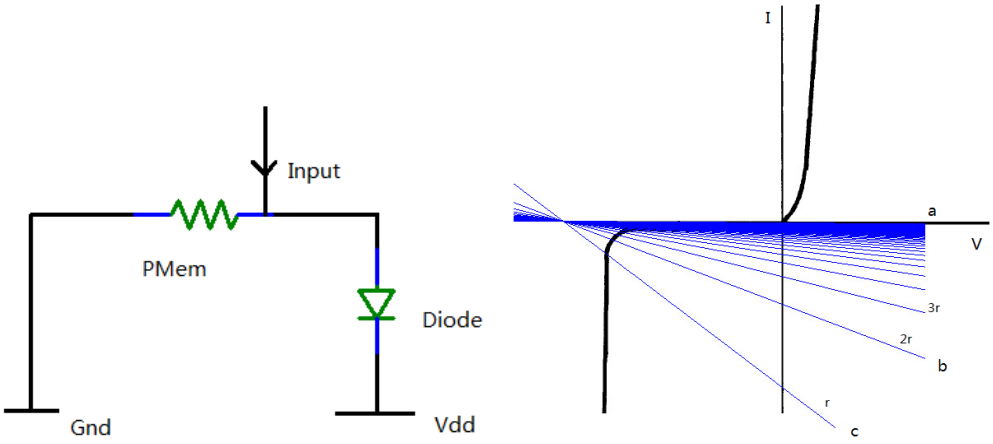

Figure 2 Operation Principle

Simulation Result

This scheme is simulated with PSPICE. The circuit is attached in Appendix. The memristor model used here comes from [1]. This simulation only aims to show the potential of the circuit of actin as an integral-fire neuron. Those parameters are not carefully tuned to be practical, i.e. 30V supply were used. But at least this circuit can operate at 5V.

Firstly, at rest state, the output current, i.e. current going through D1, is very small as shown in Figure 3.

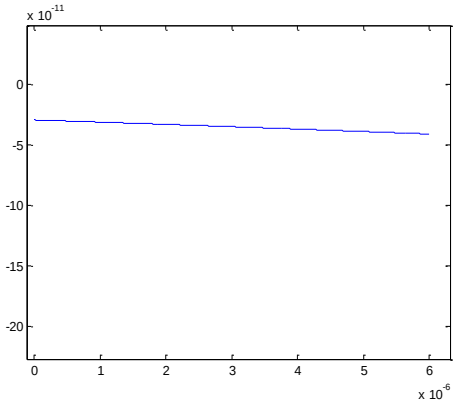

Figure 3 resting state

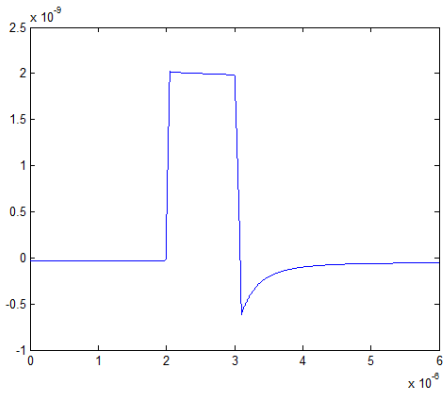

Figure 4 small input response

When the input is small, there is no noticeable output. Figure 4 shows the neuron response of a small input. The square shape is the effect of input, which is small and disappears as the input disappears. The firing-like response is the negative spike follows the square shape. This response is of a magnitude of 10^{-9} which is negligible. With an input above threshold, a spike will be given by the neuron. As shown in Figure 5. The positive spike indicates the beginning of the input signal, which is one of the issue that confuses

[1] Memristive Device Fundamentals and Modeling: Applications to Circuits and Systems Simulation (Eshraghian, K.; Kavehei, O.; Kyoung-Rok Cho; Chappell, J.M.; Iqbal, A.; Al-Sarawi, S.F.; Abbott, D., "Memristive Device Fundamentals and Modeling: Applications to Circuits and Systems Simulation," Proceedings of the IEEE , vol.100, no.6, pp.1991,2007, June 2012)

me. The negative spike is the wanted neuron spike. It is at the scale of 10^{-5}, 10k larger than the small input response. It is also worth noting that the neuron goes back to resting state after spiking.

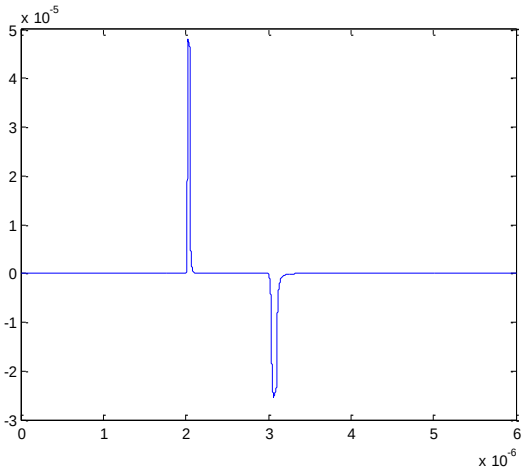

Figure 5 Firing activity of the neuron

To illustrate the winner-take-all property of this neuron, Figure 6 is plotted. Since in a simplified perspective, a memristor can be taken as a resistor whose resistance depends on the charge passes through it, this neuron fires when the charge passes it in positive direction reaches a threshold. Figure 6 plots the firing amplitude w.r.t the charge that passes through the memristor from positive direction. The spike amplitude increases drastically after the charge reaches 11 units. And the firing threshold is around 13 units.

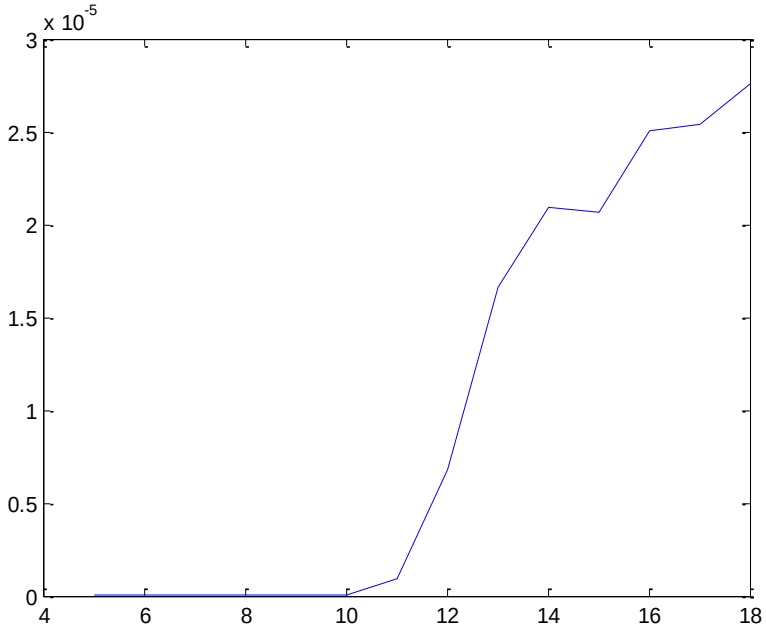

Figure 6 spike amplitude v.s. input charge

Since we use diodes to generate non-linearity of the neuron, the steepness of the firing amplitude depends on the non-linearity of the diode. And since the diode does not saturate after break down, the

firing amplitude also don't saturate, but increase linearly with a small increasing rate. Since our input signal is bonded, such behavior is not considered an issue. Though such problem can be solved by replace D1 with other non-linear devices.

Last but not least, we have to show that the firing amplitude depends on the aggregated charge from the positive direction instead of the input amplitude. The input amplitude in Figure 7 is 11V. If this input last for 1us, the charge passes through the memristor is 11 units. According to Figure 6, the response amplitude should be several micro-volts and is below threshold. But with a longer input duration, enough charge has been aggregated and the neuron fires as normal.

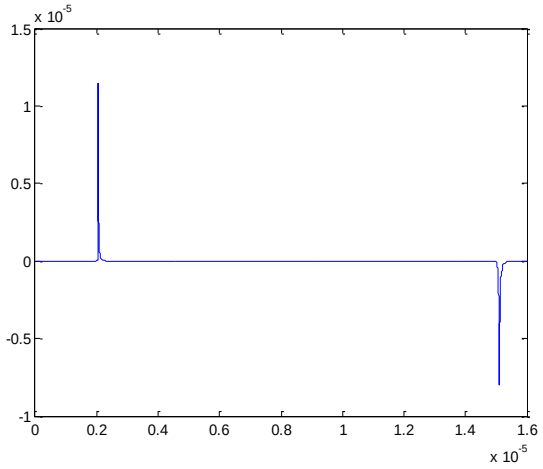

Figure 7 Response of a long lasting small input

Summary

This small report roughly introduces a possible way to build a single-device neuron. With simulation data, it is shown that such design has all the properties of an integral-and-firing neuron. Firstly, it has a steady resting state and goes back to resting state after spiking. Secondly, the neuron integrals the charge passes through the memristor from the positive direction and fires when the integrated charge reaches a threshold. The winner-takes-all behavior of this neuron is also well illustrated with data.

In short, though lots of issues like spike shape, firing frequency etc. are not addressed yet. It is quite clear that this neuron has all the major properties of a real neuron.

Severe Issues

1. The large spike before each input signal cannot be explained. It looks like to be caused by the capacitor in the model which is not present in actual device. Hence I think it is an problem of the model. But more work needs to be done on identifying this.

2. In Figure 34 it is clear that the current going through D1 becomes positive. But the voltage across D1 never go positive. This is really wired phenomenon.

It is not clear whether those 2 issues are simulation problems or some unknown property of memristor. But either is a severe problem that threats the validity of this model and the design principle.

Appendix

SPICE model

```
firing

.SUBCKT memristor Pos Neg
* Parameters:
.PARAM n=4 a1=9 a2=0.01 b1=2 b2=4 l=10N
.PARAM wmin=0.05 wmax=0.95 p0=1.2 fon=40E-3 foff=40E-3
* Shape factor, sf, can be a function of tunneling barrier width (normalized state variable)
.PARAM sfo=4  sfm=20  p=5
*** sf(w)=sfo+sfm(1-(2w-1)**2p)
*State variable:
Gvon 0 w value = {signm(wmax-V(w))*signm(V(Pos,Neg))*gon(V(Pos,Neg),sf(V(w)),p0)}
Gvoff 0 w value = {signm(V(w)-wmin)*signm(V(Neg,Pos))*goff(V(Pos,Neg),sf(V(w)),p0)}
* Initiai (internal) state:
.IC V(w) = 0.05
*Integration:
Cw w 0 8e-5
Rw w 0 0.01T
*Current equation:
Gmem Pos Neg value = {l*((V(w)**n)*a1*sinh(b1*V(Pos,Neg))+a2*(exp(b2*V(Pos,Neg))-1))}
* Series resistor, Rs, can be implemented here, between two Neg1 and Neg2 nodes.
* Functjons:
.func signm(v) = {(sgn(v)+1)/2}
.func gon(v1,v2,v3) = {fon*((1-v1/(2*v3))*exp(v2*v3*(1-sqrt((1-v1/(2*v3))))))}
.func goff(v1,v2,v3) = {foff*(-((1+v1/(2*v3))*exp(v2*v3*(1-sqrt((1+v1/(2*v3))))))))}
.func sf(v1) = {sfo+sfm*(1-(2*(v1)-1)**2p)}
.ENDS

.model Dfire D (IS=0.1PA RS=16 CJO=2pF TT=12N BV=30 IBV=0.1PA)
.model Dblock D (IS=0.1PA RS=16 CJO=2pF TT=12N BV=15 IBV=0.1PA)
.model Dshut D (IS=0.1PA RS=16 CJO=2pF TT=12N BV=100 IBV=0)

vdd 1 0 dc 32
d1 6 1 Dfire
x1  5 4 memristor
vm 3 5 dc 0
vm2 6 4 dc 0
```

```
vin 2 0 pwl(0 5 1.99u 5 2.05u 7 3u 7 3.1u 5)
*3u-2.05 is the signal duration and two 7s are the signal strangth
r1 2 4 1000meg
r2 3 0 1000k
r3 4 0 1000meg
d2 3 2 Dblock

.tran 0.0001us 6us
*.PRINT tran I(vin) I(r1) I(r2) I(r3) I(d2)
.PRINT tran I(d2) I(vm) I(vdd) v(4, 1) v(5, 4)
.END
```