

UNIVERSITY OF BOLOGNA

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MATRICULATION : 0001101279

COURSE NAME : SENSOR SYSTEM LAB

PROJECT NAME : LOW VOLTAGE OP-AMP

Specifications

<i>VDD</i>	2 V
Slew Rate	$\pm 10 \text{ V/us}$
Load Capacitor <i>CL</i>	10 pF
Max Vin Common Mode	2.5 V
Min Vin Common Mode	1 V
Max Vout	1.75 V
Min Vout	0.5 V
Gain Bandwidth	10 MHz
Phase Margin (PM)	60°
KT	4.11e-21
<i>Vtn / Vtp</i>	0.71 / -0.7
$\beta n` / \beta$	110e-6 / 50e-6
$\lambda n/\lambda p$	0.04/ 0.05

Objective

The design addresses challenges that typically arise in op-amps when power supply voltages approach 2VT. The op-amp's lower voltage limit is primarily constrained by the desired input common-mode range. Conventional op-amp design techniques can still be applied for supply voltages down to 2VT, but require careful consideration.

The op-amp structure includes:

1. An input stage using an n-channel differential amplifier (M1, M2) with current-source loads (M3, M4).
2. A folded cascode arrangement (M6, M7) that redirects the differential output currents.
3. An n-channel current mirror (M8, M9) for single-ended signal conversion.
4. A Miller-compensated class-A output stage for improved second-stage gain.

This design maintains performance comparable to standard two-stage op-amps while operating at lower supply voltages. It offers an advantage over classical two-stage designs by providing balanced loads for the input differential stage.

The next step would involve calculating the dimensions (length and width) for all transistors in the circuit to optimize performance within the low-voltage constraints.

Circuit Design

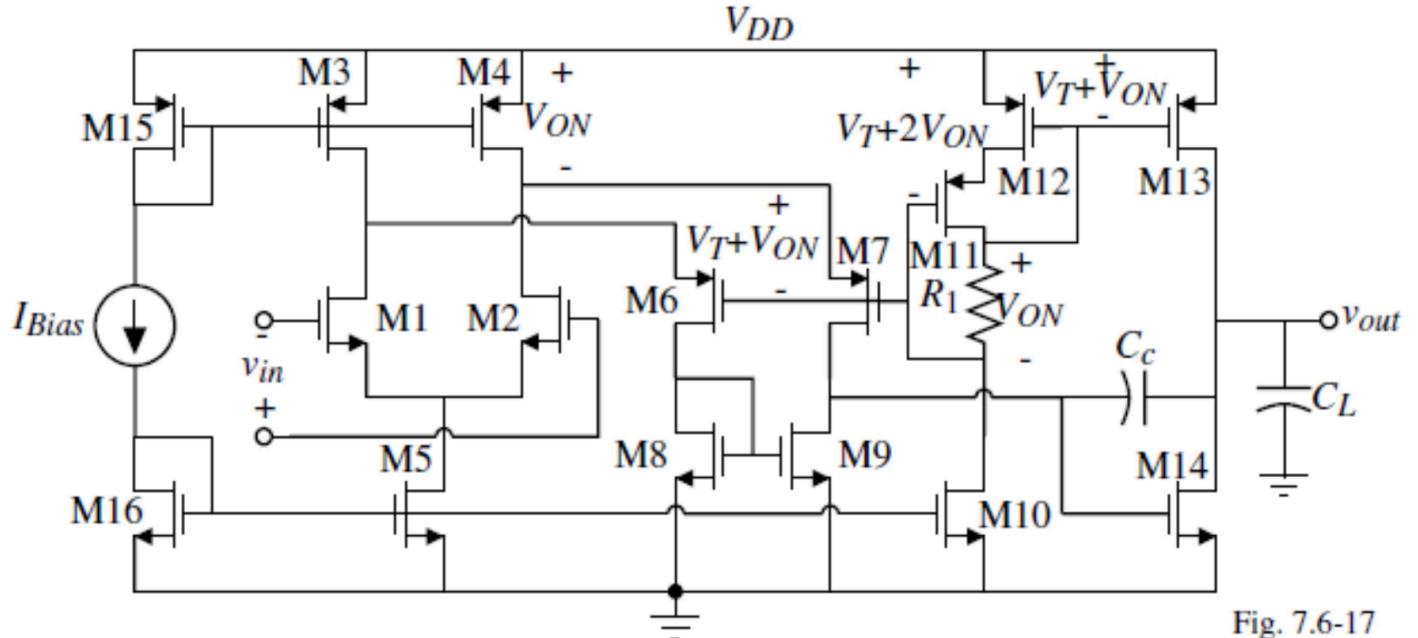


Fig. 7.6-17

Design Procedure for calculation of the Form Factor:

Let's take the length of each transistor to be 1um and use the following procedures to compute the form factors (S). After obtaining the S parameter, we will compute the transistor widths for each one.

Step 1

From $CL=10pF$, the miller capacitance is given as $CC = 2pF$. Since the slew rate is determined using M5 and is linked directly to the current I_5 , therefore the transconductance from GB and C_C is given as

$$I_5 = 20\mu A ; gm1 = gm2 = 125.67 \mu S$$

Step 2

Transistors M1 and M2's W/L ratios are computed using

$$S_1 = S_2 = gm_{12}/(2K_N I_{12}) = 7.18$$

Step 3

The input common mode voltage may be used to compute the design of M3 and M4 as shown.

$$V_{inmax} = V_{DD} - V_{SD3\ sat} + V_{sat} = 2.5V$$

$$S_{3,4} \geq 2 \times 30 / (0.25e2 \times 50) = 19.2$$

Step 4

Taking the assumption that $I_{10} = I_5 = 20\mu A$ yields $W_{10}L_{10} = 44$. The formula for R_1 is $0.25V/20\mu A = 12.5\text{Kohm}$. The W/L ratios for M11 and M12 may be written as

$$R_1 = 12.5 \text{ K}\Omega$$

$$S_{11,12} = (2I)/(K_N D_I (V_{SD8\ sat})e2) = (20 \times 2)/(50 \times (0.25)(0.25))$$

Step 5

M6 and M7 have the same VGS voltages and currents as M11 and M12, and their W/L values are likewise identical. Consequently,

$$S_{6,7} = 12.79$$

Step 6

M8 and M9 should be as tiny as feasible in order to decrease the parasitic pole. Conversely, the voltage drop across M6, M8, and M4 need to be smaller than that of the power source. Consequently,

$$S_{8,9} = (20 \times 20)/(110.08) = 1$$

Step 7

Ultimately, the second stage's W/L ratios need to be created either by utilizing the 60° phase margin relationship ($gm_{14} = 10gm_1 = 1256.7 \mu S$) or by taking into account the correct mirroring between M9 and M14 by merging the saturation region and W/L ratio formula.

$$S_{14} = (gm_1)/(K_N V_{DSSat}) = 22.85$$

Step 8

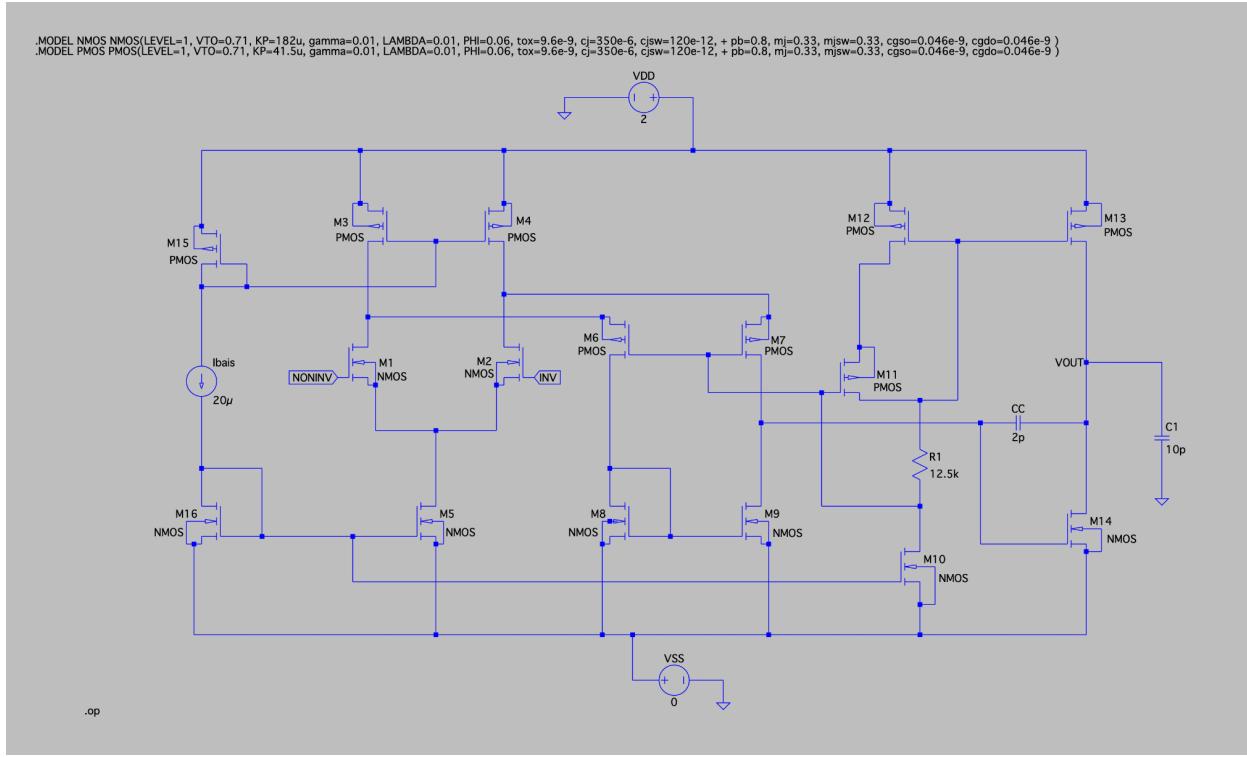
The required current ratio between the two transistors determines the design of the W/L of M13, and it is provided by

$$S_{13} = 201 \text{ um}$$

W_1	W_2	W_3	W_4	W_5	W_6	W_7	W_8	W_9	W_{10}	W_{11}	W_{12}	W_{13}	W_{14}	W_{15}	W_{16}
7.18	7.18	19.2	19.2	44.0	12.8	12.8	1.00	1.00	44.0	12.8	12.8	201	22.8	19.2	44.0

All the Widths are in (um) and L = 1um for all the transistors.

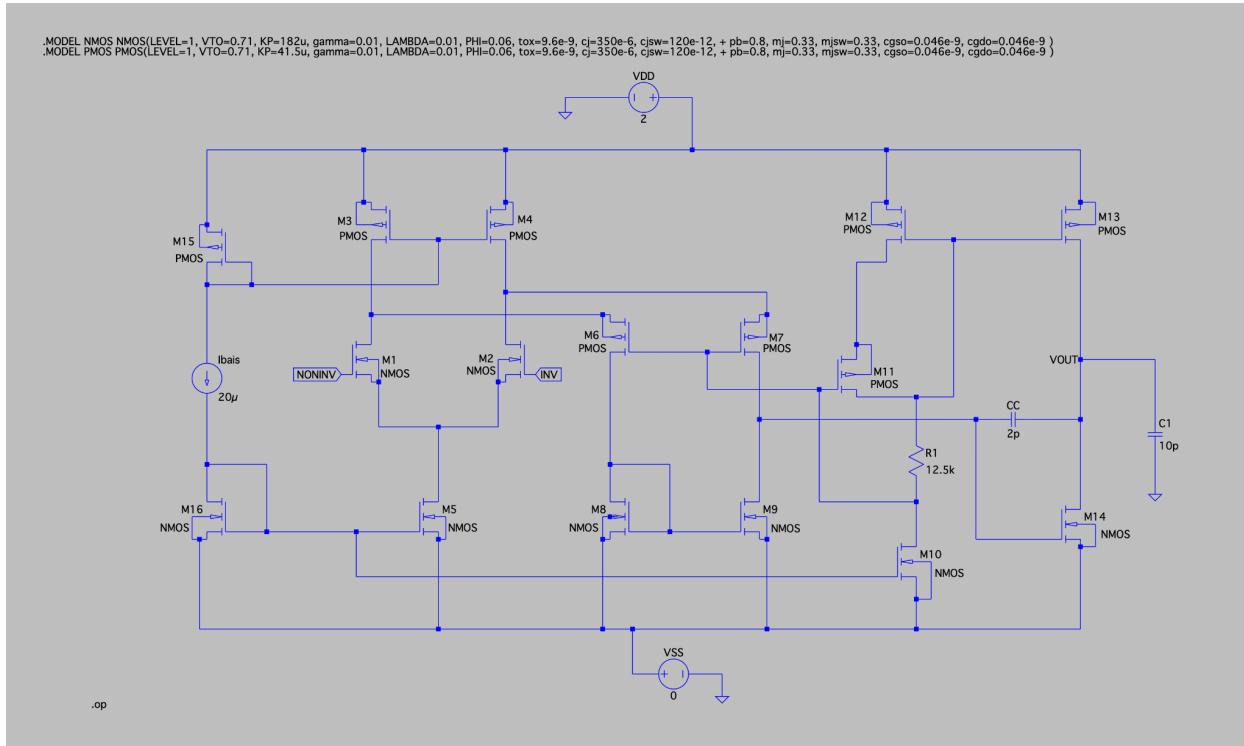
Schematic



Simulation

Let's now discuss the analysis of the low voltage op-amp simulation findings.

Operating Point Analysis

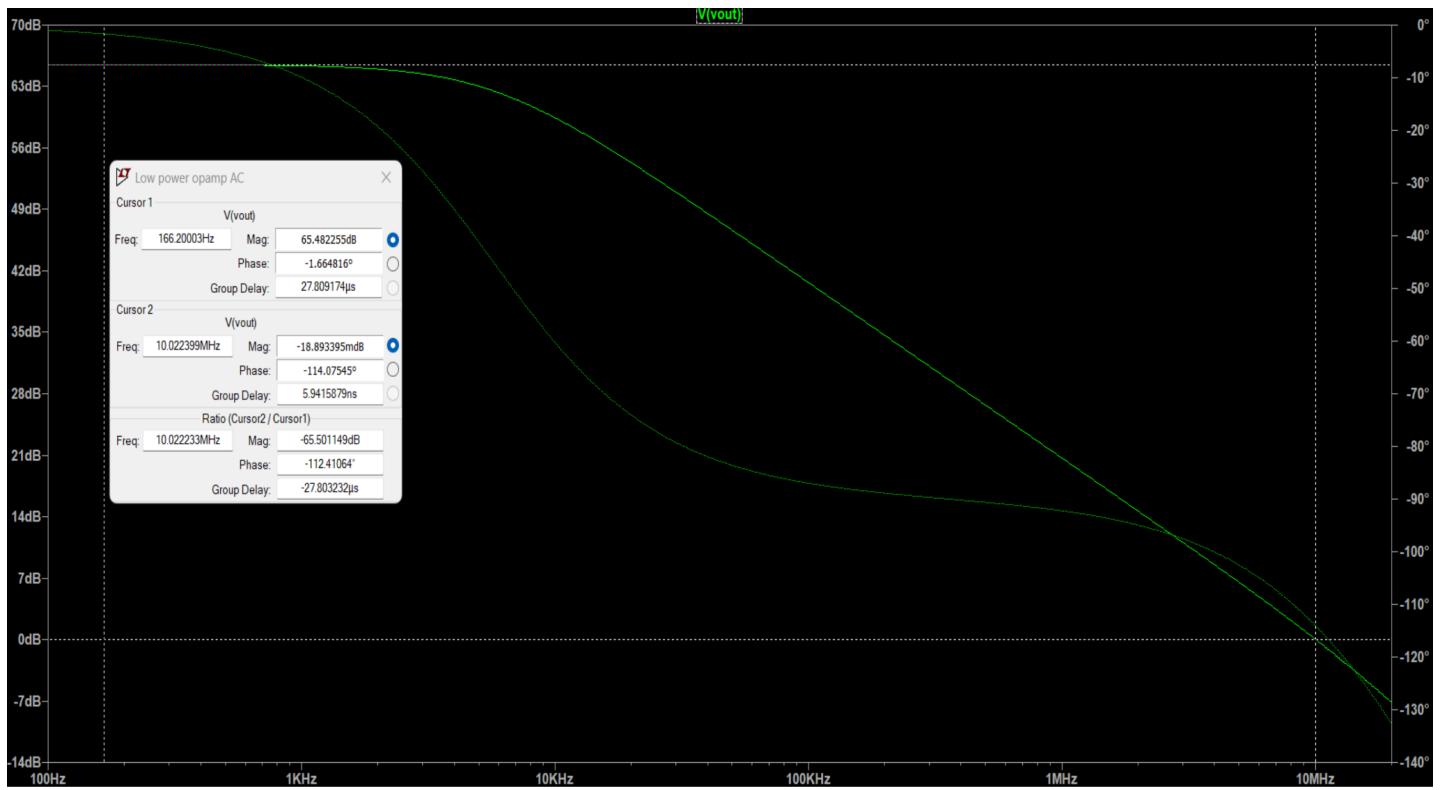
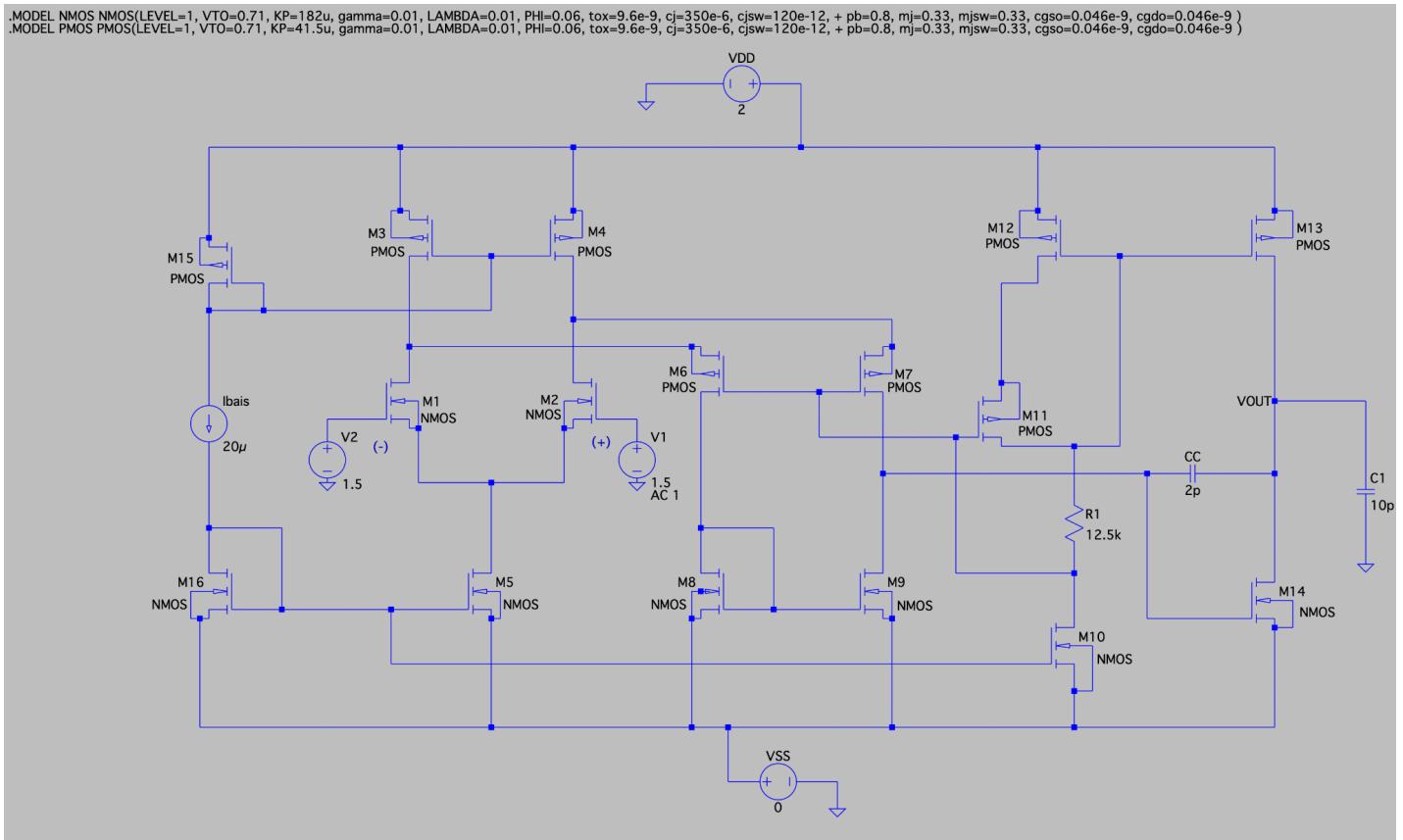


--- MOSFET Transistors ---					
Name:	m15	m4	m3	m12	m13
Model:	pmos	pmos	pmos	pmos	pmos
Id:	2.00e-05	8.08e-05	1.01e-04	2.02e-05	2.24e-03
Vgs:	0.00e+00	1.12e-01	1.53e-01	-3.31e-02	4.06e-01
Vds:	3.32e-02	1.45e-01	1.86e-01	4.24e-02	4.82e-01
Vbs:	3.32e-02	1.45e-01	1.86e-01	4.24e-02	4.82e-01
Vth:	7.10e-01	7.10e-01	7.10e-01	7.10e-01	7.10e-01
Vdsat:	-7.43e-01	-7.43e-01	-7.43e-01	-7.85e-01	-7.85e-01
Gm:	2.75e-05	1.21e-04	1.55e-04	2.64e-05	4.12e-03
Gds:	5.90e-04	4.98e-04	4.64e-04	4.63e-04	2.62e-03
Gmb:	5.62e-07	2.46e-06	3.17e-06	5.39e-07	8.41e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	9.20e-16	9.20e-16	9.20e-16	6.90e-16	9.43e-15
Cgdov:	9.20e-16	9.20e-16	9.20e-16	6.90e-16	9.43e-15
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	7.19e-14	7.19e-14	7.19e-14	5.40e-14	7.37e-13

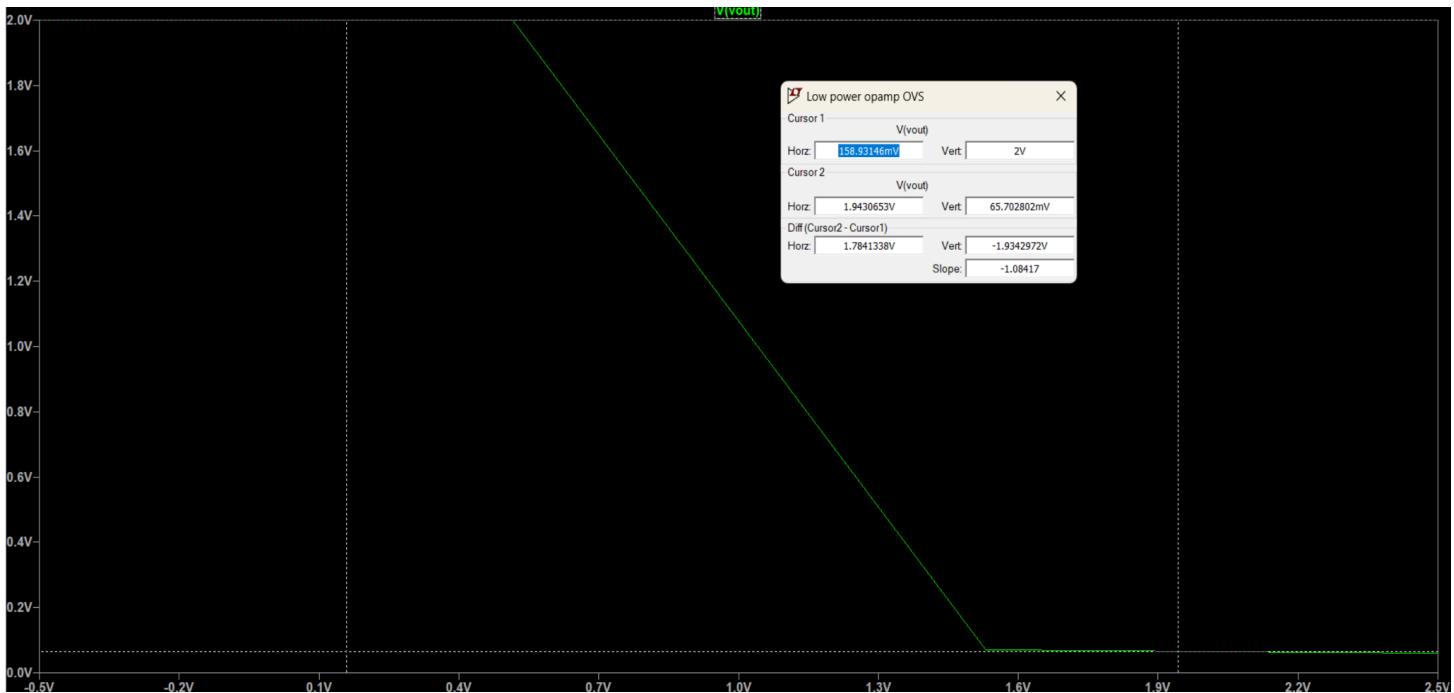
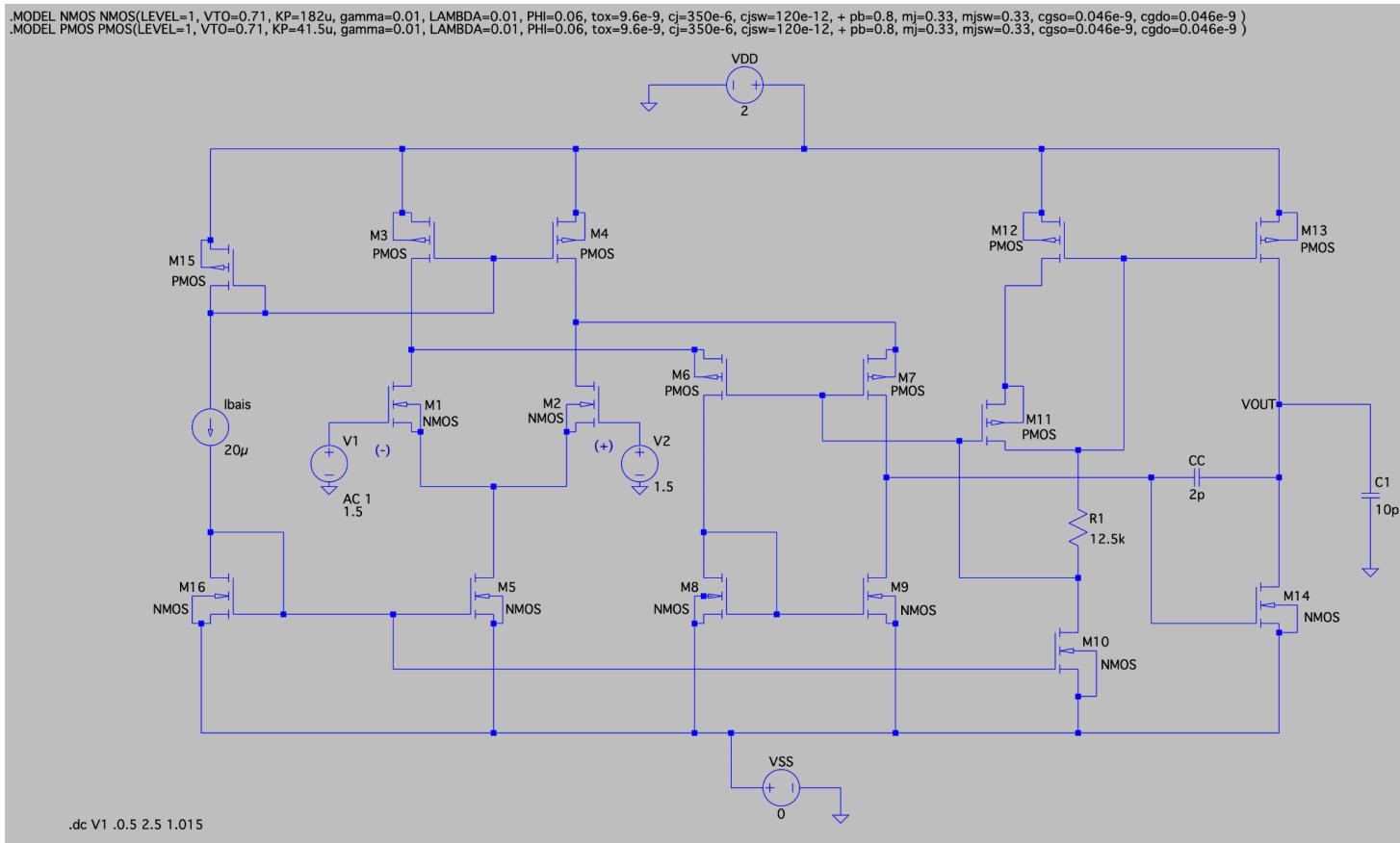
Name:	m6	m7	m11	m16	m1
Model:	pmos	pmos	pmos	nmos	nmos
Id:	8.08e-05	8.08e-05	2.02e-05	2.02e-05	2.11e-04
Vgs:	2.78e-02	-2.33e-02	-2.52e-01	7.80e-01	7.10e-01
Vds:	1.69e-01	1.59e-01	3.31e-02	7.80e-01	1.01e+00
Vbs:	1.69e-01	1.59e-01	3.31e-02	0.00e+00	0.00e+00
Vth:	7.10e-01	7.10e-01	7.10e-01	7.10e-01	7.10e-01
Vdsat:	-8.51e-01	-8.93e-01	-9.95e-01	6.96e-02	4.79e-04
Gm:	1.05e-04	9.94e-05	2.06e-05	5.75e-04	8.81e-01
Gds:	4.26e-04	4.58e-04	5.99e-04	1.98e-07	2.09e-06
Gmb:	2.15e-06	2.03e-06	4.21e-07	1.17e-05	1.80e-02
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	6.90e-16	6.90e-16	6.90e-16	2.07e-15	4.60e-10
Cgdov:	6.90e-16	6.90e-16	6.90e-16	2.07e-15	4.60e-10
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	1.08e-13
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	5.40e-14	5.40e-14	5.40e-14	0.00e+00	0.00e+00

Name:	m2	m5	m8	m9	m10
Model:	nmos	nmos	nmos	nmos	nmos
Id:	2.10e-12	2.00e-05	8.08e-05	8.08e-05	2.02e-05
Vgs:	-8.08e-01	7.80e-01	1.64e+00	1.64e+00	7.80e-01
Vds:	1.05e+00	8.08e-01	1.64e+00	1.70e+00	1.67e+00
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	7.10e-01	7.10e-01	7.10e-01	7.10e-01	7.10e-01
Vdsat:	0.00e+00	6.96e-02	9.35e-01	9.35e-01	6.96e-02
Gm:	0.00e+00	5.75e-04	1.73e-04	1.73e-04	5.80e-04
Gds:	0.00e+00	1.98e-07	7.95e-07	7.95e-07	1.98e-07
Gmb:	0.00e+00	1.17e-05	3.53e-06	3.53e-06	1.18e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	4.60e-16	2.07e-15	4.60e-17	4.60e-17	2.07e-15
Cdov:	4.60e-16	2.07e-15	4.60e-17	4.60e-17	2.07e-15
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgs:	0.00e+00	1.08e-13	2.40e-15	2.40e-15	1.08e-13
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	3.60e-14	0.00e+00	0.00e+00	0.00e+00	0.00e+00

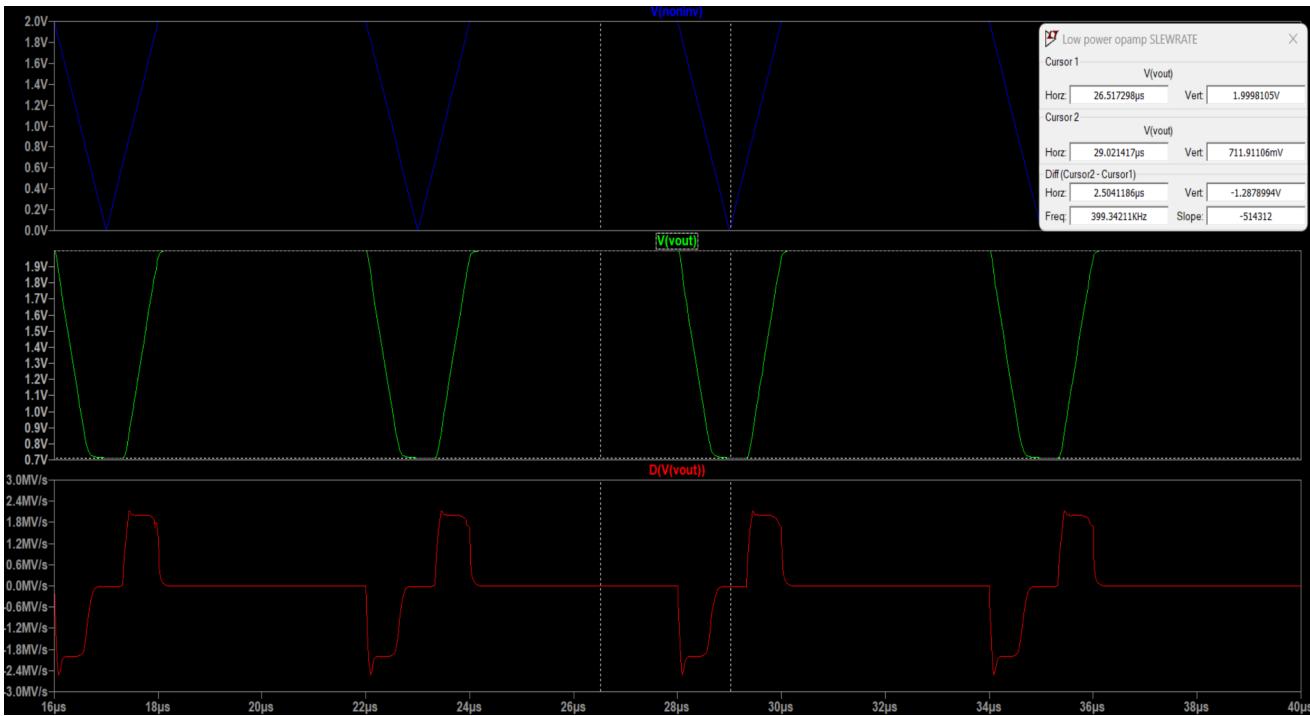
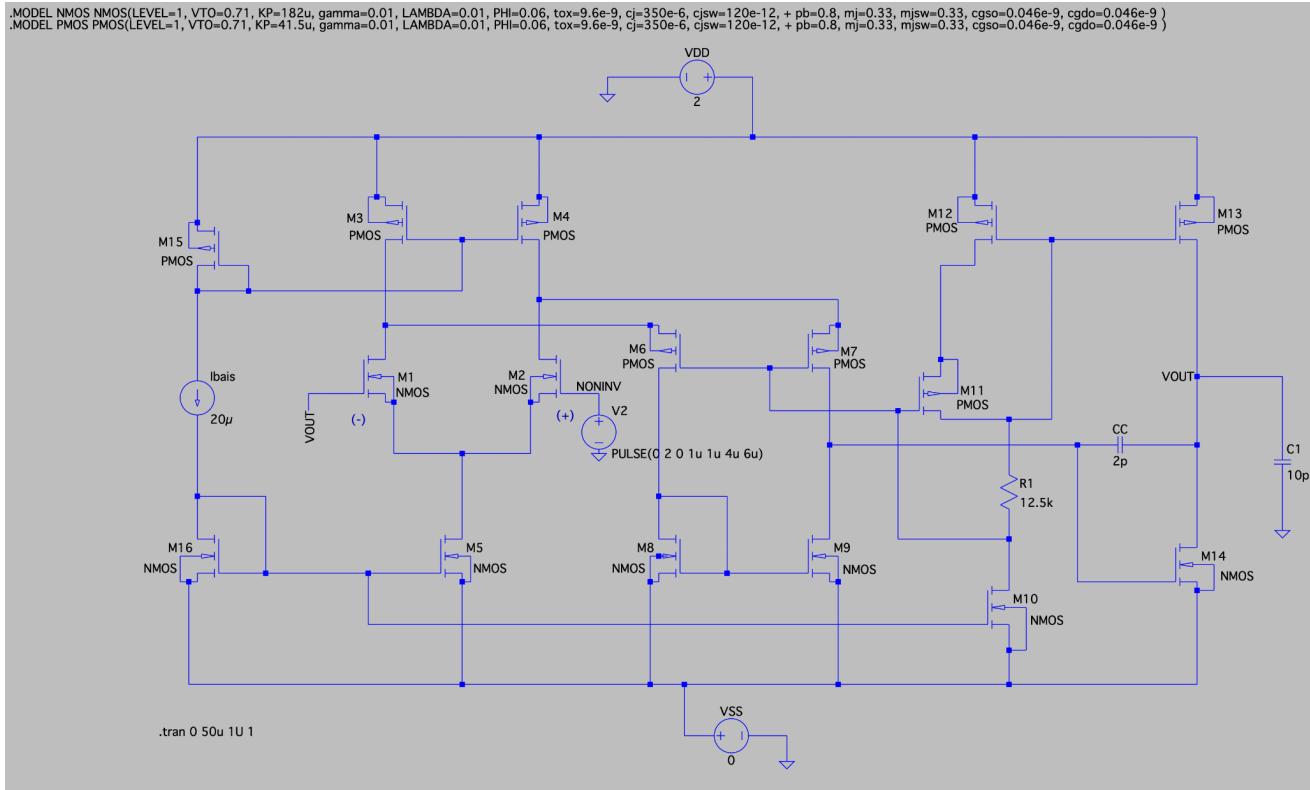
AC Analysis of the Opamp with Bode Plot



DC Analysis for Output Voltage Swing

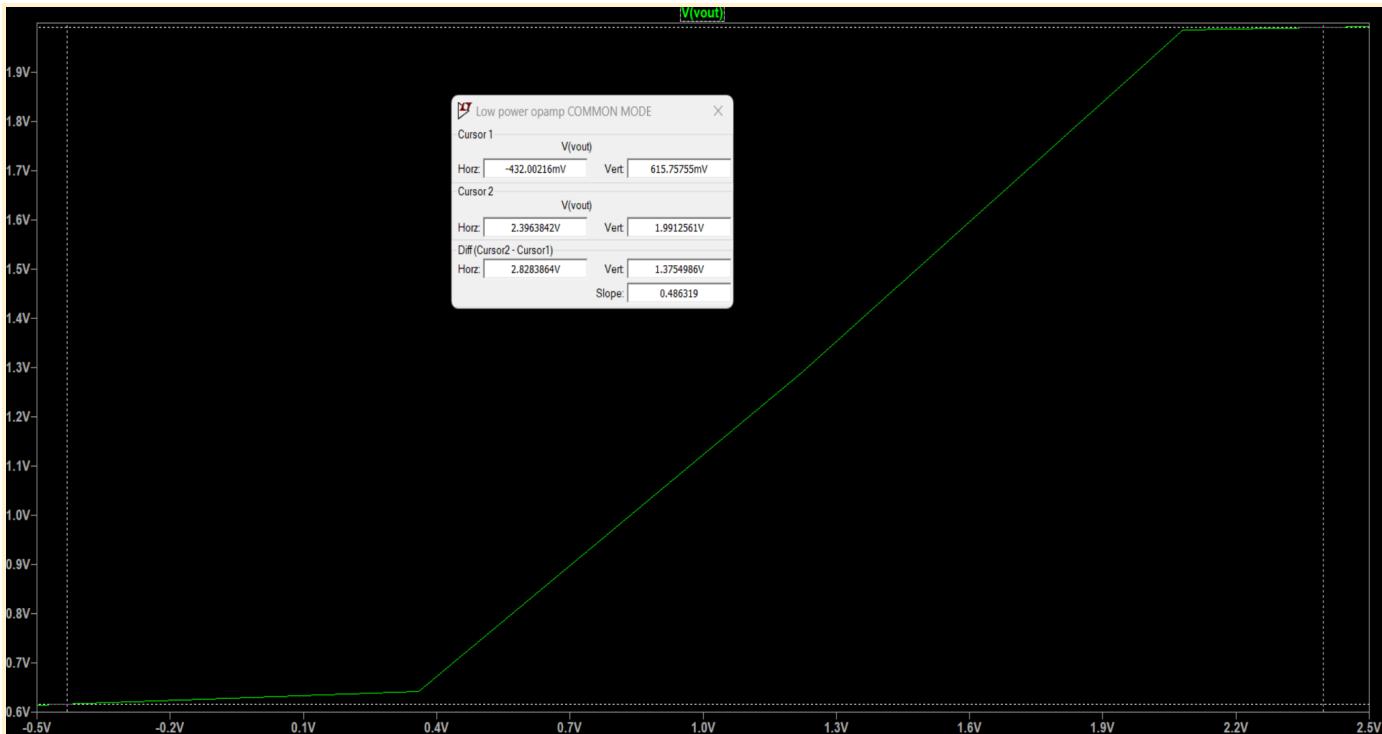
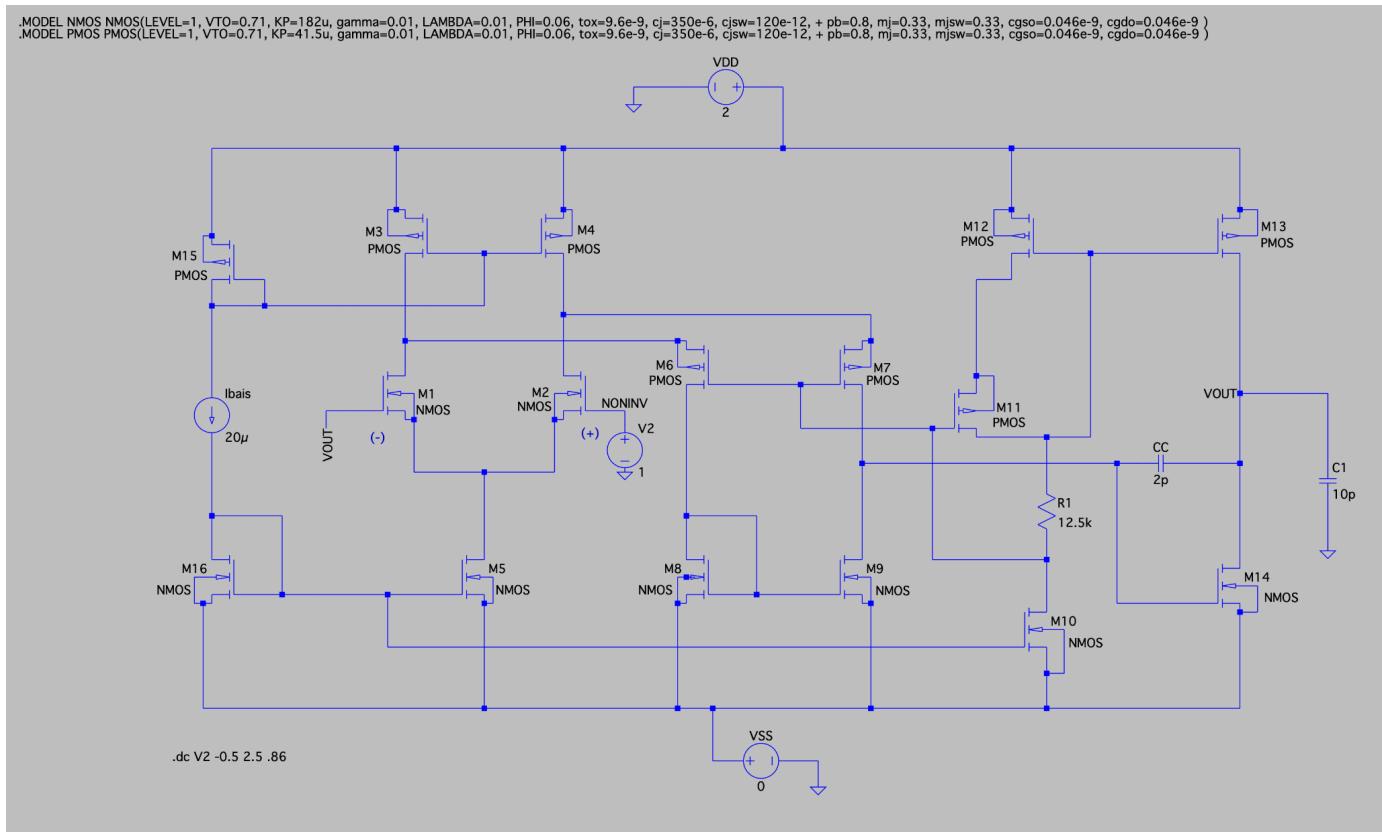


Slew Rate Analysis for Opamp



$$\text{Slew Rate} = I_5 / CC = 20 \mu\text{A} / 2\text{pF} = 10 \text{ V/uS}$$

Common Mode Analysis



The findings indicate that the opamp under study has a V_{min} of 0.61 V and a V_{max} of 2 V for common mode.

A Comparative Study of Simulated Parameters and Design

Parameters for Design	Original	Simulated
Vout(Max)	1.75 V	2 V
Vout(Min)	0.5 V	0.065 V
CM Vin(Max)	2.5 V	2.5 V
CM Vin(Min)	1 V	1 V
Phase Margin	60 Degrees	66 Degrees
Gain Bandwidth Product	10 MHz	10 MHz