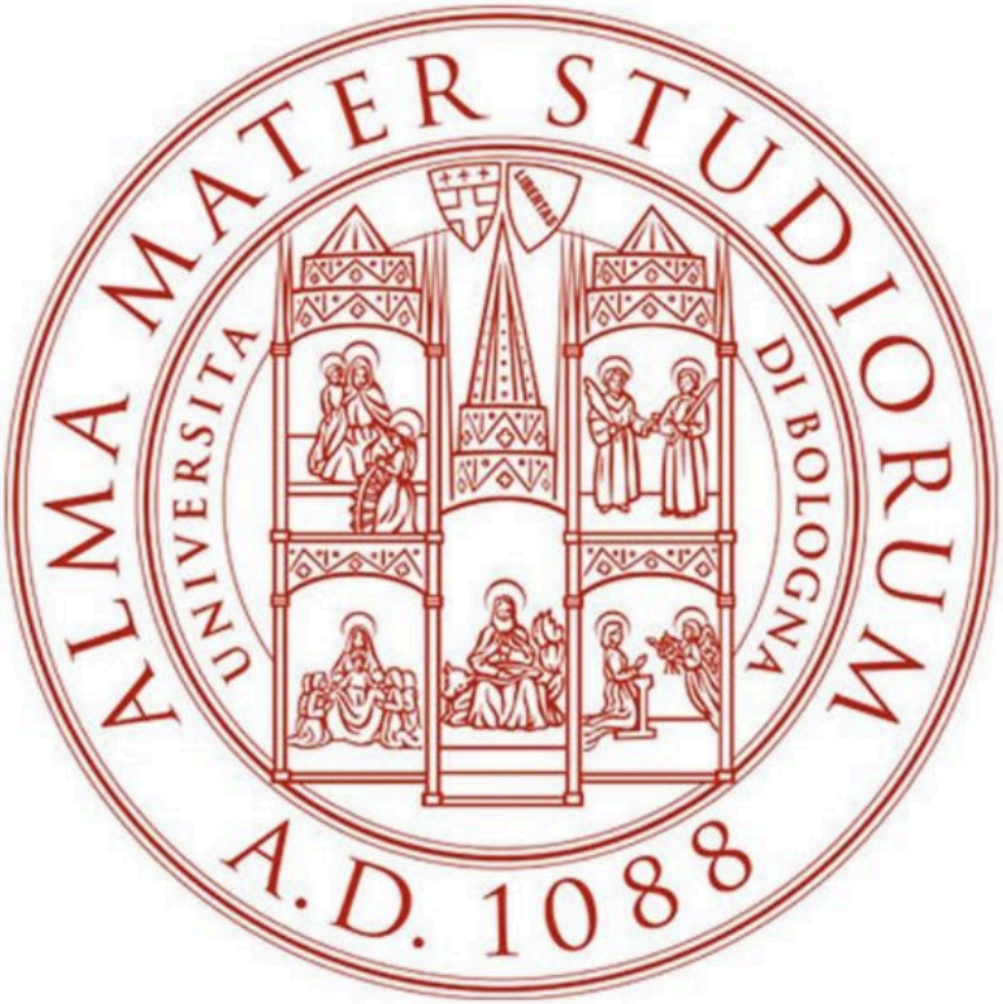


UNIVERSITY OF BOLOGNA

NAME : OM MISHRA

MATRICULATION : 0001101279

COURSE NAME : ANALOG CIRCUITS AND SENSOR SYSTEMS

PROJECT NAME : 2 STAGE OPAMP

Specifications

V_{DD}/V_{SS}	2.5/-2.5 V
Slew Rate	$+5/-5$ V/μs
Load Capacitor C_L	5pF
max Vin Common Mode	2.1V
min Vin Common Mode	-1.3V
max Vout	2.2V
min Vout	-2.2V
Gain Bandwidth	5MHz
Differential Gain	$>$80dB
Phase Margin	$>60^\circ$

Objective

The project's goal is to create a two-stage operational amplifier. Two sections can be distinguished from the entire circuit:

1. Biasing Circuit
2. Two Stage Op-Amp

Circuit Design

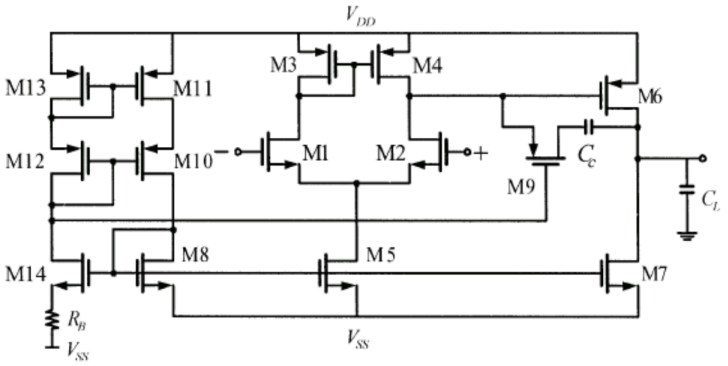


Figure 1: Op-Amp CMOS 2 stadi

The initial phase in the process is to calculate the transistor size, which is the ratio of the transistors' width to length (W/L) in relation to the *two-stage Op-amp*. Next, we will address the transistor sizes in the circuit's *biasing* section, which is located on the circuit's left side.

Here are the parameters of the N-Mos transistor

```
.model NMOD1CAP  NMOS  LEVEL=1
+ vto = 0.71     gamma = 0.01
+ phi = 0.6     kp= 182e-6
+ lambda = 0.01
+ tox = 9.6e-9
+ cj = 350e-6 cjsw = 120e-12
+ pb = 0.8 mj=0.33 mjsw = 0.33
+ cgso = 0.046e-9 cgdo = 0.046e-9
```

Because of the criteria, we can use the following formula to calculate the value of mobility:

$$\mu_n = e_0 \times \left(\frac{e_r}{tox_n}\right)$$

$e_0 = 8.854 \times 10^{-12}$, $e_r = 3.9$ → $\mu_n = 0.0506$

Here are the parameters of the P-Mos transistor

```
.model PMOD1CAP  PMOS  LEVEL=1
+ vto = -0.901    gamma = 0.01
+ phi = 0.6      kp= 41.5e-6
+ lambda = 0.01
+ tox = 9.6e-9
+ cj = 350e-6 cjsw = 120e-12
+ pb = 0.8 mj=0.33 mjsw = 0.33
+ cgso = 0.046e-9 cgdo = 0.046e-9
```

Because of the criteria, we can use the following formula to calculate the value of mobility:

$$\mu_p = e_0 \times \left(\frac{e_r}{tox_p}\right)$$

$e_0 = 8.854 \times 10^{-12}$, $e_r = 3.9$ ➔ $\mu_p = 0.0115$

Design Choices ;

Differential Gain	Phase Margin	Noise
80dB	60	1.0020e-12

Part - 1

Design Procedure for calculation of the Form Factor:

Step 1

$$Cc = \frac{16}{3} * \frac{KT}{GB\,.\,S(n)} \times \left(1 + \frac{SR}{GB*Vov3}\right)$$

$KT =$ *1.380649e-23 * 298*

$\sqrt{s_n(f)}$ *= 40 × 10⁻⁹*

GB = 5Mhz = 3.1416 × 10⁷

SR = 5 × 10⁶

$$VDD - Vov_{cm-max} = Vov3 + \left|VTp\right| + Vov1 - Vov1 - VTn$$

Vov3 = 0.2090 ; Cc = 1.0020e-12

Step 2

In the second phase, we will determine I6 and I7 using the value of Cc that was determined in the previous step.

$$I_6 = SR(Cc + CL) = I_7$$

I6 = 3.1012e-05 ; I7 = 3.1012e-05

Step 3

Now, lets compute the length of M6

$$L_6 = \sqrt{\frac{3}{2} * \frac{\mu_p . Vov6.Cc}{GB . (Cc + CL) . \tan(PM)}}$$

$$Vov6 = VDD - Vomax$$

Vov6 = 0.3000 ; L6 = 4.3019e-06

Step 4

The transistor M6's size is measured in the next procedure, after which we may determine its width

$$S6 = \frac{2I6}{\beta' p . V_{OV6}^2}$$

S6 = 16.6062 ; W6 = 7.1438e-05

We assume that all transistors have the same length equal to the length of M6.

$L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = L_8 = L_9 = L_{10} = L_{11} = L_{12} = L_{13} = L_{14} = L$

Step 5

In this step we'll measure I5

$$I_5 = Cc \times SR$$

$$I_1 = I_2 = I_3 = I_4 = \frac{I_5}{2}$$

I5 = 6.0120e-06

Step 6

Let's now compute S1 and W1. (Remember that S1 is in the saturation zone.)

$$S1 = \frac{2I1}{\beta' n \,.\, V_{OV1}^2} \qquad V_{ov1} = \frac{SR}{GB}$$

Vov1 = 0.1592 ; S1 = 1.3028 ; W1 = 5.6044-06

Step 7

This step involves computing S5 and W5.

$$S5 = \frac{2I5}{\beta' n \,.\, V_{OV5}^2}$$

$$Vov5 = VI_{cm-MIN} - VSS - VTn - Vov1$$

Vov5 = 0.3308 ; S5 = 0.6039 ; W5 = 2.5978e-06

Step 8

We are now able to compute the transistor M7's size because of the computations we performed in the earlier phases.

We are aware of the following fact:

$$V_{GS5} = V_{GS7} \rightarrow \frac{I_7}{I_5} = \frac{S_7}{S_5}$$

And due to design choice:

$$\frac{I_5}{C_c} = \frac{I_7 - I_5}{C_L} = SR$$

Therefore, we have now:

$$s_7 = \frac{c_c + c_L}{c_c} \times s_5$$

S7 = 3.1141 ; W7 = 1.3400e-05

Step 9

Perfect Balancing is achieved for the following condition

$$V_{GS7} = V_{GS4} = V_{GS3} \quad \rightarrow \quad S_3 = S_4 = \frac{S_6}{2S_7} \times s_5$$

S4 = 1.6096 ; W3 = 6.9245e-06 ; W4 = 6.9245e-06

Step 10

This step allows us to measure the M9's size and compute the transistor's width. The need that M9 operate in the triode area is one crucial consideration.

$$S_9 = \frac{C_c}{C_L + C_c} \times S_6$$

S9 = 3.2193 ; W9 = 1.3849e-05

Step 11

In this step, we will compute s1 and s2 and determine the relationship between the overdrive of M9, M6, and M8 using all of the data from the preceding steps.

$$s_1 = \frac{2I_1}{v_{0v1}^2\, k_{pn}}$$

$$w_1 = s_1 \times L$$

$$v_{ov2} = v_{imin} - v_{ss} - v_{tn} - v_{ov5}$$

$$s_2 = \frac{2I_2}{v_{0v2}^2\, k_{pn}}$$

$$W_2 = s_2 \times L$$

And due to the circuit we have;

$$V_{ov9} = V_{ov6} \quad , \quad V_{ov8} = V_{GS5}$$

S1 = 1.4955 ; W1 = 5.3928e-06 ; Vov2 = 0.1592 ; S2 = 1.4955 ; W2 = 5.3928e-06 ; Vov9 = 0.3000 ; Vgs5 = 1.0408 ; Vov8 = 0.3308

W1	W2	W3	W4	W5	W6	W7	W9
5.6044u	5.6044u	6.9245u	6.9245u	2.5978u	7.1438u	13.400u	13.849u

Part - 2

The biasing part transistor sizing has been completed in this section. Initially, we measured M8's current using an ideal biasing circuit made up of a current source and M8 in order to determine a current that was more sufficient in terms of power consumption.

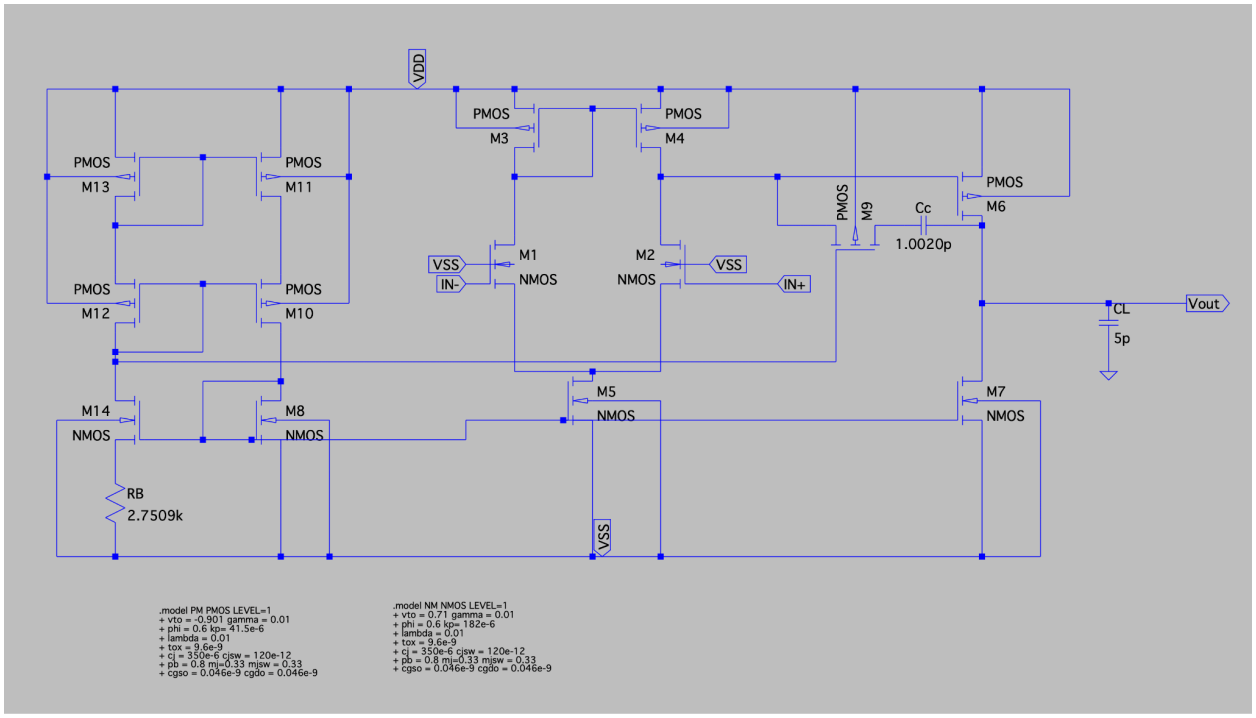
W8	W10	W11	W12	W13	W14
2.5978u	13.849u	13.849u	13.849u	13.849u	10.391u

Now in the next section, let's continue with the simulation;

Simulation

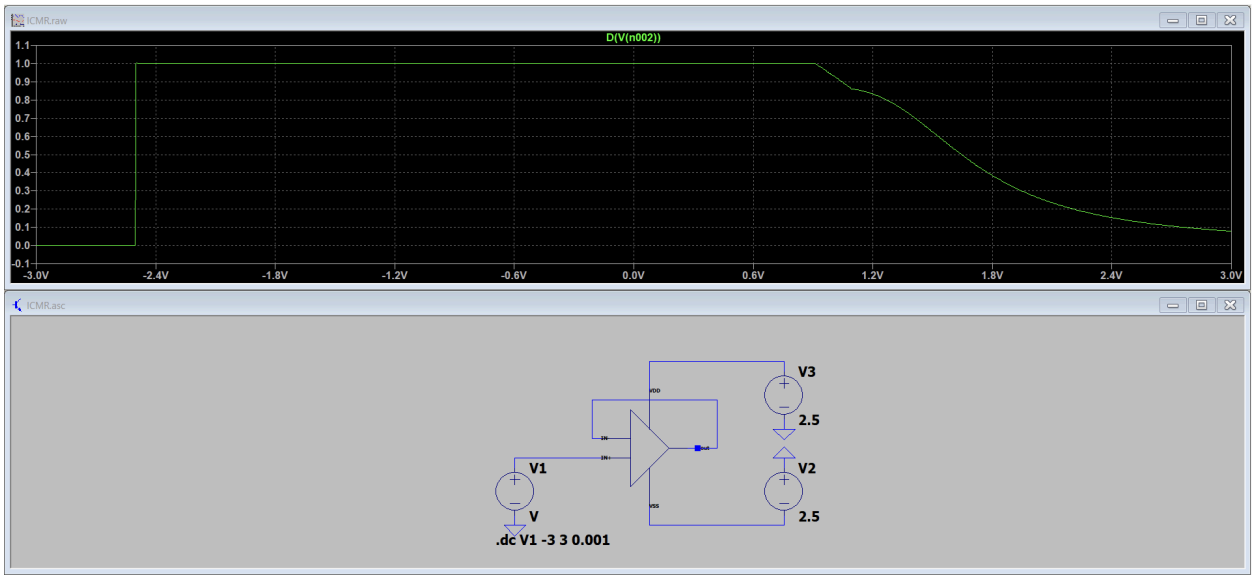
Prior to initiating the simulation, there are a few things we should be aware of:

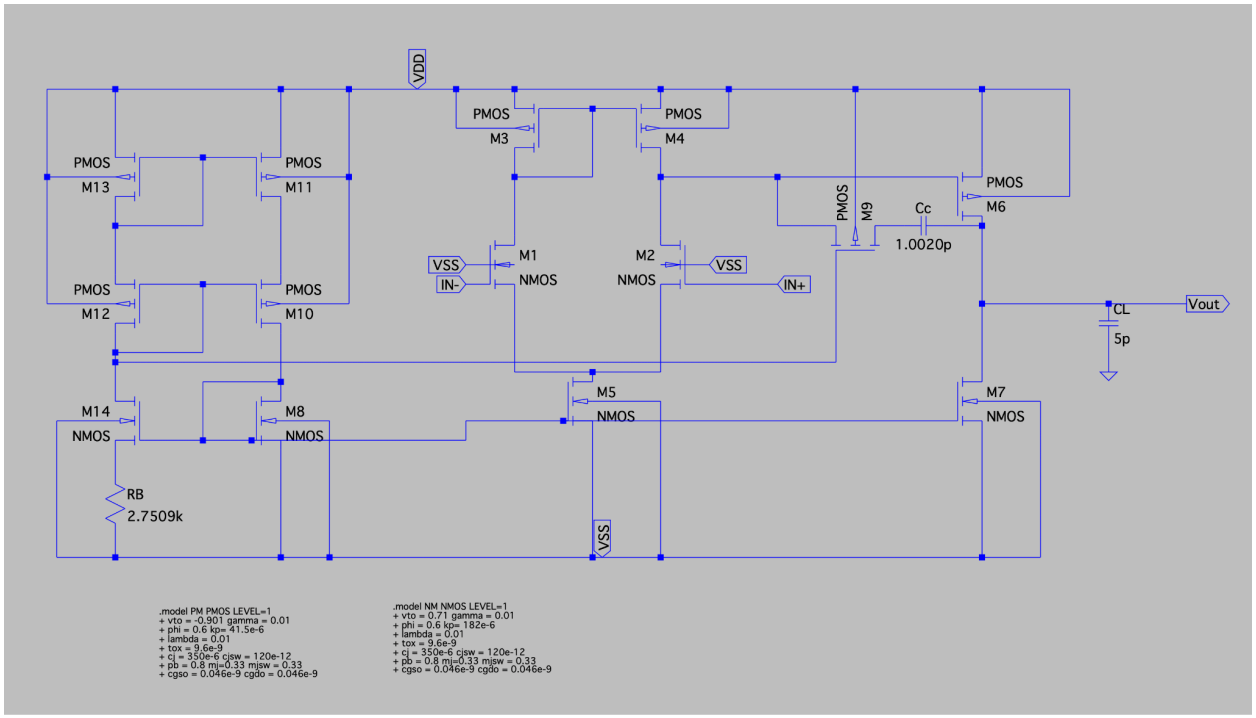
1. The source is the pin that is nearest to the gate.
2. The majority of Nmos transistors and Pmos transistors need to be linked to the VSS and VDD, respectively.
3. We created a subcircuit of the intended two-stage op-amp in order to streamline the simulation, and we then verified our intended output using several analysers.



Circuit for Analysis

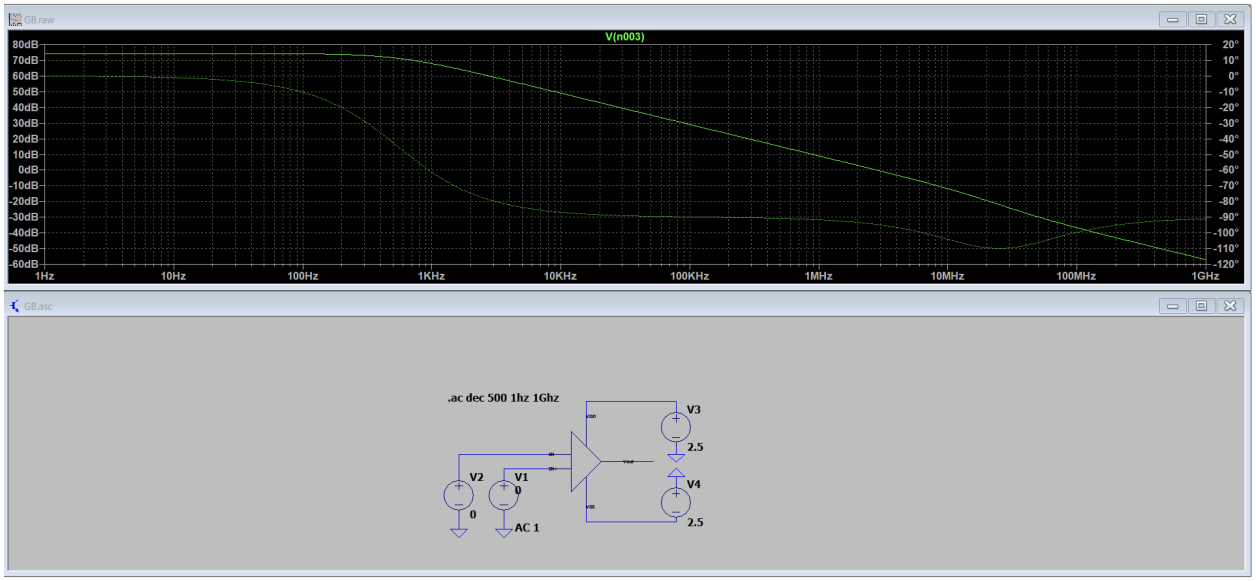
Input Common Mode Range

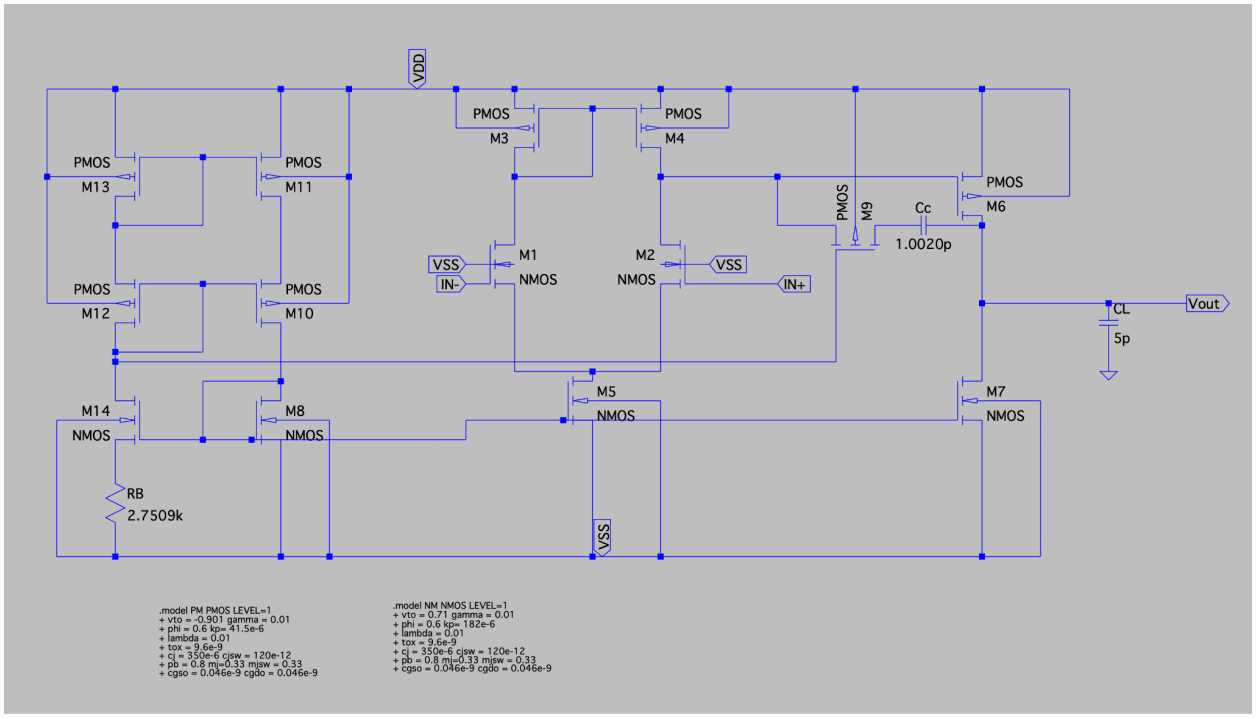




Circuit for Analysis

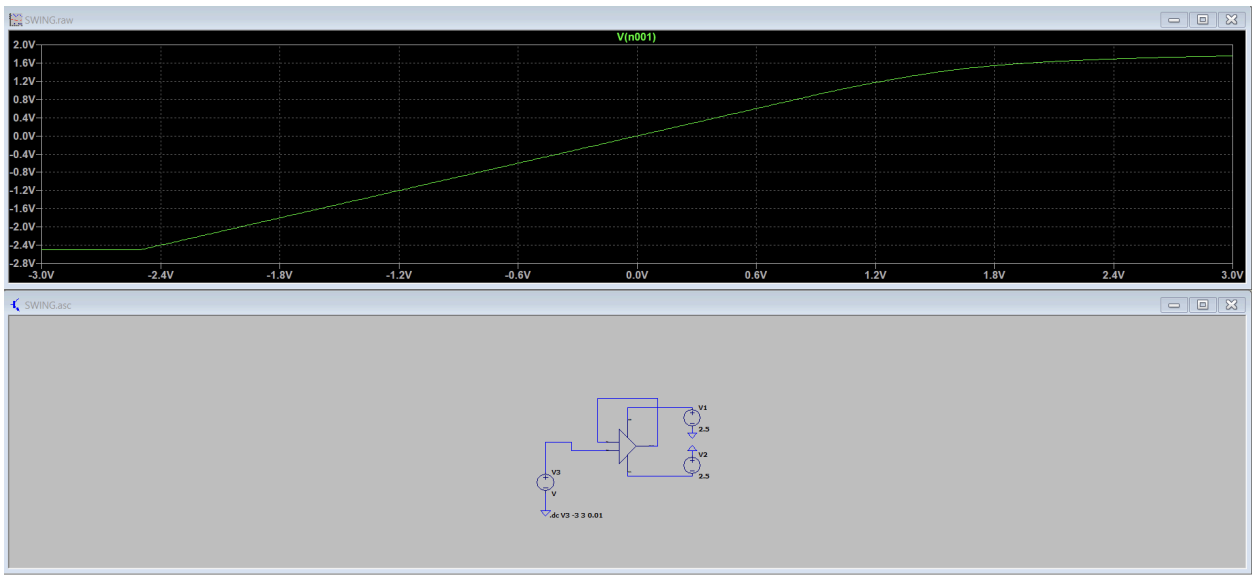
Gain Bandwidth

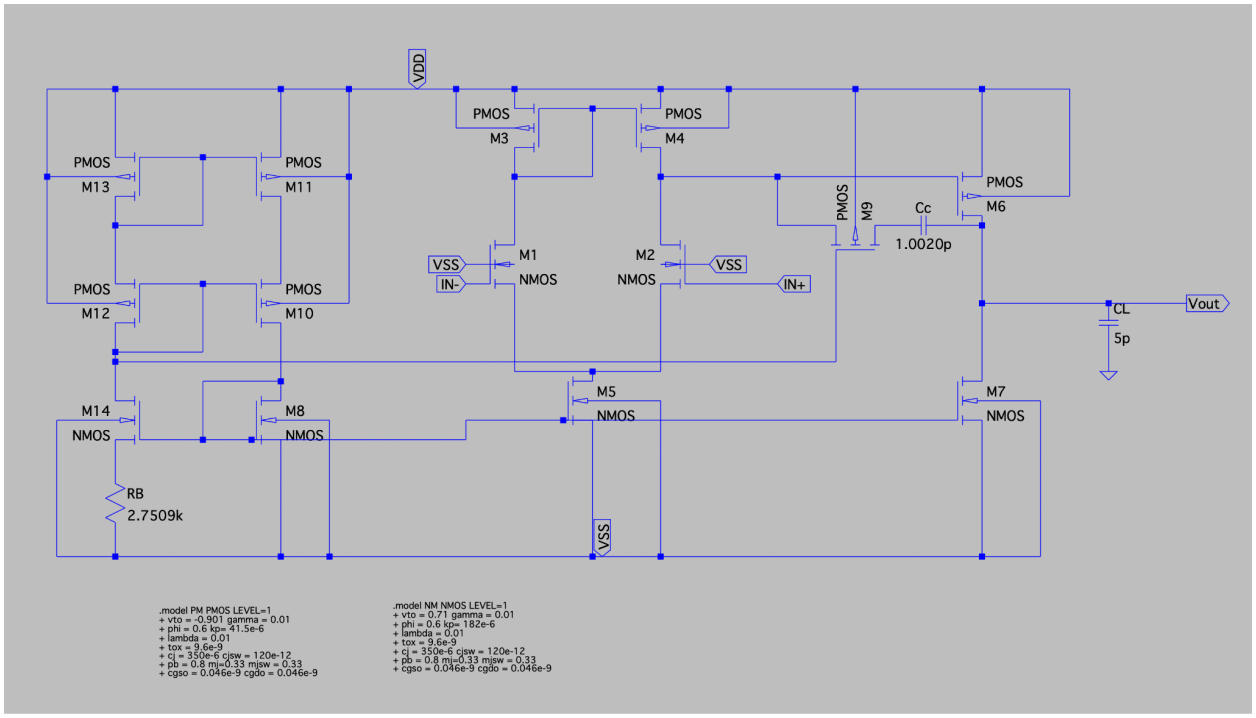




Circuit for Analysis

Swing





Circuit for Analysis

Slew Rate