國立清華大學 電機工程系

112 學年度第一學期

SOC Design Laboratory

Lab#2

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▪ Brief introduction about the overall system

☆ AXI-Master Interface

First, put the C code of FIRN11MAXI into Vitis_hls, set directives and perform simulation, synthesis, co-simulation. After confirming that there is no problem, and then export RTL as IP.

Next, open Vivado, start a new project, and introduce Zynq7 processor, then introduce the IP completed through Vitis_hls, and then run block automation.

Because AXI-Lite and AXI-Master use different ports in the processor system block, open the HP port of the processor system block, and then run connection automation. After completion, use HDL wrapper and finally generate bitstream and feed the bitstream to the FPGA for execution to verify the correctness of circuit execution.

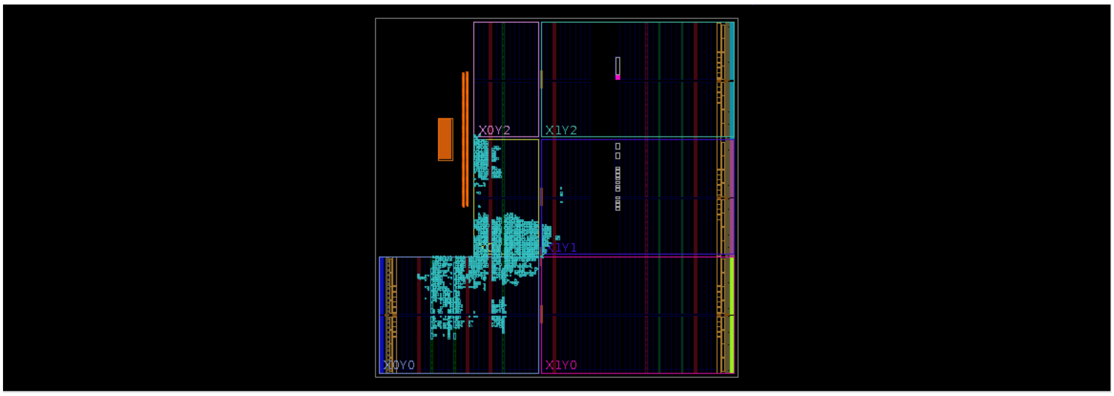
☆ Stream Interface

First, put the C code of FIRN11Stream into Vitis_hls, the pragma(inline) is set, so there is no need to set directives. Perform simulation, synthesis, co-simulation. After confirming that there is no problem, and then export RTL as IP. Next, open Vivado, start a new project, and introduce Zynq7 processor, then introduce the IP completed through Vitis_hls, and then run block automation. Because AXI-Lite and AXI-Stream use different ports in the processor system block, open the HP port of the processor system block, because AXI master to stream is implemented using Xilinx DMA IP, it's needs to be introduced. Then this LAB requires two DMAs, a single Read to do DMA in, and a single write to do DMA out. Then press connection automation, and then manually connect the wire to DMA in and DMA out, use HDL wrapper and finally generate bitstream and feed the bitstream to the FPGA for execution to verify the correctness of circuit execution.

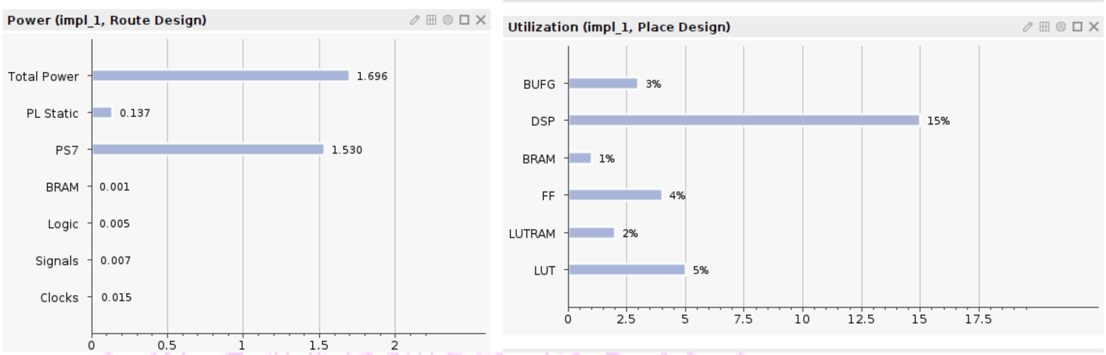
- ## What is observed & learned?

From this lab, I learned how to use different AXI interfaces and set directives, and how to solve problems when encountering problems during the lab. I have a deep understanding of the entire design process from developing IP with HLS and using Vivado for block design and setting the processor system port and then generating bitstream, etc., I believe it will be better if enhance my knowledge of communication protocols!

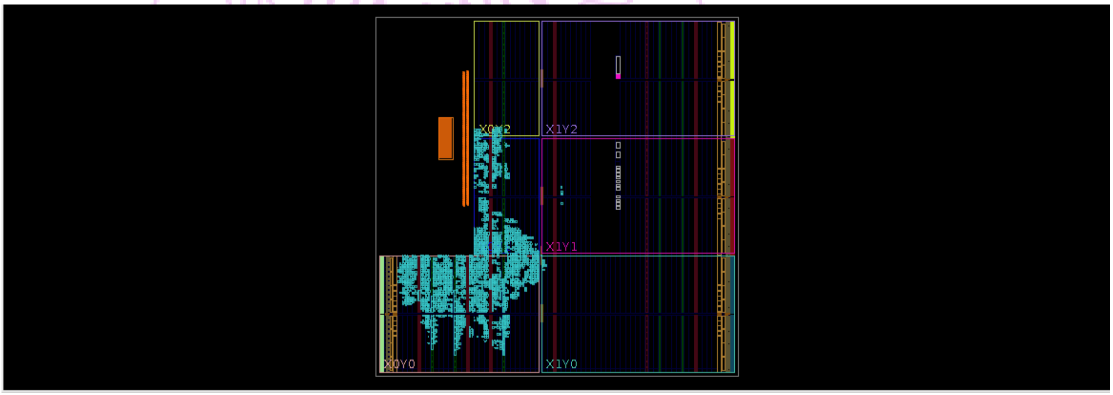
☆ AXI-Master



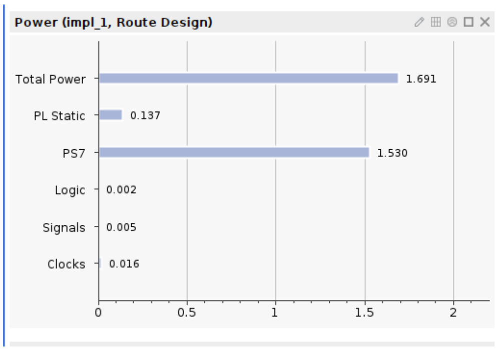
Project summary (AXI-Master)

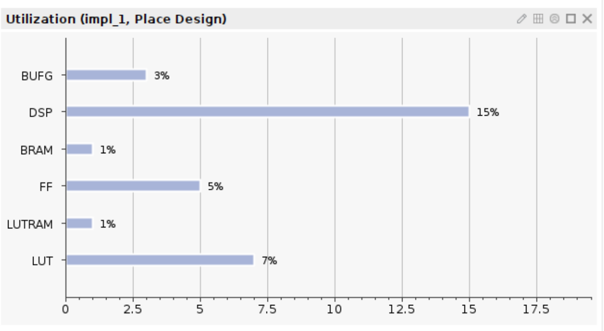


☆ AXI-Stream



Project summary (AXI-Stream)





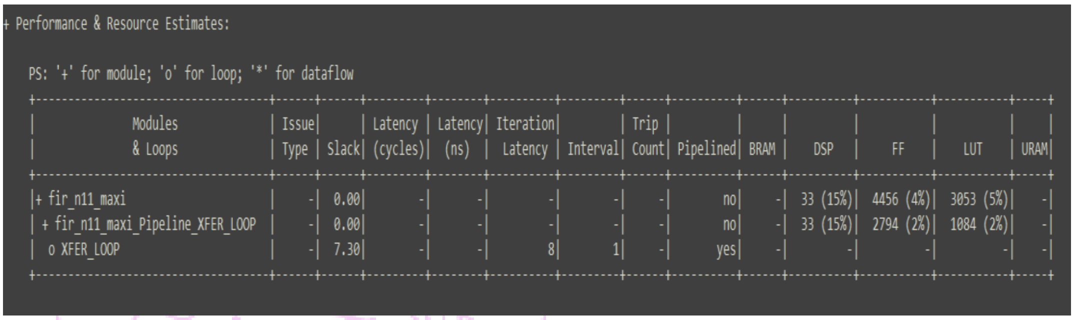
From the above AXI-Master and AXI-Stream interface diagram, the total power of AXI-Master is higher than that of AXI-Stream. The utilization part, AXI-Stream uses LUT higher than AXI-Master.

- ## Screen dump

☆ AXI-Master Interface

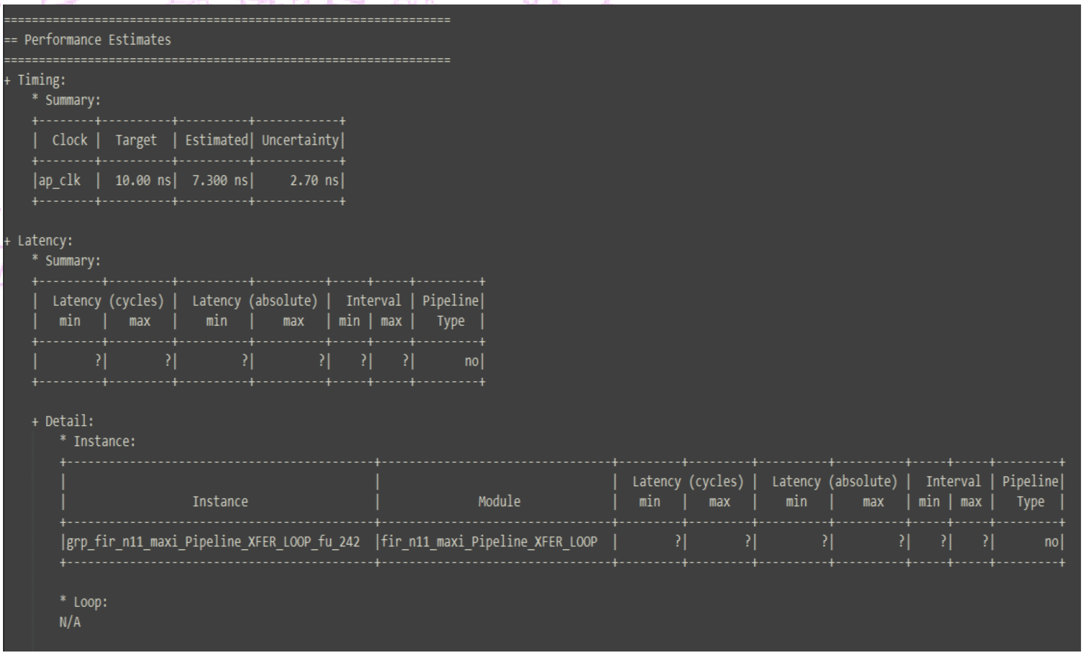
- ### Performance

1. Synthesis Summary Report



```
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +---------------------------------+------+------+---------+--------+----------+---------+------+----------+------+---------+-----------+-----------+-----+
    |              Modules            | Issue|      | Latency | Latency| Iteration|         | Trip |          |      |         |           |           |     |
    |              & Loops            | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP   |     FF    |    LUT    | URAM|
    +---------------------------------+------+------+---------+--------+----------+---------+------+----------+------+---------+-----------+-----------+-----+
    |+ fir_n11_maxi                   |     -|  0.00|        -|       -|         -|        -|     -|        no|     -| 33 (15%)|  4456 (4%)|  3053 (5%)|    -|
    | + fir_n11_maxi_Pipeline_XFER_LOOP |     -|  0.00|        -|       -|         -|        -|     -|        no|     -| 33 (15%)|  2794 (2%)|  1084 (2%)|    -|
    |  o XFER_LOOP                    |     -|  7.30|        -|       -|         8|        1|     -|       yes|     -|        -|          -|          -|    -|
    +---------------------------------+------+------+---------+--------+----------+---------+------+----------+------+---------+-----------+-----------+-----+
```

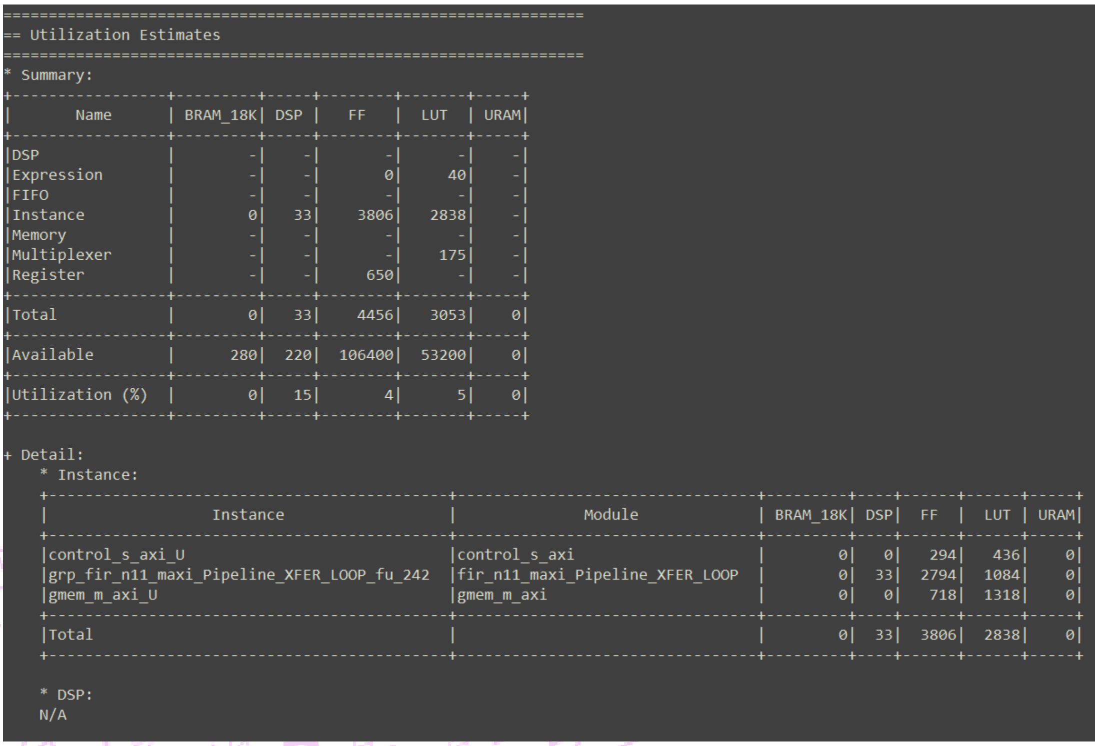
2. Synthesis Detail Report



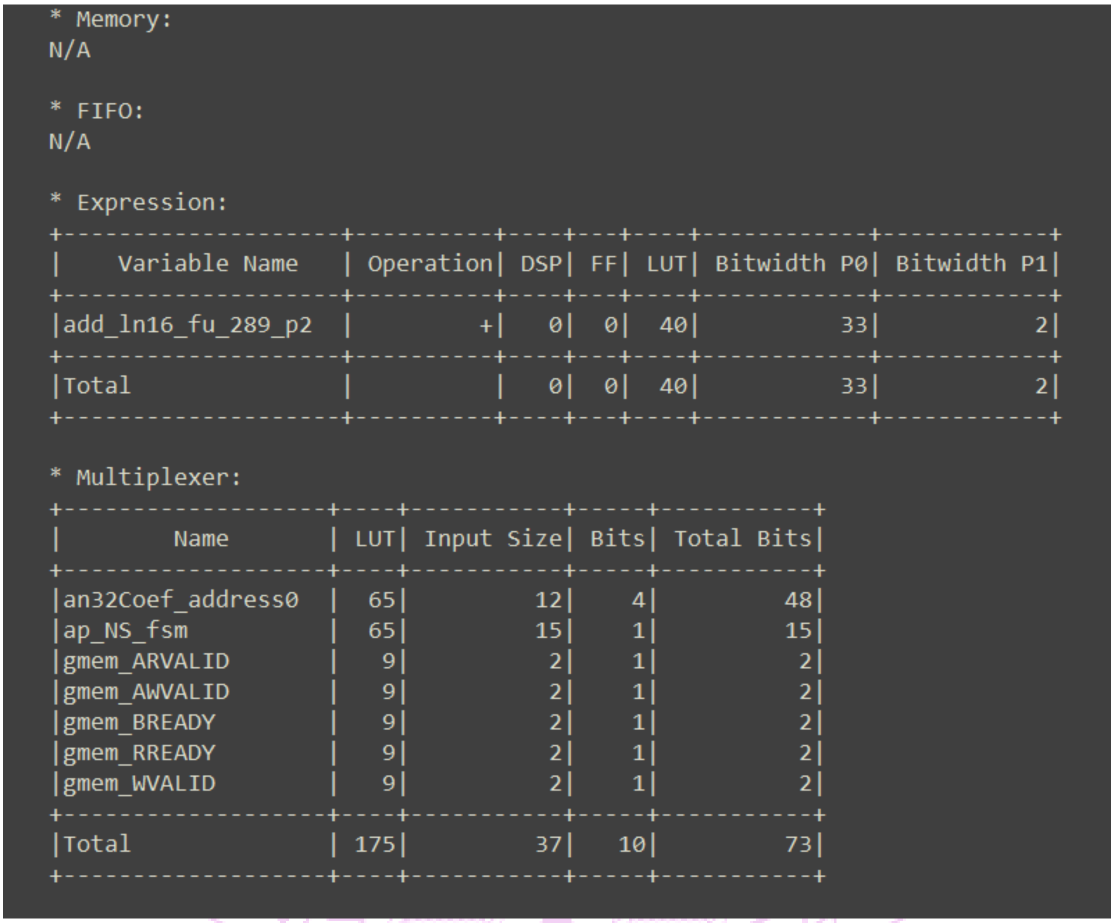
```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  7.300 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +-------------------------------------+----------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                     |                                  |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |               Instance              |              Module              |   min   |   max   |    min   |    max   | min | max |   Type  |
        +-------------------------------------+----------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242  |fir_n11_maxi_Pipeline_XFER_LOOP  |        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +-------------------------------------+----------------------------------+---------+---------+----------+----------+-----+-----+---------+

        * Loop:
        N/A
```

- Utilization

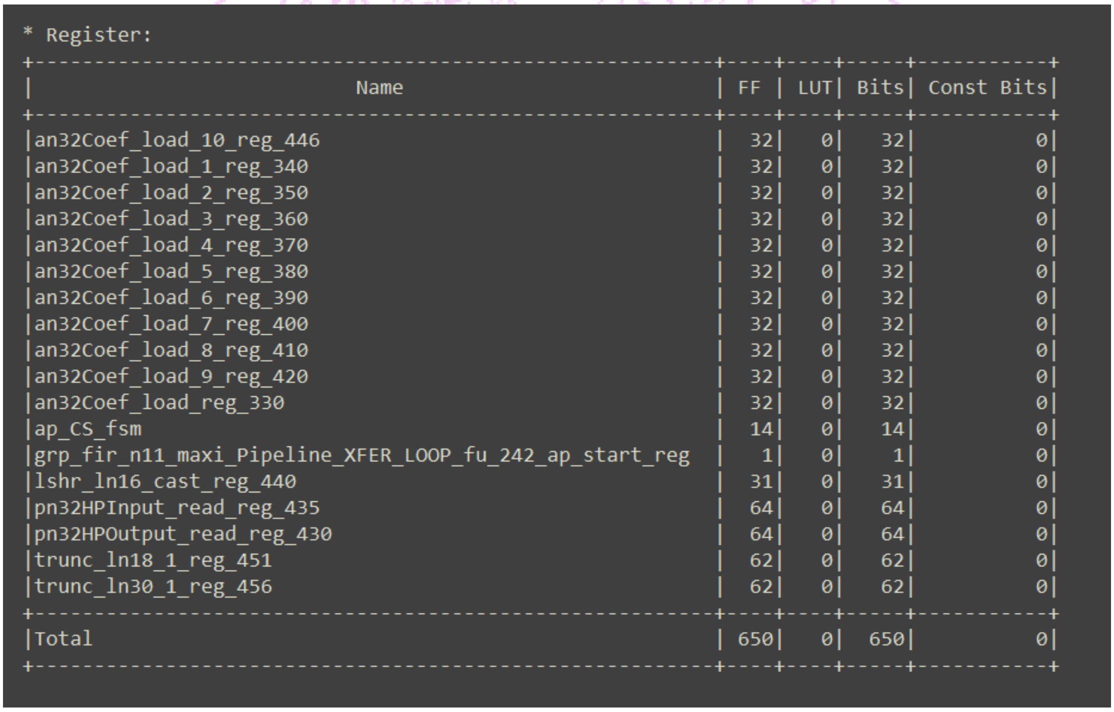
1. Synthesis Detail Report



```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     40|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    3806|   2838|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|    175|    -|
|Register         |        -|    -|     650|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    4456|   3053|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       4|      5|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-------------------------------------------+----------------------------------+---------+----+------+------+-----+
    |                  Instance                 |              Module              | BRAM_18K| DSP|  FF  | LUT  | URAM|
    +-------------------------------------------+----------------------------------+---------+----+------+------+-----+
    |control_s_axi_U                            |control_s_axi                     |        0|   0|   294|   436|    0|
    |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242 |fir_n11_maxi_Pipeline_XFER_LOOP   |        0|  33|  2794|  1084|    0|
    |gmem_m_axi_U                               |gmem_m_axi                        |        0|   0|   718|  1318|    0|
    +-------------------------------------------+----------------------------------+---------+----+------+------+-----+
    |Total                                      |                                  |        0|  33|  3806|  2838|    0|
    +-------------------------------------------+----------------------------------+---------+----+------+------+-----+

    * DSP:
    N/A
```



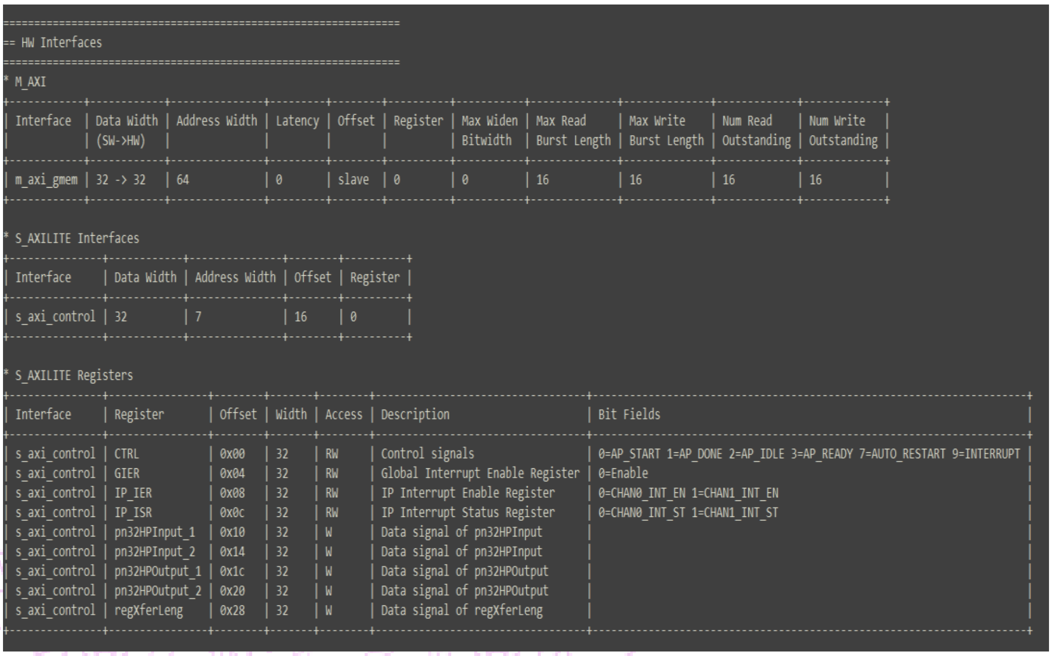
```
* Memory:
N/A

* FIFO:
N/A

* Expression:
+--------------------+----------+----+---+----+------------+------------+
|    Variable Name   | Operation| DSP| FF| LUT| Bitwidth P0| Bitwidth P1|
+--------------------+----------+----+---+----+------------+------------+
|add_ln16_fu_289_p2  |         +|   0|  0|  40|          33|           2|
+--------------------+----------+----+---+----+------------+------------+
|Total               |          |   0|  0|  40|          33|           2|
+--------------------+----------+----+---+----+------------+------------+

* Multiplexer:
+-------------------+----+-----------+-----+-----------+
|        Name       | LUT| Input Size| Bits| Total Bits|
+-------------------+----+-----------+-----+-----------+
|an32Coef_address0  |  65|         12|    4|         48|
|ap_NS_fsm          |  65|         15|    1|         15|
|gmem_ARVALID       |   9|          2|    1|          2|
|gmem_AWVALID       |   9|          2|    1|          2|
|gmem_BREADY        |   9|          2|    1|          2|
|gmem_RREADY        |   9|          2|    1|          2|
|gmem_WVALID        |   9|          2|    1|          2|
+-------------------+----+-----------+-----+-----------+
|Total              | 175|         37|   10|         73|
+-------------------+----+-----------+-----+-----------+
```



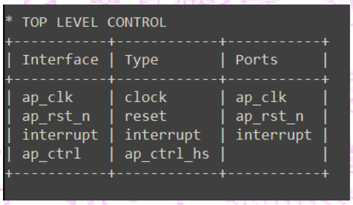
```
* Register:
+-----------------------------------------------------+----+----+-----+-----------+
|                         Name                        | FF | LUT| Bits| Const Bits|
+-----------------------------------------------------+----+----+-----+-----------+
|an32Coef_load_10_reg_446                             |  32|   0|   32|          0|
|an32Coef_load_1_reg_340                              |  32|   0|   32|          0|
|an32Coef_load_2_reg_350                              |  32|   0|   32|          0|
|an32Coef_load_3_reg_360                              |  32|   0|   32|          0|
|an32Coef_load_4_reg_370                              |  32|   0|   32|          0|
|an32Coef_load_5_reg_380                              |  32|   0|   32|          0|
|an32Coef_load_6_reg_390                              |  32|   0|   32|          0|
|an32Coef_load_7_reg_400                              |  32|   0|   32|          0|
|an32Coef_load_8_reg_410                              |  32|   0|   32|          0|
|an32Coef_load_9_reg_420                              |  32|   0|   32|          0|
|an32Coef_load_reg_330                                |  32|   0|   32|          0|
|ap_CS_fsm                                            |  14|   0|   14|          0|
|grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242_ap_start_reg  |   1|   0|    1|          0|
|lshr_ln16_cast_reg_440                               |  31|   0|   31|          0|
|pn32HPInput_read_reg_435                             |  64|   0|   64|          0|
|pn32HPOutput_read_reg_430                            |  64|   0|   64|          0|
|trunc_ln18_1_reg_451                                 |  62|   0|   62|          0|
|trunc_ln30_1_reg_456                                 |  62|   0|   62|          0|
+-----------------------------------------------------+----+----+-----+-----------+
|Total                                                | 650|   0|  650|          0|
+-----------------------------------------------------+----+----+-----+-----------+
```

- Interface

1. Synthesis Summary Report

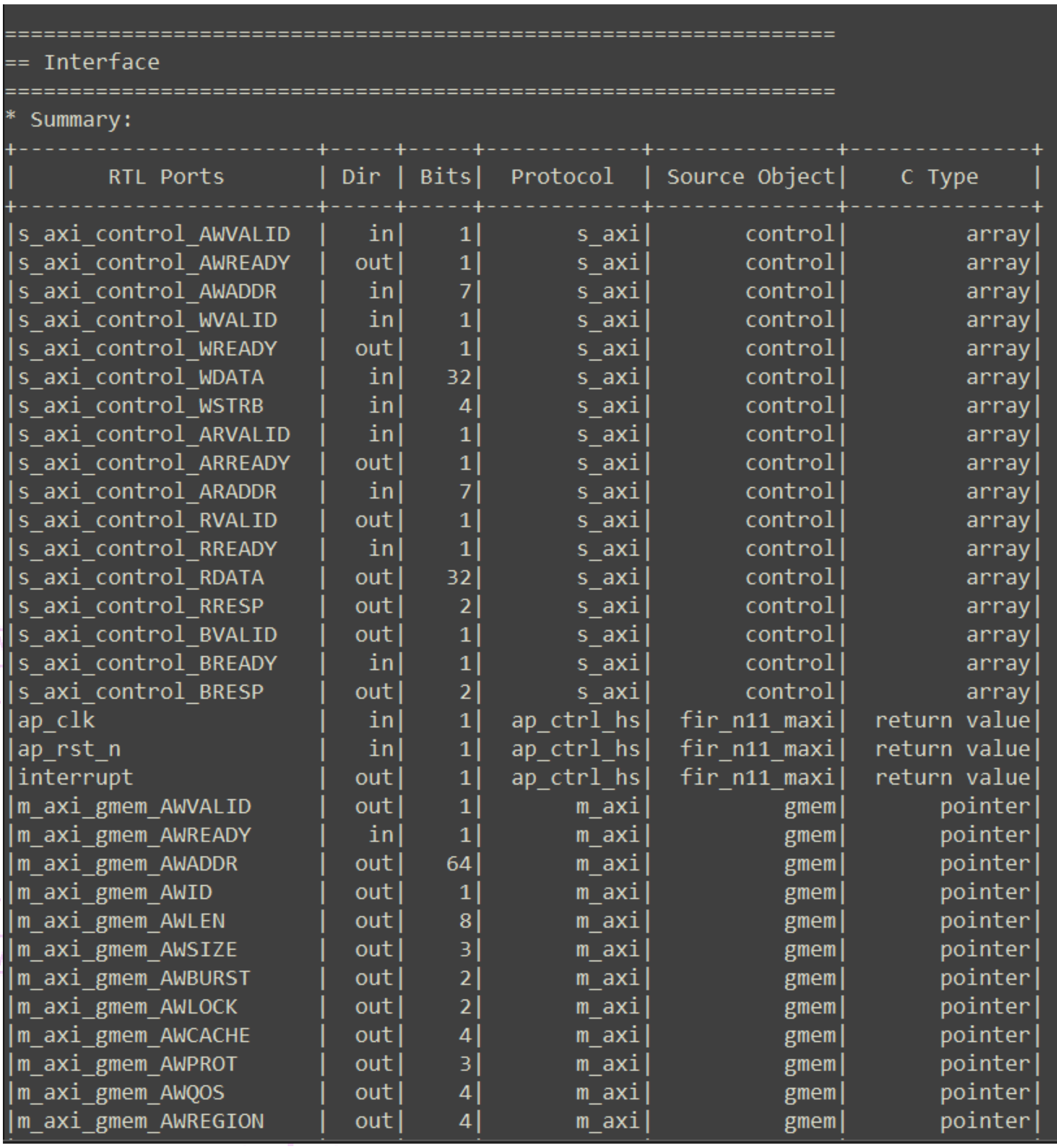


```
================================================================
== HW Interfaces
================================================================
* M_AXI
+------------+------------+---------------+---------+--------+----------+-----------+--------------+--------------+-------------+-------------+
| Interface  | Data Width | Address Width | Latency | Offset | Register | Max Widen | Max Read     | Max Write    | Num Read    | Num Write   |
|            | (SW->HW)   |               |         |        |          | Bitwidth  | Burst Length | Burst Length | Outstanding | Outstanding |
+------------+------------+---------------+---------+--------+----------+-----------+--------------+--------------+-------------+-------------+
| m_axi_gmem | 32 -> 32   | 64            | 0       | slave  | 0        | 0         | 16           | 16           | 16          | 16          |
+------------+------------+---------------+---------+--------+----------+-----------+--------------+--------------+-------------+-------------+

* S_AXILITE Interfaces
+---------------+------------+---------------+--------+----------+
| Interface     | Data Width | Address Width | Offset | Register |
+---------------+------------+---------------+--------+----------+
| s_axi_control | 32         | 7             | 16     | 0        |
+---------------+------------+---------------+--------+----------+

* S_AXILITE Registers
+---------------+-----------------+--------+-------+--------+----------------------------------+------------------------------------------------------------------+
| Interface     | Register        | Offset | Width | Access | Description                      | Bit Fields                                                       |
+---------------+-----------------+--------+-------+--------+----------------------------------+------------------------------------------------------------------+
| s_axi_control | CTRL            | 0x00   | 32    | RW     | Control signals                  | 0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT |
| s_axi_control | GIER            | 0x04   | 32    | RW     | Global Interrupt Enable Register | 0=Enable                                                         |
| s_axi_control | IP_IER          | 0x08   | 32    | RW     | IP Interrupt Enable Register     | 0=CHAN0_INT_EN 1=CHAN1_INT_EN                                    |
| s_axi_control | IP_ISR          | 0x0c   | 32    | RW     | IP Interrupt Status Register     | 0=CHAN0_INT_ST 1=CHAN1_INT_ST                                    |
| s_axi_control | pn32HPInput_1   | 0x10   | 32    | W      | Data signal of pn32HPInput       |                                                                  |
| s_axi_control | pn32HPInput_2   | 0x14   | 32    | W      | Data signal of pn32HPInput       |                                                                  |
| s_axi_control | pn32HPOutput_1  | 0x1c   | 32    | W      | Data signal of pn32HPOutput      |                                                                  |
| s_axi_control | pn32HPOutput_2  | 0x20   | 32    | W      | Data signal of pn32HPOutput      |                                                                  |
| s_axi_control | regXferLeng     | 0x28   | 32    | W      | Data signal of regXferLeng       |                                                                  |
+---------------+-----------------+--------+-------+--------+----------------------------------+------------------------------------------------------------------+
```

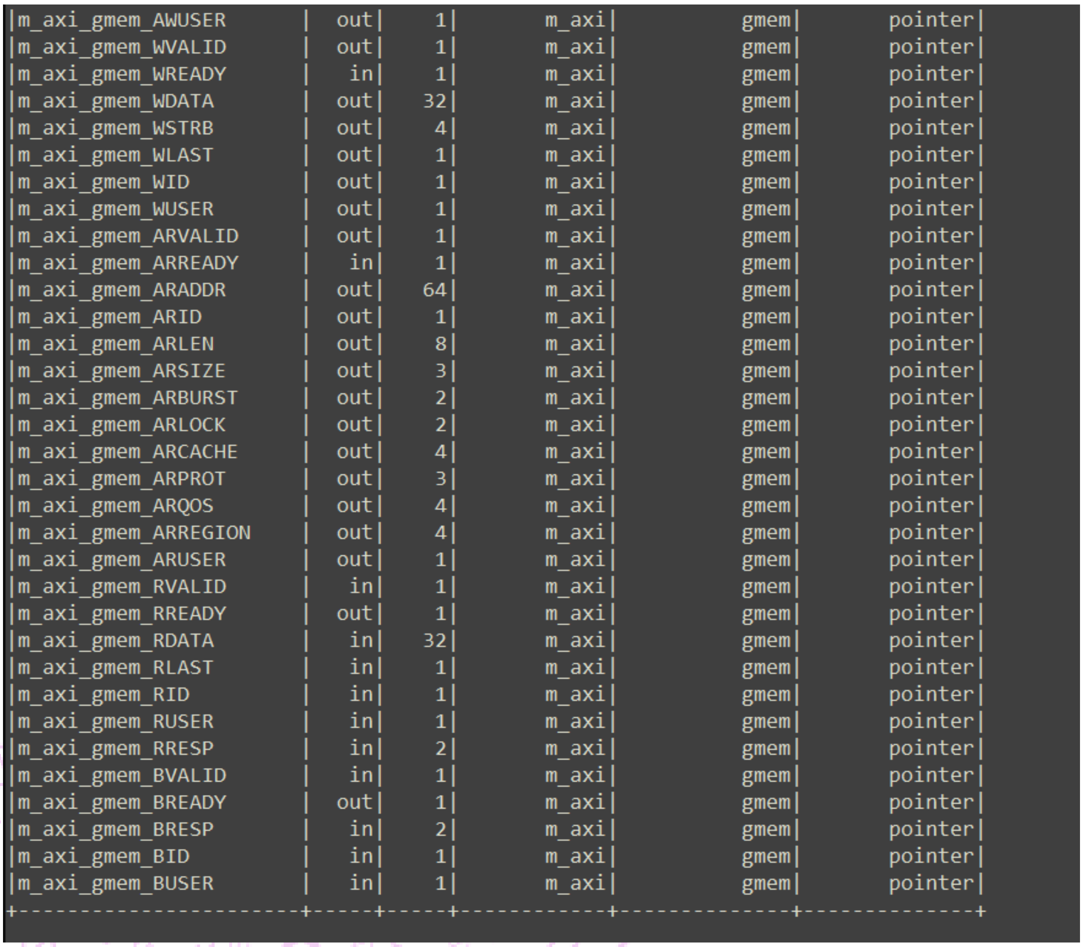


```
* TOP LEVEL CONTROL
+-----------+------------+-----------+
| Interface | Type       | Ports     |
+-----------+------------+-----------+
| ap_clk    | clock      | ap_clk    |
| ap_rst_n  | reset      | ap_rst_n  |
| interrupt | interrupt  | interrupt |
| ap_ctrl   | ap_ctrl_hs |           |
+-----------+------------+-----------+
```

2. Synthesis Detail Report

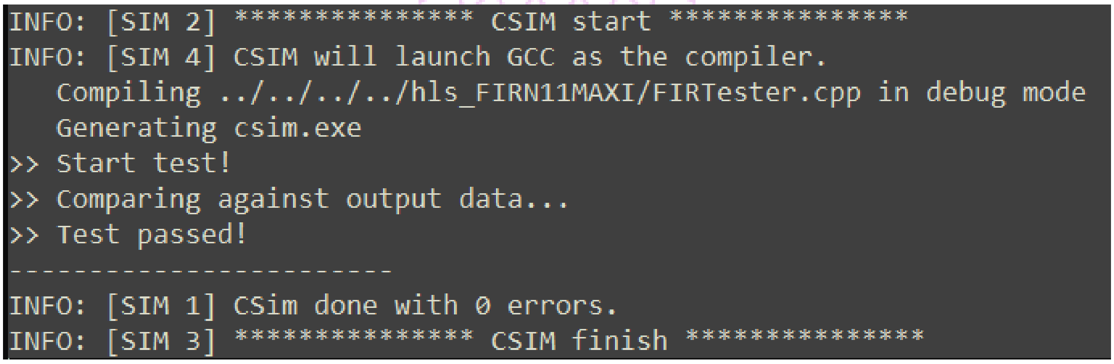


```
================================================================
== Interface
================================================================
* Summary:
+------------------------+-----+-----+------------+--------------+--------------+
|        RTL Ports       | Dir | Bits|  Protocol  | Source Object|    C Type    |
+------------------------+-----+-----+------------+--------------+--------------+
|s_axi_control_AWVALID   |   in|    1|       s_axi|       control|         array|
|s_axi_control_AWREADY   |  out|    1|       s_axi|       control|         array|
|s_axi_control_AWADDR    |   in|    7|       s_axi|       control|         array|
|s_axi_control_WVALID    |   in|    1|       s_axi|       control|         array|
|s_axi_control_WREADY    |  out|    1|       s_axi|       control|         array|
|s_axi_control_WDATA     |   in|   32|       s_axi|       control|         array|
|s_axi_control_WSTRB     |   in|    4|       s_axi|       control|         array|
|s_axi_control_ARVALID   |   in|    1|       s_axi|       control|         array|
|s_axi_control_ARREADY   |  out|    1|       s_axi|       control|         array|
|s_axi_control_ARADDR    |   in|    7|       s_axi|       control|         array|
|s_axi_control_RVALID    |  out|    1|       s_axi|       control|         array|
|s_axi_control_RREADY    |   in|    1|       s_axi|       control|         array|
|s_axi_control_RDATA     |  out|   32|       s_axi|       control|         array|
|s_axi_control_RRESP     |  out|    2|       s_axi|       control|         array|
|s_axi_control_BVALID    |  out|    1|       s_axi|       control|         array|
|s_axi_control_BREADY    |   in|    1|       s_axi|       control|         array|
|s_axi_control_BRESP     |  out|    2|       s_axi|       control|         array|
|ap_clk                  |   in|    1|   ap_ctrl_hs|   fir_n11_maxi|  return value|
|ap_rst_n                |   in|    1|   ap_ctrl_hs|   fir_n11_maxi|  return value|
|interrupt               |  out|    1|   ap_ctrl_hs|   fir_n11_maxi|  return value|
|m_axi_gmem_AWVALID      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWREADY      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWADDR       |  out|   64|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWID         |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWLEN        |  out|    8|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWSIZE       |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWBURST      |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWLOCK       |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWCACHE      |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWPROT       |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWQOS        |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWREGION     |  out|    4|       m_axi|          gmem|       pointer|
```



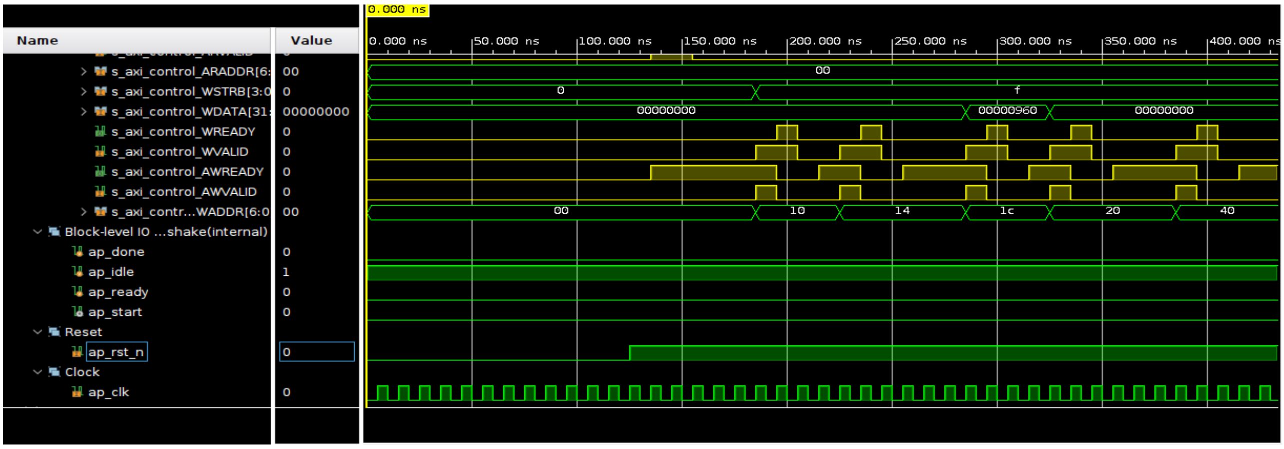
```
|m_axi_gmem_AWUSER      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WVALID      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WREADY      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WDATA       |  out|   32|       m_axi|          gmem|       pointer|
|m_axi_gmem_WSTRB       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_WLAST       |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WID         |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WUSER       |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARVALID     |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARREADY     |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARADDR      |  out|   64|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARID        |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARLEN       |  out|    8|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARSIZE      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARBURST     |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARLOCK      |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARCACHE     |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARPROT      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARQOS       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARREGION    |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARUSER      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RVALID      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RREADY      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RDATA       |   in|   32|       m_axi|          gmem|       pointer|
|m_axi_gmem_RLAST       |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RID         |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RUSER       |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RRESP       |   in|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_BVALID      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BREADY      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BRESP       |   in|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_BID         |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BUSER       |   in|    1|       m_axi|          gmem|       pointer|
+-----------------------+-----+-----+------------+--------------+--------------+
```

- Co-simulation transcript

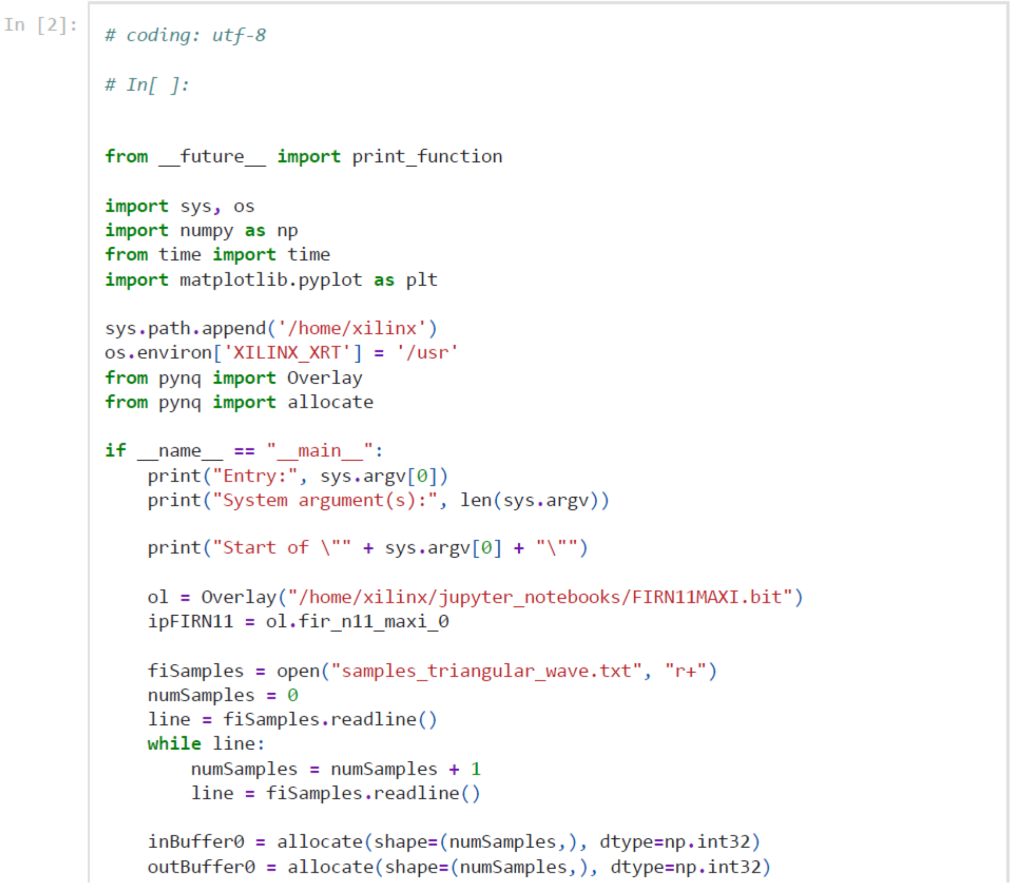


```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../hls_FIRN11MAXI/FIRTester.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

- Co-simulation waveform



- Jupyter Notebook execution results



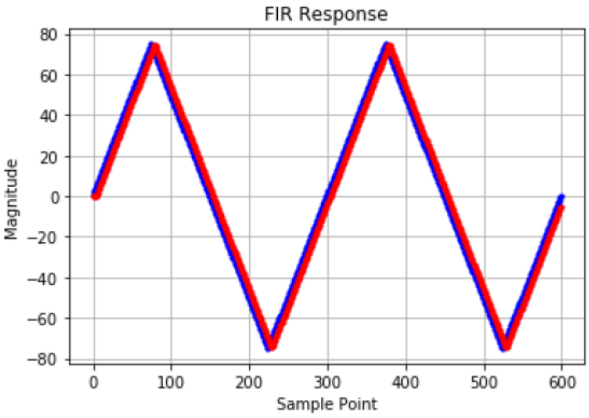
In [2]:

```
# coding: utf-8

# In[ ]:


from __future__ import print_function

import sys, os
import numpy as np
from time import time
import matplotlib.pyplot as plt

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay
from pynq import allocate

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("/home/xilinx/jupyter_notebooks/FIRN11MAXI.bit")
    ipFIRN11 = ol.fir_n11_maxi_0

    fiSamples = open("samples_triangular_wave.txt", "r+")
    numSamples = 0
    line = fiSamples.readline()
    while line:
        numSamples = numSamples + 1
        line = fiSamples.readline()

    inBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    outBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
```

```
fiSamples.seek(0)
for i in range(numSamples):
    line = fiSamples.readline()
    inBuffer0[i] = int(line)
fiSamples.close()

numTaps = 11
n32Taps = [0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0]
#n32Taps = [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1]
n32DCGain = 0
timeKernelStart = time()
for i in range(numTaps):
    n32DCGain = n32DCGain + n32Taps[i]
    ipFIRN11.write(0x40 + i * 4, n32Taps[i])
if n32DCGain < 0:
    n32DCGain = 0 - n32DCGain
ipFIRN11.write(0x28, len(inBuffer0) * 4)
ipFIRN11.write(0x10, inBuffer0.device_address)
ipFIRN11.write(0x1C, outBuffer0.device_address)
ipFIRN11.write(0x00, 0x01)
while (ipFIRN11.read(0x00) & 0x4) == 0x0:
    continue
timeKernelEnd = time()
print("Kernel execution time: " + str(timeKernelEnd - timeKernelStart) + " s")

plt.title("FIR Response")
plt.xlabel("Sample Point")
```

```
plt.ylabel("Magnitude")
xSeq = range(len(inBuffer0))
if n32DCGain == 0:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
else:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
plt.grid(True)
plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

print("============================")
print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.
py"
Kernel execution time: 0.0005536079406738281 s
```

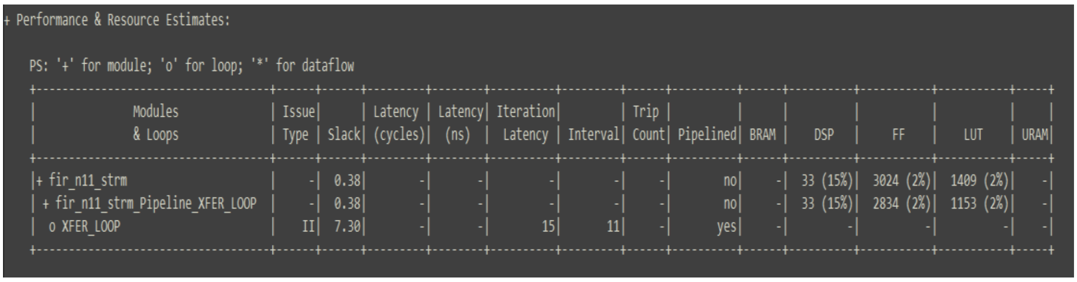


```
============================
Exit process
```

☆ Stream Interface

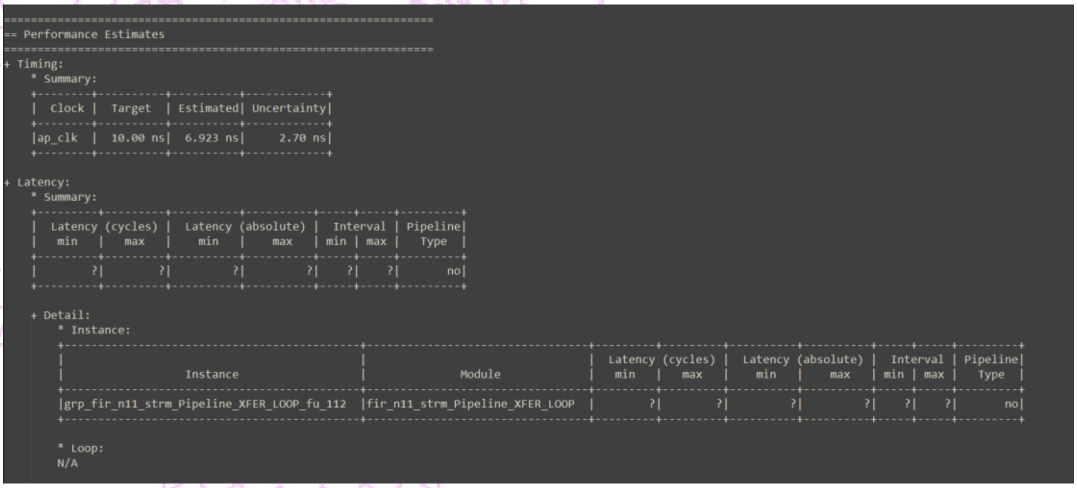
▪ Performance

1. Synthesis Summary Report



```
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow

    +---------------------------------+-----+-----+--------+-------+---------+--------+-----+---------+-----+---------+----------+----------+-----+
    |             Modules             |Issue|     |Latency |Latency|Iteration|        |Trip |         |     |         |          |          |     |
    |             & Loops             |Type |Slack|(cycles)| (ns)  | Latency |Interval|Count|Pipelined|BRAM |   DSP   |    FF    |   LUT    |URAM |
    +---------------------------------+-----+-----+--------+-------+---------+--------+-----+---------+-----+---------+----------+----------+-----+
    |+ fir_n11_strm                   |    -| 0.38|       -|      -|        -|       -|    -|       no|    -| 33 (15%)| 3024 (2%)| 1409 (2%)|    -|
    | + fir_n11_strm_Pipeline_XFER_LOOP|    -| 0.38|       -|      -|        -|       -|    -|       no|    -| 33 (15%)| 2834 (2%)| 1153 (2%)|    -|
    |  o XFER_LOOP                    |   II| 7.30|       -|      -|       15|      11|    -|      yes|    -|        -|         -|         -|    -|
    +---------------------------------+-----+-----+--------+-------+---------+--------+-----+---------+-----+---------+----------+----------+-----+
```

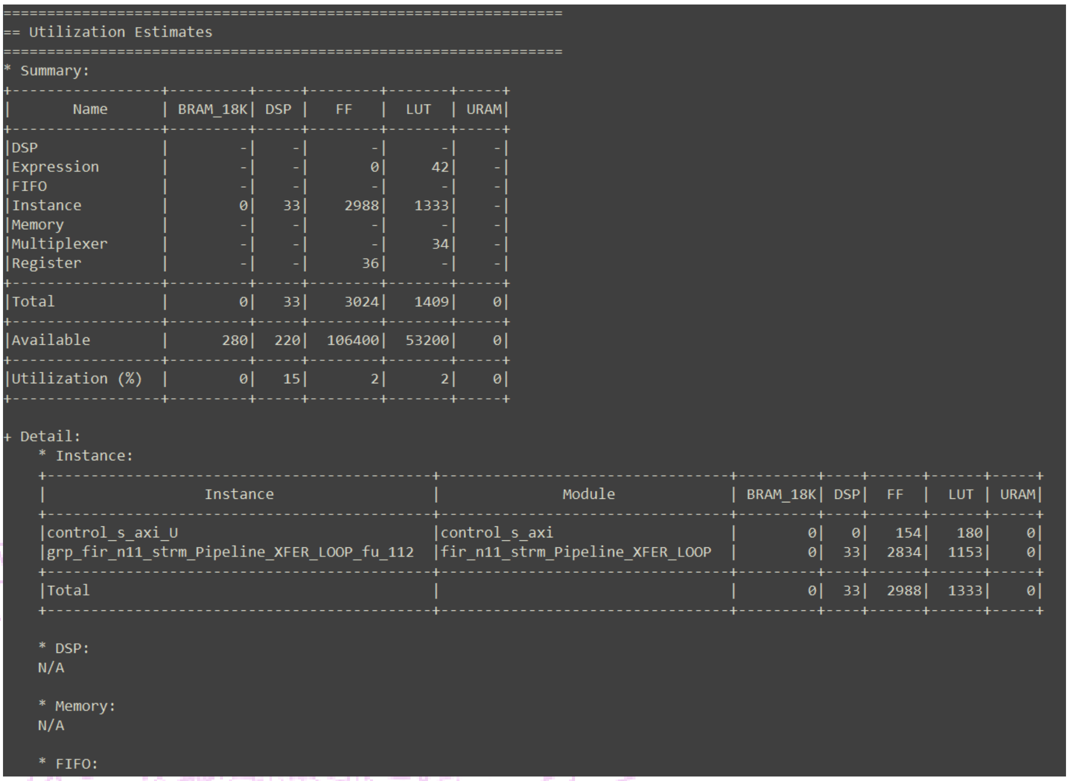
2. Synthesis Detail Report



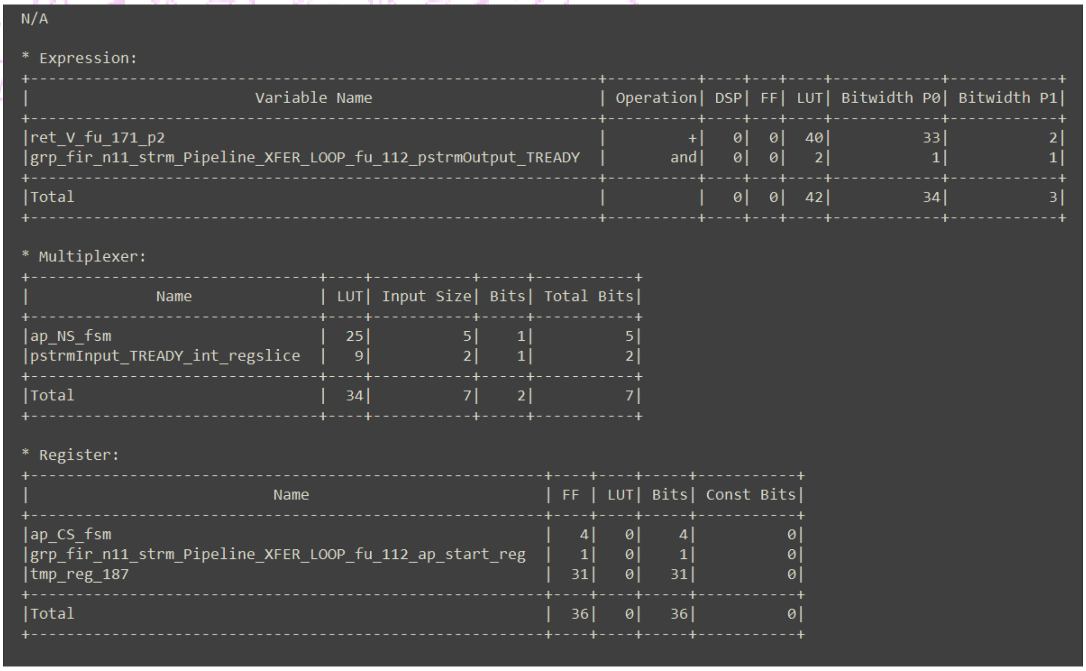
```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  6.923 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +----------------------------------------+------------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                        |                                    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |                Instance                |               Module               |   min   |   max   |    min   |    max   | min | max |   Type  |
        +----------------------------------------+------------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112  |fir_n11_strm_Pipeline_XFER_LOOP  |        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +----------------------------------------+------------------------------------+---------+---------+----------+----------+-----+-----+---------+

        * Loop:
        N/A
```

- # Utilization

1. Synthesis Detail Report



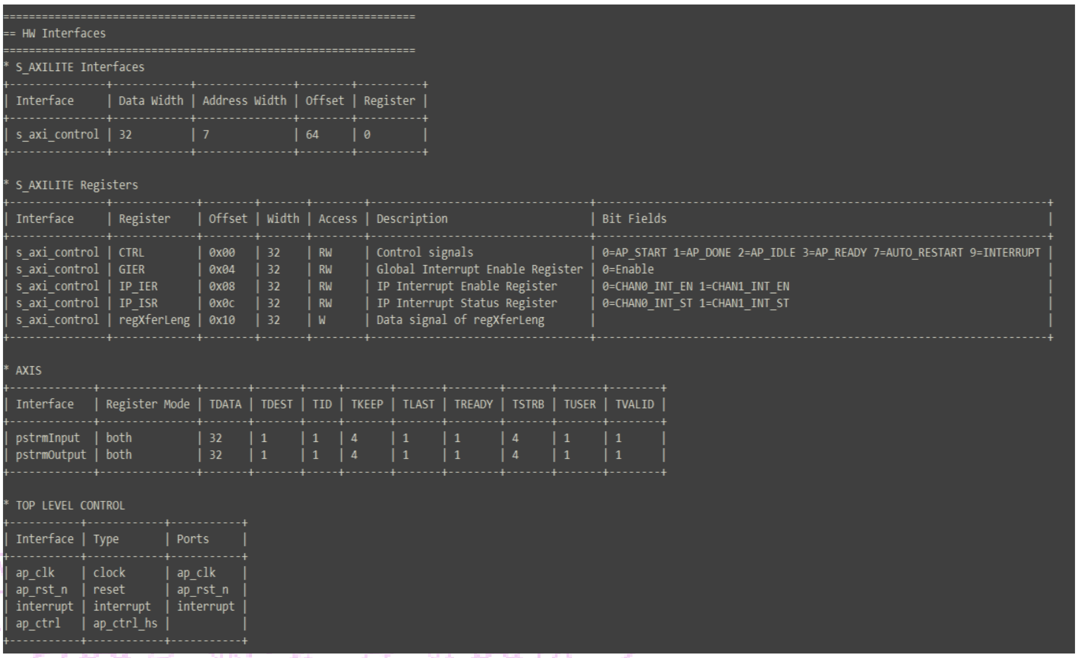
```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     42|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    2988|   1333|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|     34|    -|
|Register         |        -|    -|      36|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    3024|   1409|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       2|      2|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +---------------------------------------+----------------------------------+---------+----+------+------+-----+
    |                Instance               |              Module              | BRAM_18K| DSP|  FF  | LUT  | URAM|
    +---------------------------------------+----------------------------------+---------+----+------+------+-----+
    |control_s_axi_U                        |control_s_axi                     |        0|   0|   154|   180|    0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112  |fir_n11_strm_Pipeline_XFER_LOOP  |        0|  33|  2834|  1153|    0|
    +---------------------------------------+----------------------------------+---------+----+------+------+-----+
    |Total                                  |                                  |        0|  33|  2988|  1333|    0|
    +---------------------------------------+----------------------------------+---------+----+------+------+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
```



```
    N/A

    * Expression:
    +----------------------------------------------------------+----------+----+---+----+------------+------------+
    |                       Variable Name                      | Operation| DSP| FF| LUT| Bitwidth P0| Bitwidth P1|
    +----------------------------------------------------------+----------+----+---+----+------------+------------+
    |ret_V_fu_171_p2                                           |         +|   0|  0|  40|          33|           2|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_pstrmOutput_TREADY  |       and|   0|  0|   2|           1|           1|
    +----------------------------------------------------------+----------+----+---+----+------------+------------+
    |Total                                                     |          |   0|  0|  42|          34|           3|
    +----------------------------------------------------------+----------+----+---+----+------------+------------+

    * Multiplexer:
    +-------------------------------+----+-----------+-----+-----------+
    |              Name             | LUT| Input Size| Bits| Total Bits|
    +-------------------------------+----+-----------+-----+-----------+
    |ap_NS_fsm                      |  25|          5|    1|          5|
    |pstrmInput_TREADY_int_regslice |   9|          2|    1|          2|
    +-------------------------------+----+-----------+-----+-----------+
    |Total                          |  34|          7|    2|          7|
    +-------------------------------+----+-----------+-----+-----------+

    * Register:
    +-----------------------------------------------------+----+----+-----+-----------+
    |                         Name                        | FF | LUT| Bits| Const Bits|
    +-----------------------------------------------------+----+----+-----+-----------+
    |ap_CS_fsm                                            |   4|   0|    4|          0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_ap_start_reg  |   1|   0|    1|          0|
    |tmp_reg_187                                          |  31|   0|   31|          0|
    +-----------------------------------------------------+----+----+-----+-----------+
    |Total                                                |  36|   0|   36|          0|
    +-----------------------------------------------------+----+----+-----+-----------+
```

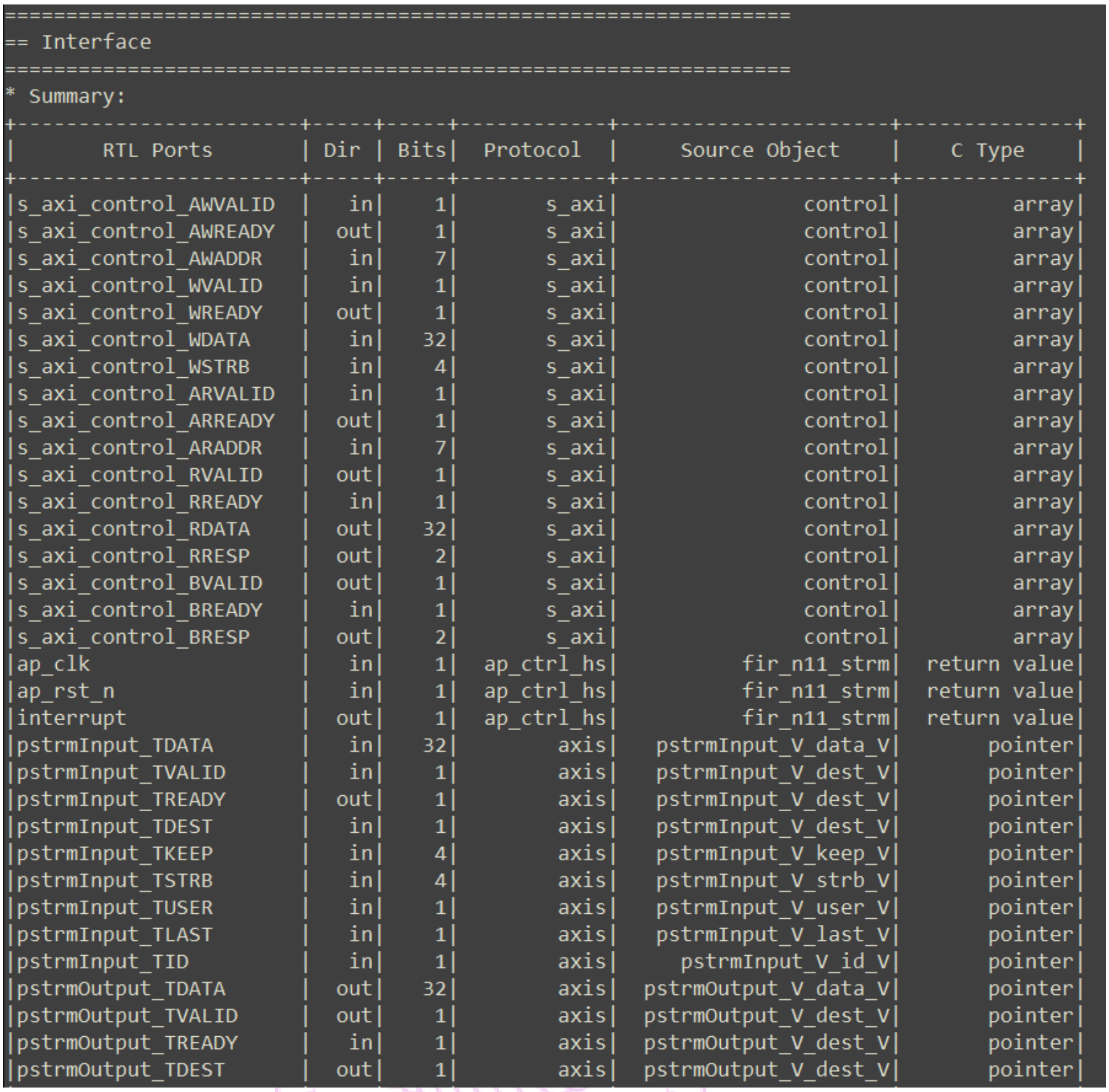
- Interface

1. Synthesis Summary Report

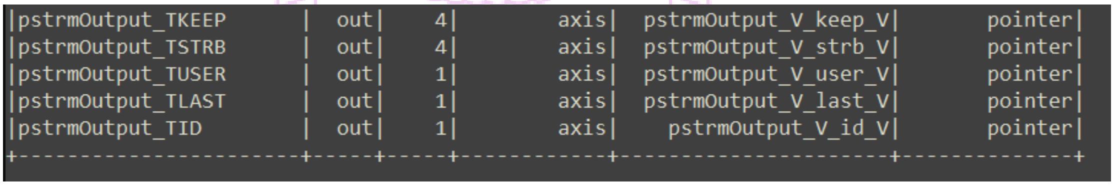


```
================================================================
== HW Interfaces
================================================================
* S_AXILITE Interfaces
+---------------+------------+---------------+--------+----------+
| Interface     | Data Width | Address Width | Offset | Register |
+---------------+------------+---------------+--------+----------+
| s_axi_control | 32         | 7             | 64     | 0        |
+---------------+------------+---------------+--------+----------+

* S_AXILITE Registers
+---------------+-------------+--------+-------+--------+----------------------------------+----------------------------------------------------------------------+
| Interface     | Register    | Offset | Width | Access | Description                      | Bit Fields                                                           |
+---------------+-------------+--------+-------+--------+----------------------------------+----------------------------------------------------------------------+
| s_axi_control | CTRL        | 0x00   | 32    | RW     | Control signals                  | 0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT |
| s_axi_control | GIER        | 0x04   | 32    | RW     | Global Interrupt Enable Register | 0=Enable                                                             |
| s_axi_control | IP_IER      | 0x08   | 32    | RW     | IP Interrupt Enable Register     | 0=CHAN0_INT_EN 1=CHAN1_INT_EN                                        |
| s_axi_control | IP_ISR      | 0x0c   | 32    | RW     | IP Interrupt Status Register     | 0=CHAN0_INT_ST 1=CHAN1_INT_ST                                        |
| s_axi_control | regXferLeng | 0x10   | 32    | W      | Data signal of regXferLeng       |                                                                      |
+---------------+-------------+--------+-------+--------+----------------------------------+----------------------------------------------------------------------+

* AXIS
+-------------+---------------+-------+-------+-----+-------+-------+--------+-------+-------+--------+
| Interface   | Register Mode | TDATA | TDEST | TID | TKEEP | TLAST | TREADY | TSTRB | TUSER | TVALID |
+-------------+---------------+-------+-------+-----+-------+-------+--------+-------+-------+--------+
| pstrmInput  | both          | 32    | 1     | 1   | 4     | 1     | 1      | 4     | 1     | 1      |
| pstrmOutput | both          | 32    | 1     | 1   | 4     | 1     | 1      | 4     | 1     | 1      |
+-------------+---------------+-------+-------+-----+-------+-------+--------+-------+-------+--------+

* TOP LEVEL CONTROL
+-----------+------------+-----------+
| Interface | Type       | Ports     |
+-----------+------------+-----------+
| ap_clk    | clock      | ap_clk    |
| ap_rst_n  | reset      | ap_rst_n  |
| interrupt | interrupt  | interrupt |
| ap_ctrl   | ap_ctrl_hs |           |
+-----------+------------+-----------+
```

2. Synthesis Detail Report

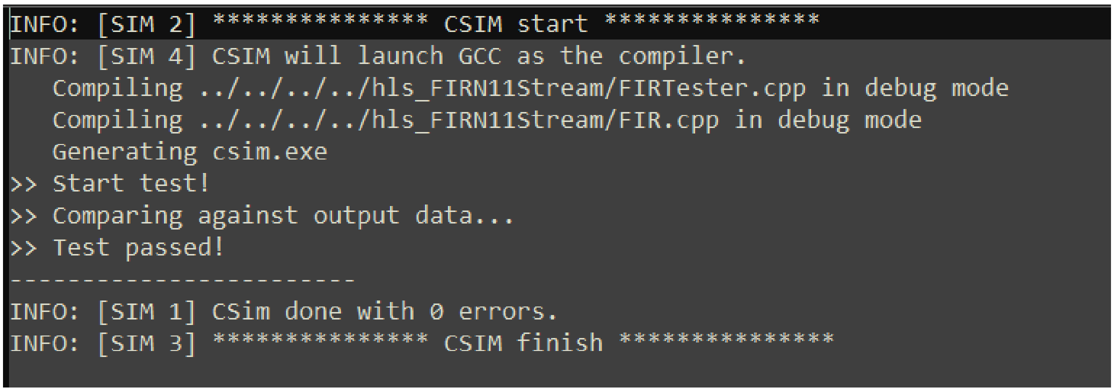


```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+----------------------+--------------+
|       RTL Ports       | Dir | Bits|  Protocol  |    Source Object     |    C Type    |
+-----------------------+-----+-----+------------+----------------------+--------------+
|s_axi_control_AWVALID  |   in|    1|       s_axi|               control|         array|
|s_axi_control_AWREADY  |  out|    1|       s_axi|               control|         array|
|s_axi_control_AWADDR   |   in|    7|       s_axi|               control|         array|
|s_axi_control_WVALID   |   in|    1|       s_axi|               control|         array|
|s_axi_control_WREADY   |  out|    1|       s_axi|               control|         array|
|s_axi_control_WDATA    |   in|   32|       s_axi|               control|         array|
|s_axi_control_WSTRB    |   in|    4|       s_axi|               control|         array|
|s_axi_control_ARVALID  |   in|    1|       s_axi|               control|         array|
|s_axi_control_ARREADY  |  out|    1|       s_axi|               control|         array|
|s_axi_control_ARADDR   |   in|    7|       s_axi|               control|         array|
|s_axi_control_RVALID   |  out|    1|       s_axi|               control|         array|
|s_axi_control_RREADY   |   in|    1|       s_axi|               control|         array|
|s_axi_control_RDATA    |  out|   32|       s_axi|               control|         array|
|s_axi_control_RRESP    |  out|    2|       s_axi|               control|         array|
|s_axi_control_BVALID   |  out|    1|       s_axi|               control|         array|
|s_axi_control_BREADY   |   in|    1|       s_axi|               control|         array|
|s_axi_control_BRESP    |  out|    2|       s_axi|               control|         array|
|ap_clk                 |   in|    1|  ap_ctrl_hs|          fir_n11_strm|  return value|
|ap_rst_n               |   in|    1|  ap_ctrl_hs|          fir_n11_strm|  return value|
|interrupt              |  out|    1|  ap_ctrl_hs|          fir_n11_strm|  return value|
|pstrmInput_TDATA       |   in|   32|        axis|    pstrmInput_V_data_V|       pointer|
|pstrmInput_TVALID      |   in|    1|        axis|    pstrmInput_V_dest_V|       pointer|
|pstrmInput_TREADY      |  out|    1|        axis|    pstrmInput_V_dest_V|       pointer|
|pstrmInput_TDEST       |   in|    1|        axis|    pstrmInput_V_dest_V|       pointer|
|pstrmInput_TKEEP       |   in|    4|        axis|    pstrmInput_V_keep_V|       pointer|
|pstrmInput_TSTRB       |   in|    4|        axis|    pstrmInput_V_strb_V|       pointer|
|pstrmInput_TUSER       |   in|    1|        axis|    pstrmInput_V_user_V|       pointer|
|pstrmInput_TLAST       |   in|    1|        axis|    pstrmInput_V_last_V|       pointer|
|pstrmInput_TID         |   in|    1|        axis|      pstrmInput_V_id_V|       pointer|
|pstrmOutput_TDATA      |  out|   32|        axis|   pstrmOutput_V_data_V|       pointer|
|pstrmOutput_TVALID     |  out|    1|        axis|   pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TREADY     |   in|    1|        axis|   pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TDEST      |  out|    1|        axis|   pstrmOutput_V_dest_V|       pointer|
```



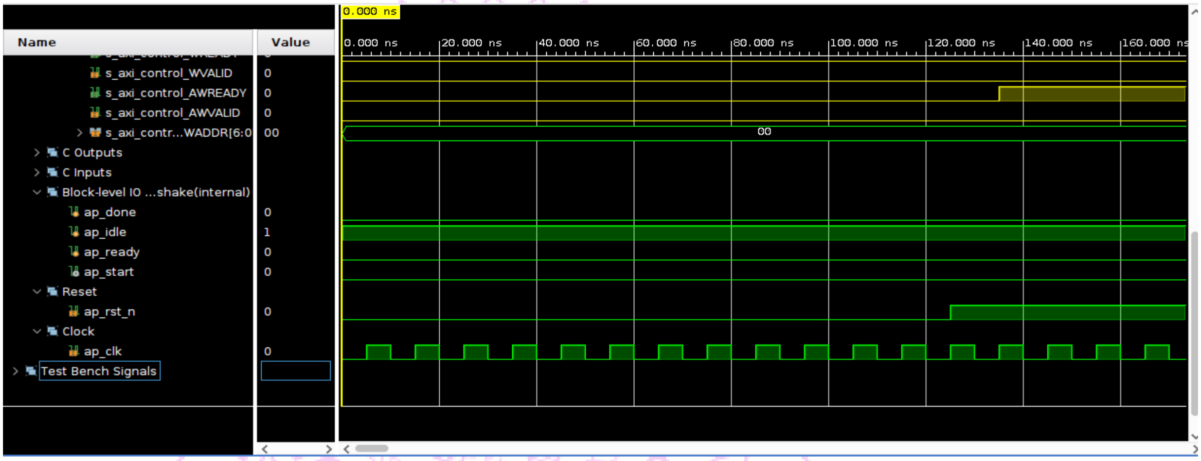
```
|pstrmOutput_TKEEP      |  out|    4|        axis|   pstrmOutput_V_keep_V|       pointer|
|pstrmOutput_TSTRB      |  out|    4|        axis|   pstrmOutput_V_strb_V|       pointer|
|pstrmOutput_TUSER      |  out|    1|        axis|   pstrmOutput_V_user_V|       pointer|
|pstrmOutput_TLAST      |  out|    1|        axis|   pstrmOutput_V_last_V|       pointer|
|pstrmOutput_TID        |  out|    1|        axis|     pstrmOutput_V_id_V|       pointer|
+-----------------------+-----+-----+------------+----------------------+--------------+
```

- Co-simulation transcript

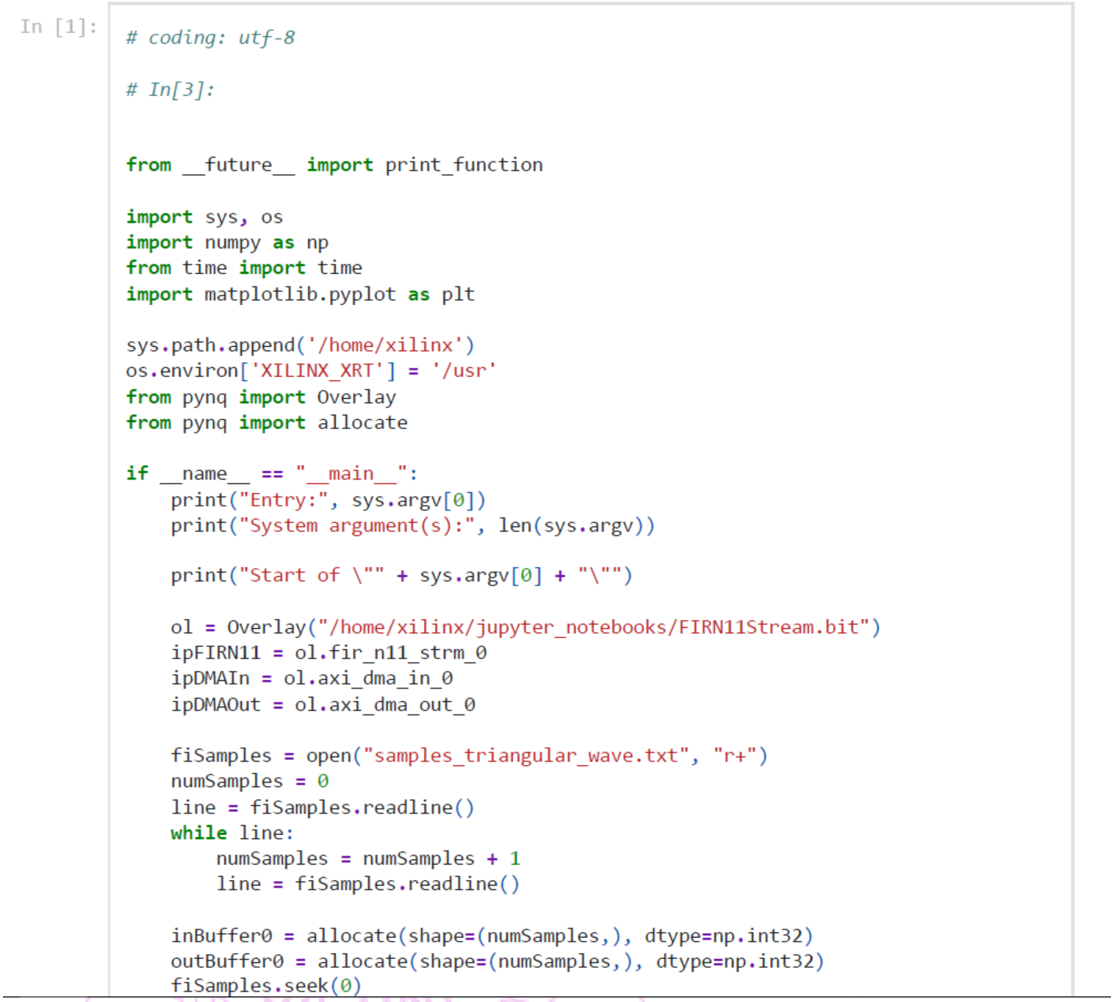


```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../hls_FIRN11Stream/FIRTester.cpp in debug mode
   Compiling ../../../../hls_FIRN11Stream/FIR.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

- Co-simulation waveform



- Jupyter Notebook execution results

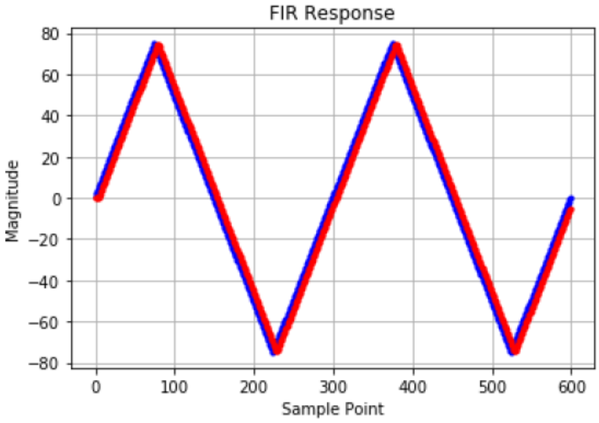


In [1]:

```
# coding: utf-8

# In[3]:


from __future__ import print_function

import sys, os
import numpy as np
from time import time
import matplotlib.pyplot as plt

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay
from pynq import allocate

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("/home/xilinx/jupyter_notebooks/FIRN11Stream.bit")
    ipFIRN11 = ol.fir_n11_strm_0
    ipDMAIn = ol.axi_dma_in_0
    ipDMAOut = ol.axi_dma_out_0

    fiSamples = open("samples_triangular_wave.txt", "r+")
    numSamples = 0
    line = fiSamples.readline()
    while line:
        numSamples = numSamples + 1
        line = fiSamples.readline()

    inBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    outBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    fiSamples.seek(0)
    for i in range(numSamples):
        line = fiSamples.readline()
        inBuffer0[i] = int(line)
    fiSamples.close()

    numTaps = 11
    n32Taps = [0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0]
    #n32Taps = [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1]
    n32DCGain = 0
    timeKernelStart = time()
    for i in range(numTaps):
        n32DCGain = n32DCGain + n32Taps[i]
        ipFIRN11.write(0x40 + i * 4, n32Taps[i])
    if n32DCGain < 0:
        n32DCGain = 0 - n32DCGain
    ipFIRN11.write(0x10, len(inBuffer0) * 4)
    ipFIRN11.write(0x00, 0x01)
    ipDMAIn.sendchannel.transfer(inBuffer0)
    ipDMAOut.recvchannel.transfer(outBuffer0)
    ipDMAIn.sendchannel.wait()
    ipDMAOut.recvchannel.wait()
    timeKernelEnd = time()
    print("Kernel execution time: " + str(timeKernelEnd - timeKernelStart) + " s")
```

```
    plt.title("FIR Response")
    plt.xlabel("Sample Point")
    plt.ylabel("Magnitude")
    xSeq = range(len(inBuffer0))
    if n32DCGain == 0:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
    else:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
    plt.grid(True)

    plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

    print("============================")
    print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.
py"
Kernel execution time: 0.0016922950744628906 s
```



```
============================
Exit process
```