

國立清華大學 電機工程系
112 學年度第二學期

Advanced SOC Design Laboratory

Low power design



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中華民國一一三年六月

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1. Odyssey:

- Clock gating

- DC side:

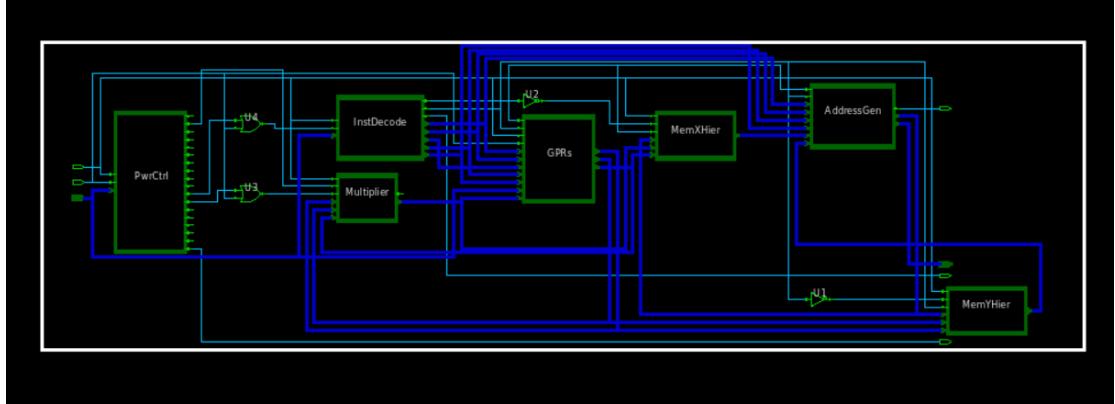


Fig. 1. Design view after compile.

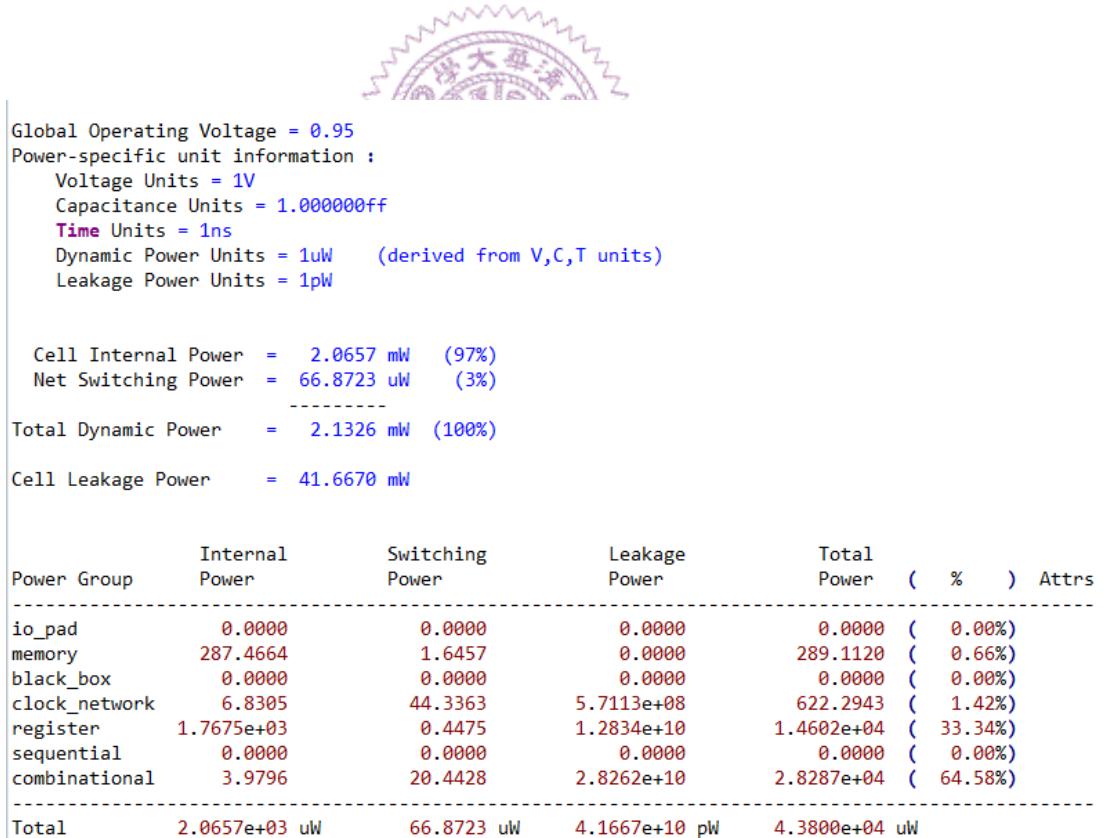


Fig. 2. Report of power.

```
*****
Report : area
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 21:20:45 2024
*****  

Information: Updating design information... (UID-85)  

Library(s) Used:  

    saed32sram_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_tt1p05v25c.db)  

    saed32rvt_ff0p85v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ff0p85v125c.db)  

Number of ports:          4187  

Number of nets:           10924  

Number of cells:          6998  

Number of combinational cells: 5399  

Number of sequential cells: 753  

Number of macros/black boxes: 4  

Number of buf/inv:         1268  

Number of references:      9  

Combinational area:       14525.854538  

Buf/Inv area:             2246.124758  

Noncombinational area:     5315.675997  

Macro/Black Box area:      109409.210938  

Net Interconnect area:     5886.323972  

Total cell area:          129250.741473  

Total area:                135137.065444
```

Fig. 3. Report of area.



```
*****
Report : timing
    -path full
    -delay max
    -max_paths 1
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 21:20:45 2024
*****
```

Operating Conditions: ss0p95v125c Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed

Startpoint: GPRs/B_reg_reg_3_
(rising edge-triggered flip-flop clocked by clock)
Endpoint: Multiplier/S_reg_reg_31_
(rising edge-triggered flip-flop clocked by clock)
Path Group: CLOCK
Path Type: max

Des/Clust/Port	Wire Load Model	Library
GeneralPurposeRegisters		
	16000	saed32rvt_ff0p85v125c
ChipTop	140000	saed32rvt_ff0p85v125c
GenPP_32Bits	8000	saed32rvt_ff0p85v125c
Mult_32x32	16000	saed32rvt_ff0p85v125c
CSA_nBits_width32_0	8000	saed32rvt_ff0p85v125c
PP_Add_32Bits	8000	saed32rvt_ff0p85v125c
CSA_nBits_width32_3	8000	saed32rvt_ff0p85v125c
CSA_nBits_width32_2	8000	saed32rvt_ff0p85v125c
CSA_nBits_width32_1	8000	saed32rvt_ff0p85v125c
CLA_4Bits_6	ForQA	saed32rvt_ff0p85v125c
CLA_16Bits_0	8000	saed32rvt_ff0p85v125c
CLA_Gen_4Bits_0	ForQA	saed32rvt_ff0p85v125c
CLA_32Bit_Adder	8000	saed32rvt_ff0p85v125c
CLA_16Bits_1	8000	saed32rvt_ff0p85v125c
CLA_4Bits_1	ForQA	saed32rvt_ff0p85v125c
Point		
clock clock (rise edge)	0.00	0.00
clock network delay (ideal)	1.50	1.50

GPRs/B_reg_reg_3_/CLK (DFFSSRX1_RVT)	0.00	1.50	r
GPRs/B_reg_reg_3_/Q (DFFSSRX1_RVT)	0.13	1.63	f
GPRs/B[3] (GeneralPurposeRegisters)	0.00	1.63	f
Multiplier/Y[3] (Mult_32x32)	0.00	1.63	f
Multiplier/GENPP/iso_Y[3] (GenPP_32Bits)	0.00	1.63	f
Multiplier/GENPP/U582/Y (OR2X1_RVT)	0.03	1.66	f
Multiplier/GENPP/U654/Y (INVX1_RVT)	0.01	1.67	r
Multiplier/GENPP/U583/Y (A021X1_RVT)	0.03	1.70	r
Multiplier/GENPP/U587/Y (AND2X1_RVT)	0.03	1.73	r
Multiplier/GENPP/U301/Y (NBUFFX2_RVT)	0.02	1.75	r
Multiplier/GENPP/U300/Y (NBUFFX2_RVT)	0.03	1.79	r
Multiplier/GENPP/U589/Y (A022X1_RVT)	0.04	1.83	r
Multiplier/GENPP/U590/Y (A0221X1_RVT)	0.05	1.88	r
Multiplier/GENPP/PP2[1] (GenPP_32Bits)	0.00	1.88	r
Multiplier/ADDPP/PP2[1] (PP_Add_32Bits)	0.00	1.88	r
Multiplier/ADDPP/CSA10/X[5] (CSA_nBits_width32_0)	0.00	1.88	r
Multiplier/ADDPP/CSA10/U63/Y (XNOR3X1_RVT)	0.12	2.00	r
Multiplier/ADDPP/CSA10/U72/Y (INVX1_RVT)	0.01	2.01	f
Multiplier/ADDPP/CSA10/U117/Y (OR2X1_RVT)	0.03	2.04	f
Multiplier/ADDPP/CSA10/U116/Y (A022X1_RVT)	0.03	2.07	f
Multiplier/ADDPP/CSA10/C[6] (CSA_nBits_width32_0)	0.00	2.07	f
Multiplier/ADDPP/CSA20/X[6] (CSA_nBits_width32_3)	0.00	2.07	f
Multiplier/ADDPP/CSA20/U63/Y (XNOR3X1_RVT)	0.11	2.19	f
Multiplier/ADDPP/CSA20/U74/Y (INVX1_RVT)	0.02	2.20	r
Multiplier/ADDPP/CSA20/U112/Y (A022X1_RVT)	0.05	2.25	r
Multiplier/ADDPP/CSA20/C[7] (CSA_nBits_width32_3)	0.00	2.25	r
Multiplier/ADDPP/CSA30/X[7] (CSA_nBits_width32_2)	0.00	2.25	r
Multiplier/ADDPP/CSA30/U36/Y (XNOR3X2_RVT)	0.10	2.35	r
Multiplier/ADDPP/CSA30/U72/Y (INVX1_RVT)	0.01	2.36	f
Multiplier/ADDPP/CSA30/U108/Y (A022X1_RVT)	0.04	2.41	f
Multiplier/ADDPP/CSA30/C[8] (CSA_nBits_width32_2)	0.00	2.41	f
Multiplier/ADDPP/CSA40/X[8] (CSA_nBits_width32_1)	0.00	2.41	f
Multiplier/ADDPP/CSA40/U35/Y (XNOR3X1_RVT)	0.11	2.52	f
Multiplier/ADDPP/CSA40/U77/Y (INVX1_RVT)	0.02	2.54	r
Multiplier/ADDPP/CSA40/U104/Y (A022X1_RVT)	0.06	2.59	r
Multiplier/ADDPP/CSA40/C[9] (CSA_nBits_width32_1)	0.00	2.59	r
Multiplier/ADDPP/CLA1/B[9] (CLA_32Bit_Adder)	0.00	2.59	r
Multiplier/ADDPP/CLA1/BITS15_0/B[9] (CLA_16Bits_0)	0.00	2.59	r
Multiplier/ADDPP/CLA1/BITS15_0/BITS118/B[1] (CLA_4Bits_6)	0.00	2.59	r
Multiplier/ADDPP/CLA1/BITS15_0/BITS118/U16/Y (OR2X1_RVT)	0.04	2.63	r
Multiplier/ADDPP/CLA1/BITS15_0/BITS118/U15/Y (AND2X1_RVT)	0.03	2.66	r
Multiplier/ADDPP/CLA1/BITS15_0/BITS118/U14/Y (A022X1_RVT)	0.03	2.69	r
Multiplier/ADDPP/CLA1/BITS15_0/BITS118/U12/Y (A022X1_RVT)	0.03	2.73	r

Multiplier/ADDP(CL1/BITS15_0/BITS118/U10/Y (A022X1_RVT)	0.04	2.76 r
Multiplier/ADDP(CL1/BITS15_0/BITS118/GP (CLA_4Bits_6)	0.00	2.76 r
Multiplier/ADDP(CL1/BITS15_0/GEN150/GP[2] (CLA_Gen_4Bits_0)	0.00	2.76 r
Multiplier/ADDP(CL1/BITS15_0/GEN150/U3/Y (A021X1_RVT)	0.03	2.79 r
Multiplier/ADDP(CL1/BITS15_0/GEN150/U2/Y (A021X1_RVT)	0.04	2.83 r
Multiplier/ADDP(CL1/BITS15_0/GEN150/GPP (CLA_Gen_4Bits_0)	0.00	2.83 r
Multiplier/ADDP(CL1/BITS15_0/GPP (CLA_16Bits_0)	0.00	2.83 r
Multiplier/ADDP(CL1/GEN31_0/GP[0] (CLA_Gen_2Bits)	0.00	2.83 r
Multiplier/ADDP(CL1/GEN31_0/U3/Y (A021X1_RVT)	0.03	2.87 r
Multiplier/ADDP(CL1/GEN31_0/C4 (CLA_Gen_2Bits)	0.00	2.87 r
Multiplier/ADDP(CL1/BITS31_16/CI (CLA_16Bits_1)	0.00	2.87 r
Multiplier/ADDP(CL1/BITS31_16/GEN150/CI (CLA_Gen_4Bits_1)	0.00	2.87 r
Multiplier/ADDP(CL1/BITS31_16/GEN150/U7/Y (A021X1_RVT)	0.05	2.91 r
Multiplier/ADDP(CL1/BITS31_16/GEN150/U6/Y (A021X1_RVT)	0.05	2.96 r
Multiplier/ADDP(CL1/BITS31_16/GEN150/U5/Y (A021X1_RVT)	0.05	3.01 r
Multiplier/ADDP(CL1/BITS31_16/GEN150/C12 (CLA_Gen_4Bits_1)	0.00	3.01 r
Multiplier/ADDP(CL1/BITS31_16/BITS1512/CI (CLA_4Bits_1)	0.00	3.01 r
Multiplier/ADDP(CL1/BITS31_16/BITS1512/U7/Y (A022X1_RVT)	0.04	3.05 r
Multiplier/ADDP(CL1/BITS31_16/BITS1512/U6/Y (A022X1_RVT)	0.04	3.09 r
Multiplier/ADDP(CL1/BITS31_16/BITS1512/U2/Y (AOI22X1_RVT)	0.05	3.14 f
Multiplier/ADDP(CL1/BITS31_16/BITS1512/U1/Y (XNOR3X1_RVT)	0.04	3.18 r
Multiplier/ADDP(CL1/BITS31_16/BITS1512/S[3] (CLA_4Bits_1)	0.00	3.18 r
Multiplier/ADDP(CL1/BITS31_16/S[15] (CLA_16Bits_1)	0.00	3.18 r
Multiplier/ADDP(CL1/S[31] (CLA_32Bit_Adder)	0.00	3.18 r
Multiplier/ADDP/Sum[31] (PP_Add_32Bits)	0.00	3.18 r
Multiplier/S_reg_reg_31_/D (DFFSSRX1_RVT)	0.00	3.18 r
data arrival time		3.18
clock clock (rise edge)	7.00	7.00
clock network delay (ideal)	1.50	8.50

clock uncertainty	-0.30	8.20
Multiplier/S_reg_reg_31_/CLK (DFFSSRX1_RVT)	0.00	8.20 r
library setup time	-0.12	8.08
data required time		8.08

data required time		8.08
data arrival time		-3.18

slack (MET)		4.90

Fig. 4. Report of timing.

```
*****
Report : clock_gating
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 21:20:37 2024
*****
```

Information: Identification of clock-gating cells has **not** been performed. Pre-existing clock-gating cells will **not** be reported. (PWR-947)

Clock Gating Summary	
Number of Clock gating elements	34
Number of Gated registers	719 (100.00%)
Number of Ungated registers	0 (0.00%)
Total number of registers	719

Clock Gating Report by Origin	
	Actual (%) Count
Number of tool-inserted Clock gating elements	34 (100.00%)
Number of pre-existing Clock gating elements	0 (0.00%)
Number of gated registers	719 (100.00%)
Number of tool-inserted gated registers	719 (100.00%)
Number of pre-existing gated registers	0 (0.00%)
Number of ungated registers	0 (0.00%)
Number of registers	719

Fig. 5. Report of clock gating.

- ICC side:

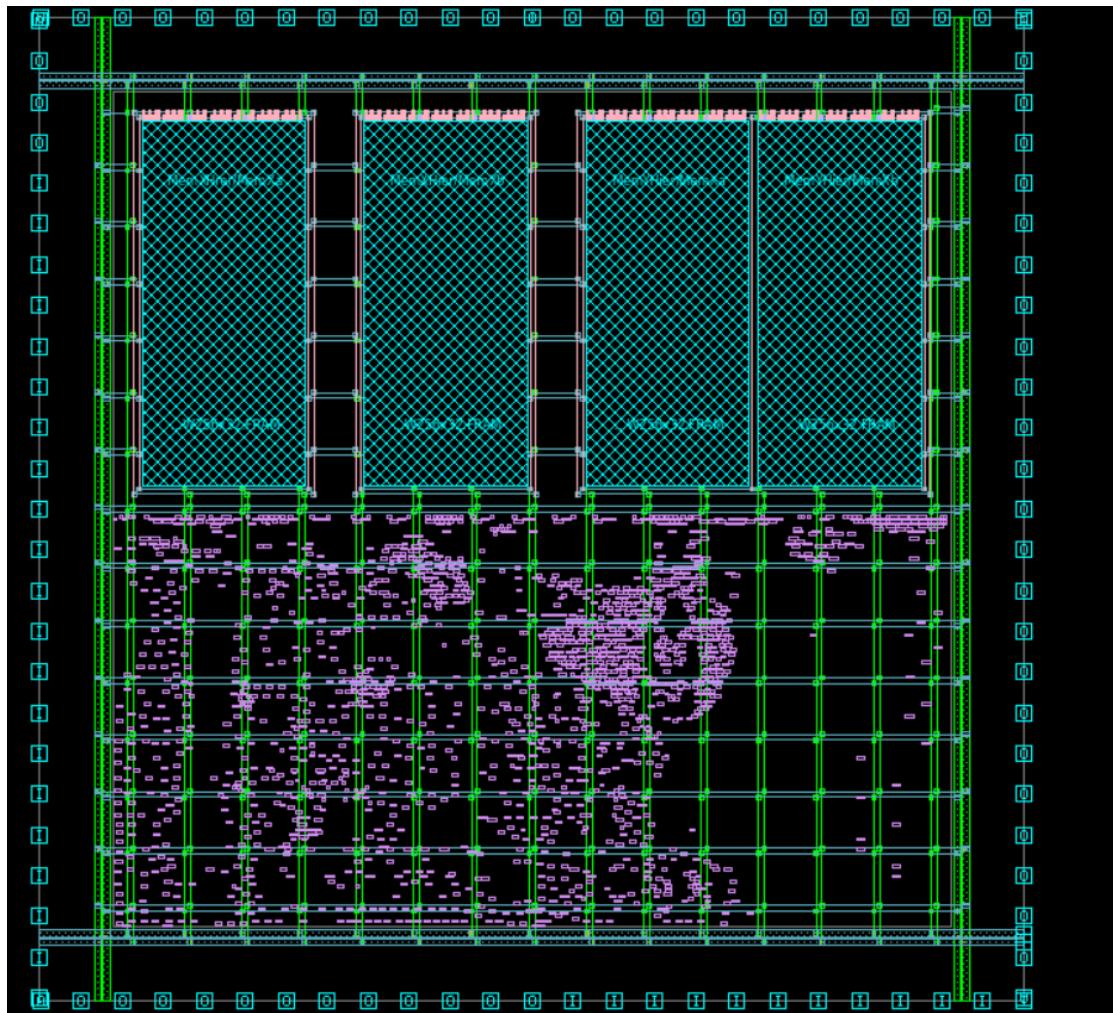


Fig. 6. Design view after compile.

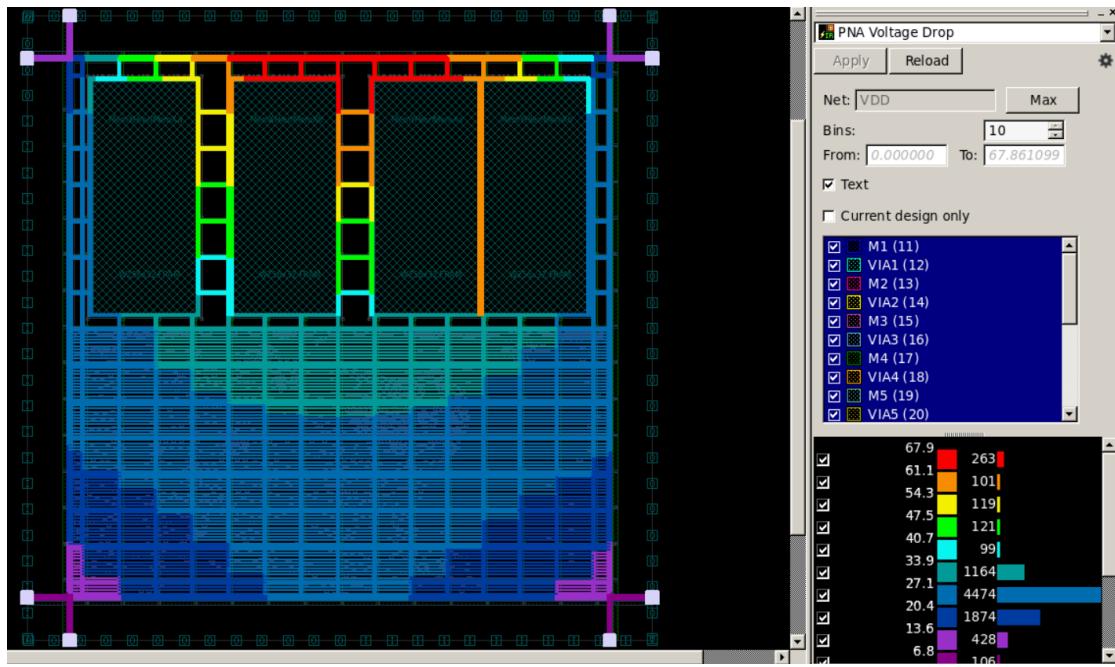


Fig. 7. Design view of leakage power density.

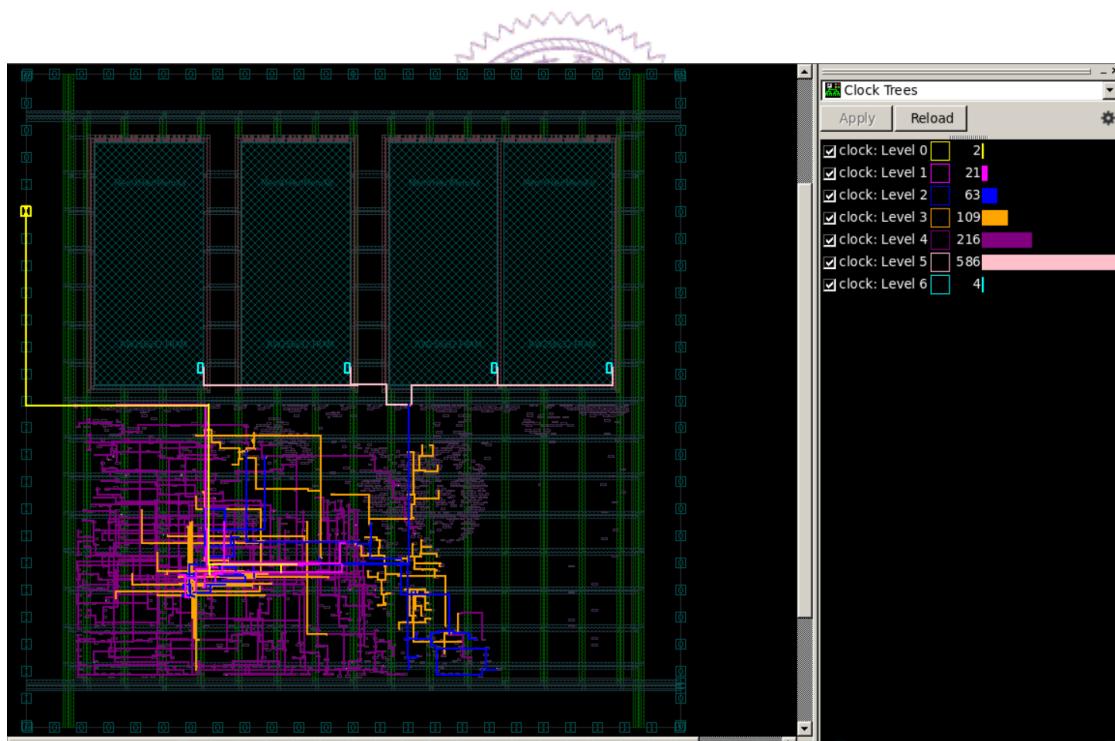


Fig. 8. Design view after CTS.

- **Multi voltage**

- DC side:

```
*****
Report : area
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 16:51:39 2024
*****  
  
Information: Updating design information... (UID-85)  
Library(s) Used:  
  
saed32rvt_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ss0p95v125c.db)  
saed32rvt_u1vl_ss0p95v125c_i0p7v (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_u1vl_ss0p95v125c_i0p7v.db)  
saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)  
saed32rvt_ss0p7v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ss0p7v125c.db)  
saed32rvt_d1vl_ss0p7v125c_i0p95v (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_d1vl_ss0p7v125c_i0p95v.db)  
  
Number of ports: 285  
Number of nets: 6307  
Number of cells: 5859  
Number of combinational cells: 5137  
Number of sequential cells: 710  
Number of macros/black boxes: 4  
Number of buf/inv: 955  
Number of references: 56  
  
Combinational area: 14010.450544  
Buf/Inv area: 1283.935495  
Noncombinational area: 5042.725338  
Macro/Black Box area: 109409.210938  
Net Interconnect area: 8706.528303  
  
Total cell area: 128462.386819  
Total area: 137168.915122
```

Fig. 9. Report of area.



Report : timing -path full -delay max -max_paths 1				
Design : ChipTop				
Version: R-2020.09-SP5				
Date : Sun Jun 23 16:51:39 2024				

Wire Load Model Mode: enclosed				
Startpoint: GPRs/B_reg_reg[4] (rising edge-triggered flip-flop clocked by clock)				
Endpoint: Multiplier/S_reg_reg[29] (rising edge-triggered flip-flop clocked by clock)				
Path Group: CLOCK				
Path Type: max				
Des/Clust/Port	Wire Load Model	Library	Point	Incr
-----	-----	-----	-----	-----
ChipTop	140000	saed32rvt_ss0p95v125c	clock clock (rise edge)	0.00
			clock network delay (ideal)	0.20
			GPRs/B_reg_reg[4]/CLK (DFFSSRX1_RVT)	0.00
			GPRs/B_reg_reg[4]/Q (DFFSSRX1_RVT)	0.56
			GPRs/B[4] (GeneralPurposeRegisters)	0.00
			LS_B[4]_UPF_LS/Y (LSUPX4_RVT)	0.24
			U1695/Y (OR2X1_RVT)	0.06
			U1514/Y (OR2X2_RVT)	0.11
			U1570/Y (INVX0_RVT)	0.04
			U2567/Y (A021X1_RVT)	0.08
			U1737/Y (OR2X1_RVT)	0.05
			U1736/Y (A021X1_RVT)	0.05
			U1524/Y (OR2X1_RVT)	0.05
			U1506/Y (INVX0_RVT)	0.03
			U1569/Y (OR2X2_RVT)	0.06
			U1568/Y (XOR2X2_RVT)	0.10
			U2559/Y (NOR2X0_RVT)	0.07
			U2684/Y (NOR2X0_RVT)	0.07
			U2685/Y (NOR2X0_RVT)	0.07
			U1649/Y (XNOR2X1_RVT)	0.12
			U1647/Y (INVX0_RVT)	0.02
			U2698/Y (AND2X1_RVT)	0.05
			U1930/Y (OR2X1_RVT)	0.05
			U2509/Y (XNOR2X2_RVT)	0.09
			U1639/Y (INVX0_RVT)	0.03

U1631/Y (OR2X1_RVT)	0.07	2.28 f	0.95
U1626/Y (XNOR2X1_RVT)	0.11	2.39 r	0.95
U1583/Y (XNOR2X2_RVT)	0.11	2.50 r	0.95
U1530/Y (OR2X2_RVT)	0.06	2.56 r	0.95
U3006/Y (AND2X1_RVT)	0.05	2.61 r	0.95
U3007/Y (AND3X1_RVT)	0.07	2.67 r	0.95
U1527/Y (OR2X2_RVT)	0.06	2.73 r	0.95
U1560/Y (OAI22X2_RVT)	0.08	2.82 f	0.95
U1706/Y (A021X1_RVT)	0.08	2.89 f	0.95
U2343/Y (A021X1_RVT)	0.05	2.94 f	0.95
U1532/Y (INVX1_RVT)	0.03	2.97 r	0.95
U2358/Y (A021X1_RVT)	0.08	3.05 r	0.95
U2354/Y (A021X1_RVT)	0.09	3.14 r	0.95
U2277/Y (NOR2X0_RVT)	0.07	3.21 f	0.95
U3344/Y (OR3X1_RVT)	0.07	3.28 f	0.95
U1554/Y (AOI21X1_RVT)	0.07	3.34 r	0.95
Multiplier/S_reg_reg[29]/D (DFFX1_RVT)	0.00	3.34 r	0.95
data arrival time		3.34	
clock clock (rise edge)	3.30	3.30	
clock network delay (ideal)	0.20	3.50	
clock uncertainty	-0.10	3.40	
Multiplier/S_reg_reg[29]/CLK (DFFX1_RVT)	0.00	3.40 r	
library setup time	-0.06	3.34	
data required time		3.34	

data required time		3.34	
data arrival time		-3.34	

slack (MET)		0.00	

Fig. 10. Report of timing.



```
*****
Report : power
          -analysis_effort low
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 16:51:39 2024
*****
```

Library(s) Used:

```
saed32rvt_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ss0p95v125c.db)
saed32rvt_ulv1_ss0p95v125c_i0p7v (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ulv1_ss0p95v125c_i0p7v.db)
saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)
saed32rvt_ss0p7v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ss0p7v125c.db)
saed32rvt_dl1v1_ss0p7v125c_i0p95 (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_dl1v1_ss0p7v125c_i0p95v.db)
```

Global Operating Voltage = 0.95
Power-specific unit information :
 Voltage Units = 1V
 Capacitance Units = 1.000000ff
 Time Units = 1ns
 Dynamic Power Units = 1uW (derived from V,C,T units)
 Leakage Power Units = 1pW

Cell Internal Power = 1.2692 mW (98%)
Net Switching Power = 32.5160 uW (2%)

Total Dynamic Power = 1.3017 mW (100%)
Cell Leakage Power = 616.4048 uW

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	148.7093	2.2901	0.0000	150.9994	(7.87%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	1.0835e+03	0.3640	1.2767e+08	1.2116e+03	(63.17%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	36.9246	29.8615	4.8874e+08	555.5220	(28.96%)	
Total	1.2692e+03 uW	32.5156 uW	6.1640e+08 pW	1.9181e+03 uW		

Fig. 11. Report of power.

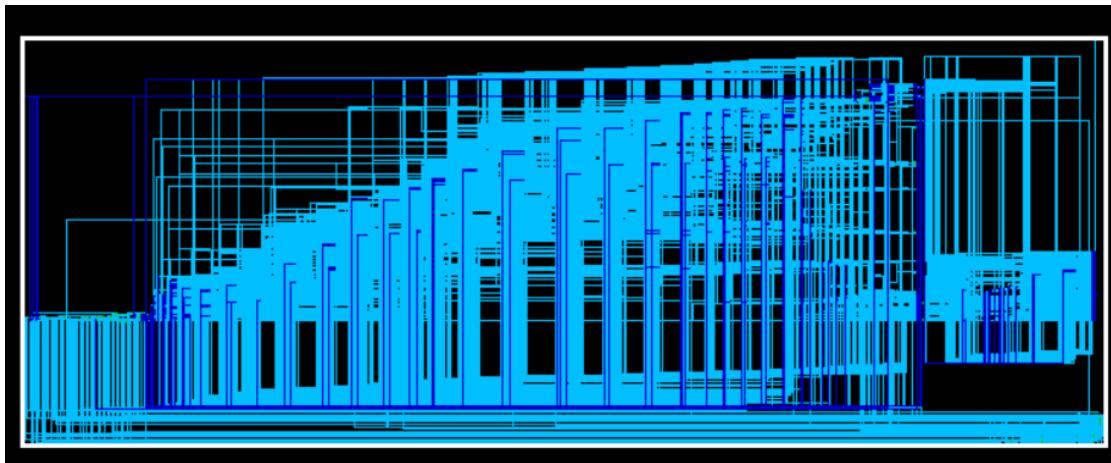


Fig. 12. Design view after compile_ultra.



- ICC side:

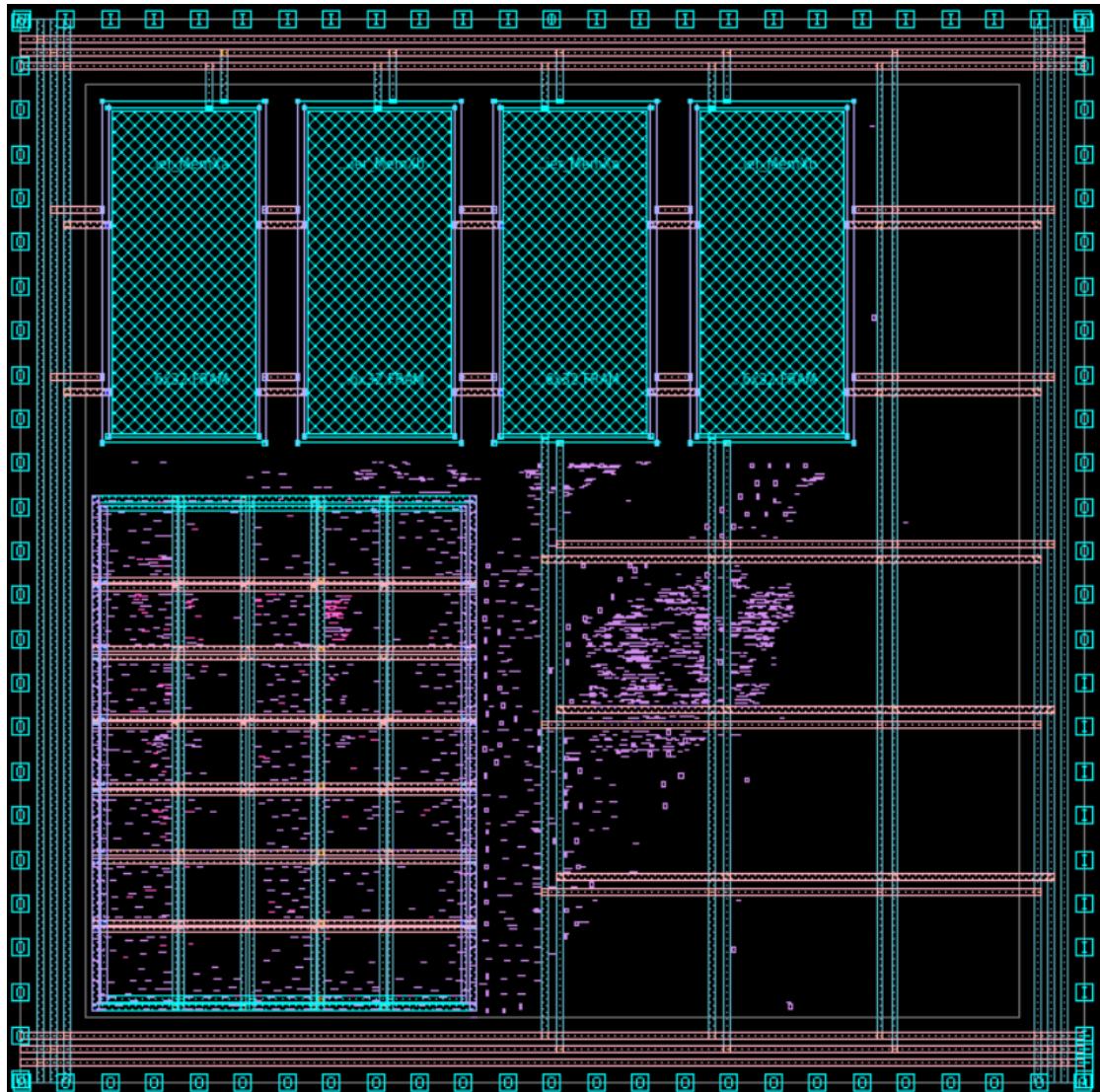


Fig. 13. Design view after creating power straps.



Fig. 14. Design view after CTS.

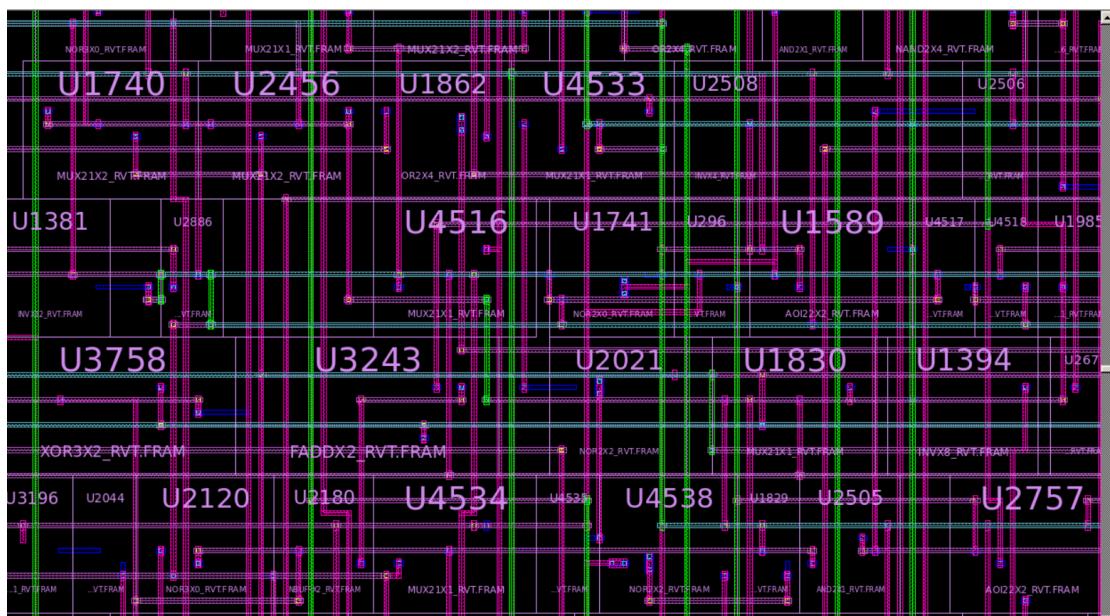


Fig. 15. Design view of standard cell routing.

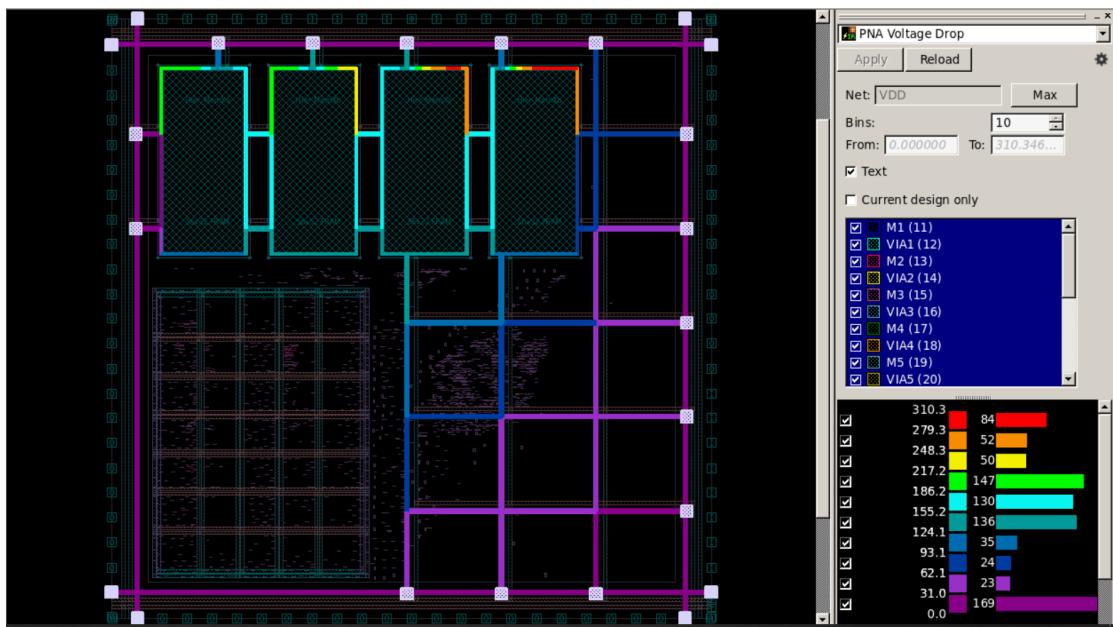


Fig. 16. Design view of leakage power density.

```
=====> TOTAL CELLS OUTPUT: 108 <=====  
write_gds completed successfully!  
1  
#close_mw_lib  
icc_shell> icc_shell>
```

Fig. 17. Terminal result (Successfully!).

- **Multi Vt**
 - DC side:

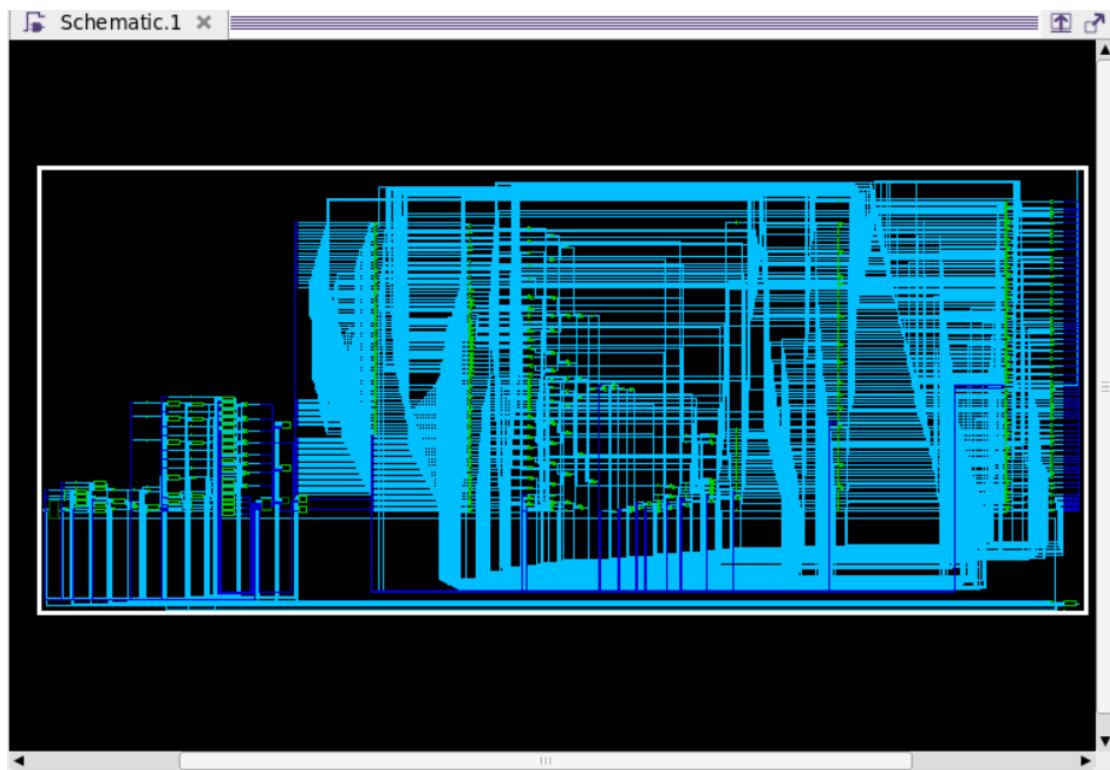


Fig. 18. Design view after compile_ultra.

```
*****
Report : power
    -analysis_effort low
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 18:40:26 2024
*****
Library(s) Used:
    saed32hvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_tt1p05v25c.db)
    saed32rvrt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvrt_tt1p05v25c.db)
    saed32sriram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sriram_ss0p95v125c.db)
Operating Conditions: ss0p95v125c Library: saed32rvrt_ss0p95v125c
Wire Load Model Mode: enclosed
Design      Wire Load Model      Library
-----
ChipTop          140000      saed32rvrt_tt1p05v25c
GeneralPurposeRegisters 16000      saed32rvrt_tt1p05v25c
Mult_32x32        8000       saed32rvrt_tt1p05v25c
power_controller   8000       saed32rvrt_tt1p05v25c
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW     (derived from V,C,T units)
    Leakage Power Units = 1pW
    Cell Internal Power = 1.7680 mW (97%)
    Net Switching Power = 51.5389 uW (3%)
-----
Total Dynamic Power = 1.8195 mW (100%)
Cell Leakage Power = 61.2553 uW
-----
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	126.4131	2.3107	0.0000	128.7239	(6.84%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	1.5937e+03	1.1786	2.9755e+07	1.6246e+03	(86.38%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	47.8756	48.0490	3.1500e+07	127.4253	(6.78%)	
Total	1.7680e+03 uW	51.5383 uW	6.1255e+07 pW	1.8808e+03 uW		

Fig. 19. Report of power.



```
*****
Report : timing
    -path full
    -delay max
    -max_paths 1
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 18:40:26 2024
*****


Operating Conditions: ss0p95v125c  Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed

Startpoint: GPRs/B_reg_reg[13]
            (rising edge-triggered flip-flop clocked by clock)
Endpoint: Multiplier/S_reg_reg[26]
            (rising edge-triggered flip-flop clocked by clock)
Path Group: CLOCK
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----
ChipTop           140000                 saed32rvt_tt1p05v25c
Mult_32x32        8000                  saed32rvt_tt1p05v25c

Point                      Incr      Path
-----
clock clock (rise edge)      0.00      0.00
clock network delay (ideal)  1.50      1.50
GPRs/B_reg_reg[13]/CLK (DFFSSRX1_HVT) 0.00      1.50 r
GPRs/B_reg_reg[13]/QN (DFFSSRX1_HVT)  0.28      1.78 f
GPRs/B[13] (GeneralPurposeRegisters) 0.00      1.78 f
Multiplier/Y[13] (Mult_32x32)       0.00      1.78 f
Multiplier/U345/Y (OR2X1_HVT)       0.08      1.87 f
Multiplier/U977/Y (AND2X1_HVT)      0.11      1.97 f
Multiplier/U1062/Y (NAND2X0_HVT)    0.06      2.03 r
Multiplier/U241/Y (NAND3X0_HVT)    0.08      2.11 f
Multiplier/U238/Y (AO21X1_HVT)      0.07      2.17 f
Multiplier/U10/Y (XNOR3X1_HVT)     0.24      2.42 r
Multiplier/U399/Y (XNOR3X1_HVT)    0.25      2.67 r
Multiplier/U176/S (FADDX1_HVT)     0.19      2.86 f
Multiplier/U790/Y (OR2X1_HVT)      0.06      2.92 f
Multiplier/U1091/Y (AND2X1_HVT)    0.05      2.97 f
```

Multiplier/U1092/Y (XOR2X1_HVT)	0.13	3.10 r
Multiplier/U563/Y (INVX0_HVT)	0.03	3.13 f
Multiplier/U1161/Y (NAND2X0_HVT)	0.03	3.16 r
Multiplier/U1162/Y (NAND2X0_HVT)	0.05	3.22 f
Multiplier/U1204/Y (XOR2X1_HVT)	0.12	3.33 r
Multiplier/U779/Y (INVX0_HVT)	0.03	3.36 f
Multiplier/U1224/Y (AND2X1_HVT)	0.05	3.42 f
Multiplier/U408/Y (OR2X1_HVT)	0.05	3.47 f
Multiplier/U1268/Y (XOR2X1_HVT)	0.11	3.57 r
Multiplier/U1269/Y (AND2X1_HVT)	0.06	3.64 r
Multiplier/U816/Y (INVX0_HVT)	0.03	3.67 f
Multiplier/U1923/Y (AND2X1_HVT)	0.05	3.72 f
Multiplier/U1925/Y (NAND2X0_HVT)	0.03	3.75 r
Multiplier/U1927/Y (NAND4X0_HVT)	0.10	3.85 f
Multiplier/U424/Y (OR2X1_HVT)	0.08	3.92 f
Multiplier/U2009/Y (AND2X1_HVT)	0.06	3.98 f
Multiplier/U2011/Y (NAND2X0_HVT)	0.03	4.01 r
Multiplier/U2012/Y (A021X1_HVT)	0.05	4.06 r
Multiplier/U86/Y (NAND3X1_HVT)	0.11	4.17 f
Multiplier/U84/Y (AND2X1_HVT)	0.05	4.22 f
Multiplier/U880/Y (OR3X1_HVT)	0.06	4.28 f
Multiplier/U2719/Y (XOR2X1_HVT)	0.10	4.39 r
Multiplier/S_reg_reg[26]/D (DFFSSRX1_HVT)	0.00	4.39 r
data arrival time		4.39

clock clock (rise edge)	3.30	3.30
clock network delay (ideal)	1.50	4.80
clock uncertainty	-0.30	4.50
Multiplier/S_reg_reg[26]/CLK (DFFSSRX1_HVT)	0.00	4.50 r
library setup time	-0.11	4.39
data required time		4.39

data required time		4.39
data arrival time		-4.39

slack (MET)		0.00

Fig. 20. Report of timing.

```
#####
#reports#####
report_area

*****
Report : area
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 18:40:26 2024
*****


Information: Updating design information... (UID-85)
Library(s) Used:

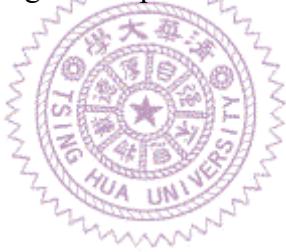
    saed32hvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_tt1p05v25c.db)
    saed32rvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_tt1p05v25c.db)
    saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)

Number of ports:          445
Number of nets:           7110
Number of cells:          6059
Number of combinational cells: 5335
Number of sequential cells: 710
Number of macros/black boxes: 4
Number of buf/inv:         865
Number of references:      28

Combinational area:       12842.150483
Buf/Inv area:             1133.482244
Noncombinational area:    5229.775122
Macro/Black Box area:     109409.210938
Net Interconnect area:    7970.475883

Total cell area:          127481.136542
Total area:                135451.612425
```

Fig. 21. Report of area.



- ICC side:

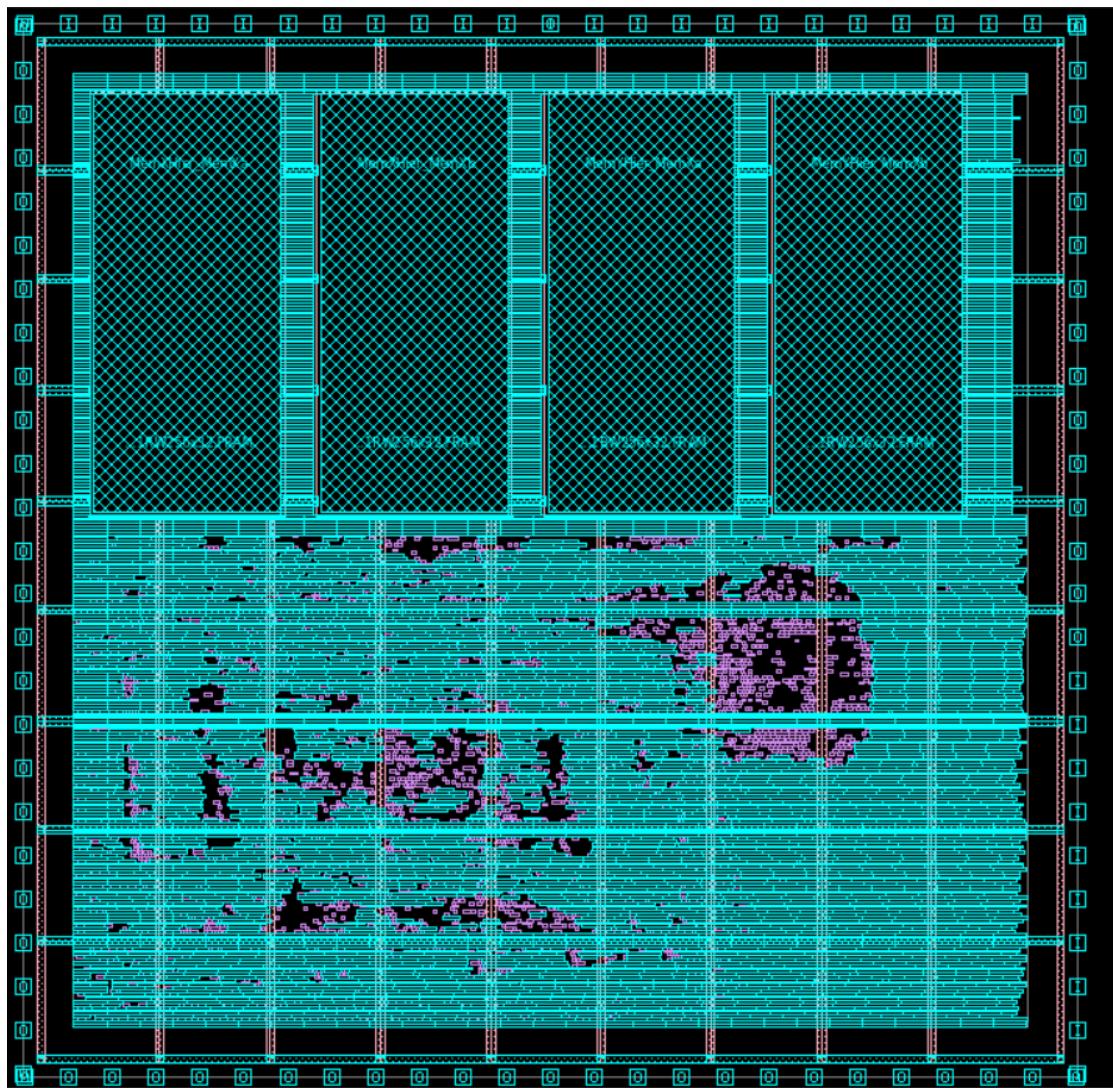


Fig. 22. Design view after compile.

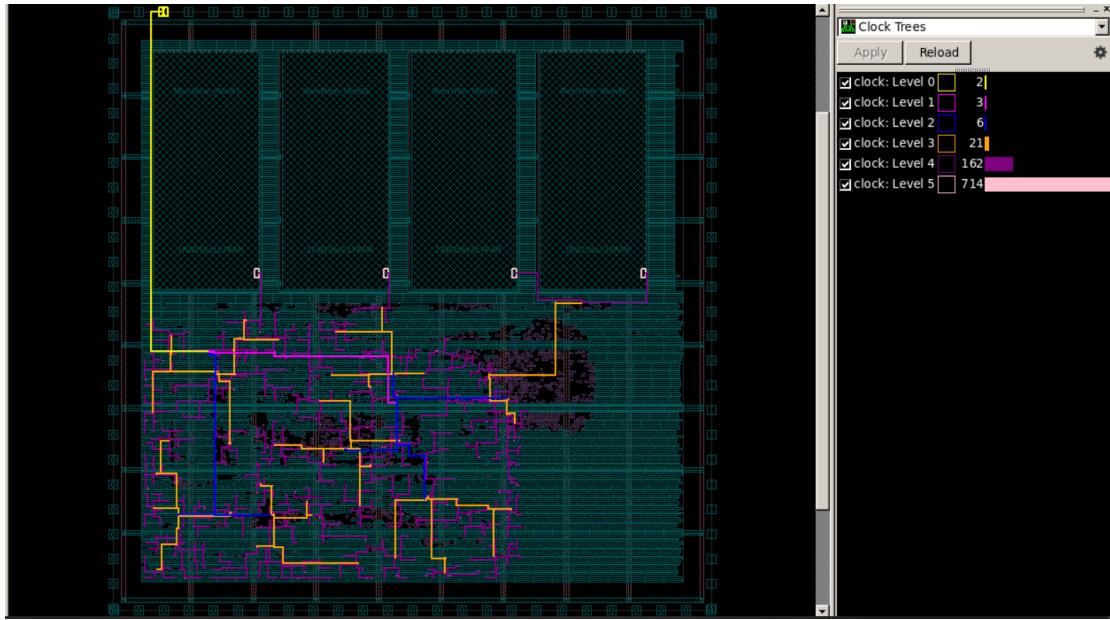


Fig. 23. Design view after CTS.

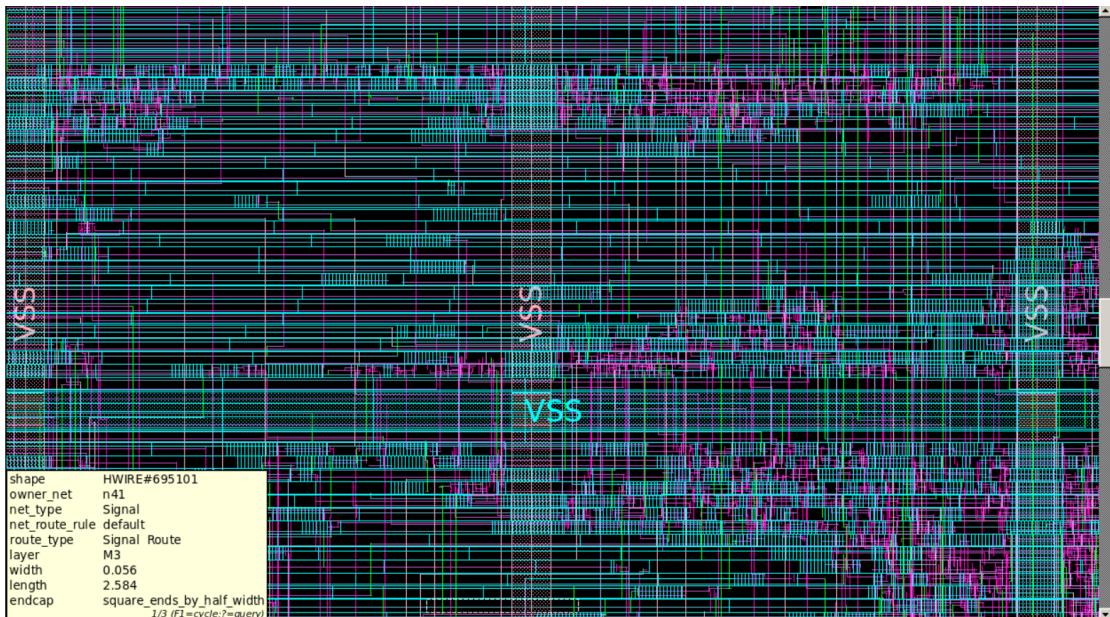


Fig. 24. Design view of standard cell routing.

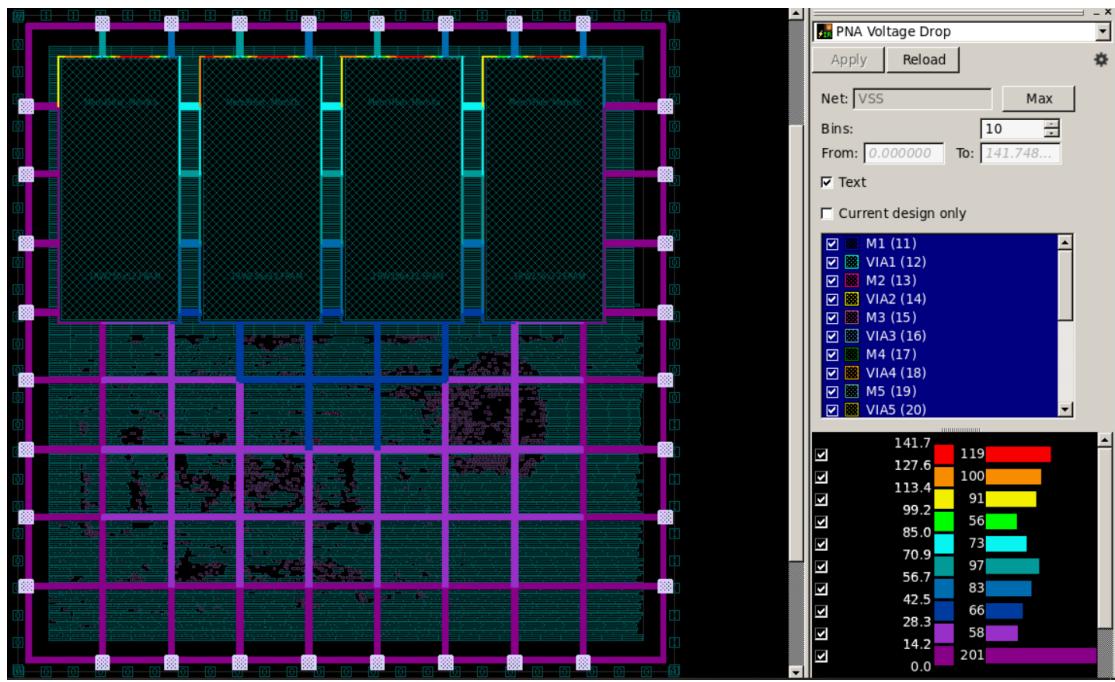


Fig. 25. Design view of leakage power density.

```
*****
Report : timing
    -path full
    -delay max
    -max_paths 1
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 19:13:41 2024
*****  

* Some/all delay information is back-annotated.  

Operating Conditions: ss0p95v125c  Library: saed32rvt_ss0p95v125c
  Parasitic source   : LPE
  Parasitic mode     : RealRC
  Extraction mode   : MIN_MAX
  Extraction derating : 125/125/125  

Information: Percent of Arnoldi-based delays = 28.87%  

Startpoint: GPRs/B_reg_reg_6_
  (rising edge-triggered flip-flop clocked by clock)
Endpoint: Multiplier/S_reg_reg_31_
  (rising edge-triggered flip-flop clocked by clock)
Path Group: CLOCK
Path Type: max  

Point           Incr      Path
-----
```

clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.20	0.20
GPRs/B_reg_reg_6_/CLK (DFFSSRX2_LVT)	0.00	0.20 r
GPRs/B_reg_reg_6_/QN (DFFSSRX2_LVT)	0.23	0.43 r
GPRs/B[6] (GeneralPurposeRegisters)	0.00	0.43 r
Multiplier/Y[6] (Mult_32x32)	0.00	0.43 r
Multiplier/U310/Y (OR2X1_RVT)	0.05 &	0.48 r
Multiplier/U638/Y (INVX0_HVT)	0.03 &	0.51 f
Multiplier/U1008/Y (AND2X2_RVT)	0.05 &	0.56 f
Multiplier/U65/Y (INVX2_RVT)	0.03 &	0.59 r
Multiplier/U252/Y (INVX8_RVT)	0.02 @	0.61 f
Multiplier/U2580/Y (NAND2X0_HVT)	0.04 @	0.65 r
Multiplier/U674/Y (NAND3X0_HVT)	0.13 &	0.78 f
Multiplier/U201/Y (AO21X1_RVT)	0.07 &	0.84 f
Multiplier/U510/Y (XNOR3X1_HVT)	0.26 &	1.10 r
Multiplier/intadd_30_U3/S (FADDX1_HVT)	0.20 &	1.30 f
Multiplier/U2516/S (FADDX1_HVT)	0.14 &	1.44 r
Multiplier/U2532/CO (FADDX1_HVT)	0.11 &	1.56 r
Multiplier/U554/Y (XOR2X1_HVT)	0.13 &	1.68 f
Multiplier/U553/Y (XNOR3X1_HVT)	0.23 &	1.91 r
Multiplier/U796/Y (XNOR3X1_HVT)	0.28 &	2.19 r
Multiplier/U5/Y (XNOR3X1_RVT)	0.14 &	2.33 r
Multiplier/U2592/Y (XNOR3X2_RVT)	0.06 &	2.39 r
Multiplier/U125/Y (XOR3X1_HVT)	0.08 &	2.47 f
Multiplier/U3/Y (XNOR3X2_RVT)	0.11 &	2.58 r
Multiplier/U2774/Y (NBUFFX2_RVT)	0.05 &	2.62 r
Multiplier/U82/Y (XOR2X2_HVT)	0.11 &	2.74 f
Multiplier/U2759/Y (NBUFFX4_RVT)	0.05 @	2.79 f
Multiplier/U896/Y (NAND2X4_RVT)	0.06 @	2.85 r
Multiplier/S_reg_reg_31/_D (DFFX2_RVT)	0.00 @	2.85 r
data arrival time		2.85
clock clock (rise edge)	3.30	3.30
clock network delay (propagated)	0.20	3.50
clock uncertainty	-0.30	3.20
Multiplier/S_reg_reg_31_/CLK (DFFX2_RVT)	0.00	3.20 r
library setup time	-0.03	3.17
data required time		3.17
data required time		3.17
data arrival time		-2.85
slack (MET)		0.32

Fig. 26. Report of timing.

```
*****
Report : area
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 19:13:35 2024
*****


Information: Updating design information... (UID-85)
Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)
Library(s) Used:

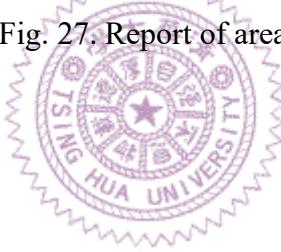
    saed32rvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_tt1p05v25c.db)
    saed32lvt_ss0p7v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p7v125c.db)
    saed32hvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_tt1p05v25c.db)
    saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)

Number of ports:          101
Number of nets:           1288
Number of cells:          987
Number of combinational cells: 944
Number of sequential cells: 36
Number of macros/black boxes: 4
Number of buf/inv:         543
Number of references:      66

Combinational area:       16911.504256
Buf/Inv area:             4070.878629
Noncombinational area:    5199.532158
Macro/Black Box area:     109409.210938
Net Interconnect area:    9872.732980

Total cell area:          131520.247351
Total area:                141392.980331
```

Fig. 27. Report of area.



```
*****
Report : power
|   -analysis_effort low
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 19:13:42 2024
*****
Library(s) Used:
    saed32rvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_tt1p05v25c.db)
    saed32lvt_ss0p7v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p7v125c.db)
    saed32hvt_tt1p05v25c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_tt1p05v25c.db)
    saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)
Operating Conditions: ss0p95v125c Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed
Design      Wire Load Model      Library
-----
ChipTop          ForQA           saed32rvt_tt1p05v25c
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW     (derived from V,C,T units)
    Leakage Power Units = 1pW
    Cell Internal Power = 2.1211 mW (74%)
    Net Switching Power = 727.3290 uW (26%)
    -----
Total Dynamic Power = 2.8484 mW (100%)
Cell Leakage Power = 2.3033 mW
-----
Power Group | Internal Power | Switching Power | Leakage Power | Total Power ( % ) Attrs
-----
io_pad       0.0000          0.0000          0.0000          0.0000 ( 0.00% )
memory      6.3665          17.2457          0.0000          23.6122 ( 0.46% )
black_box    0.0000          0.0000          0.0000          0.0000 ( 0.00% )
clock_network 212.0070        462.7664        7.2862e+07        747.6350 ( 14.51% )
register    1.7742e+03        4.0673        7.7074e+08        2.5490e+03 ( 49.48% )
sequential   0.0000          0.0000          0.0000          0.0000 ( 0.00% )
combinational 128.5272        243.2504        1.4597e+09        1.8315e+03 ( 35.55% )
-----
Total       2.1211e+03 uW    727.3297 uW    2.3033e+09 pW    5.1517e+03 uW
```

Fig. 28. Report of power.

- **Power gating**

- DC side:

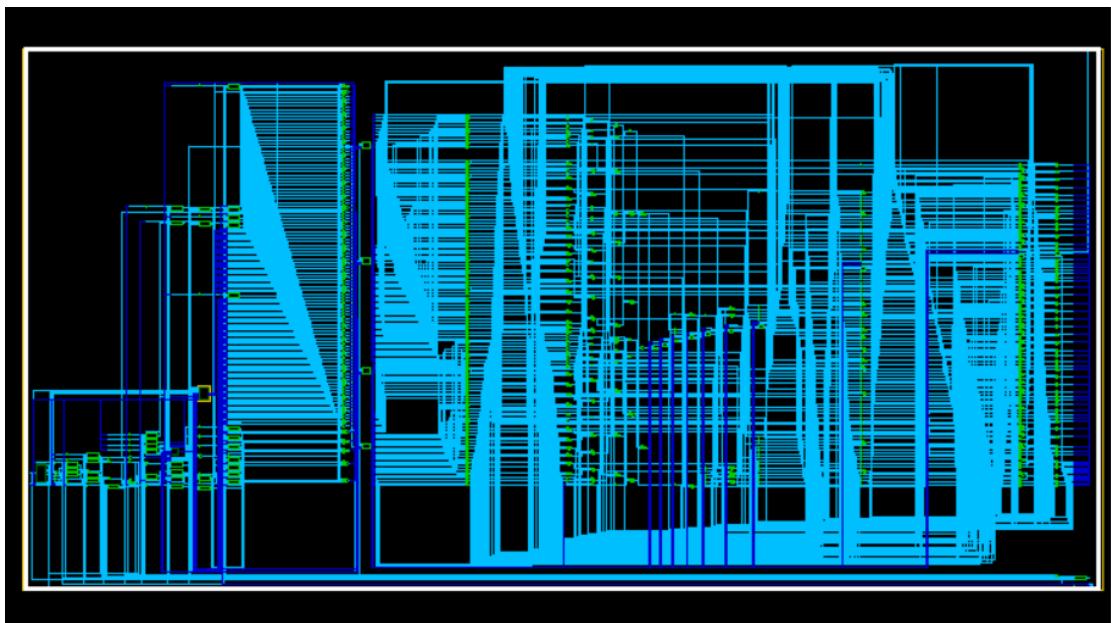


Fig. 29. Design view after compile_ultra.



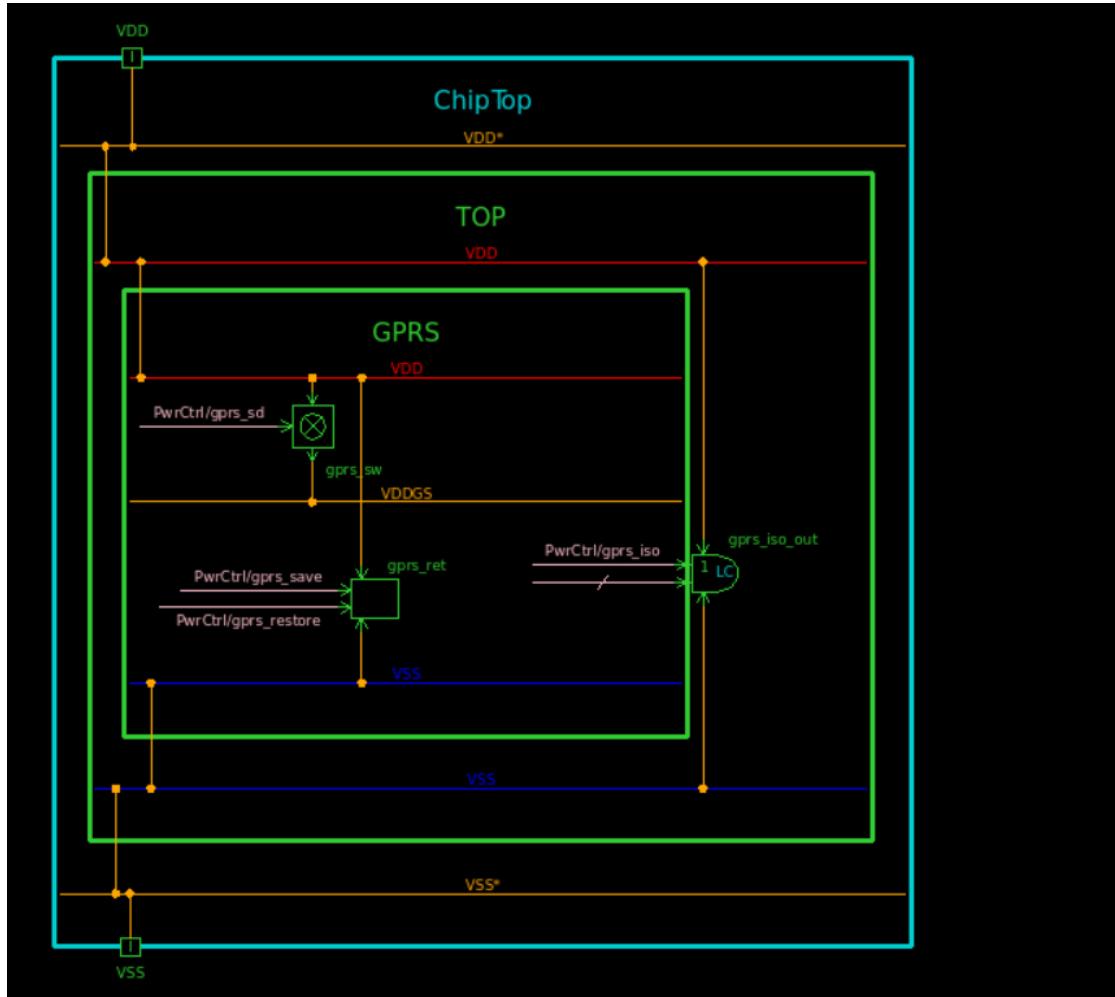


Fig. 30. UPF diagram.

- ICC side:

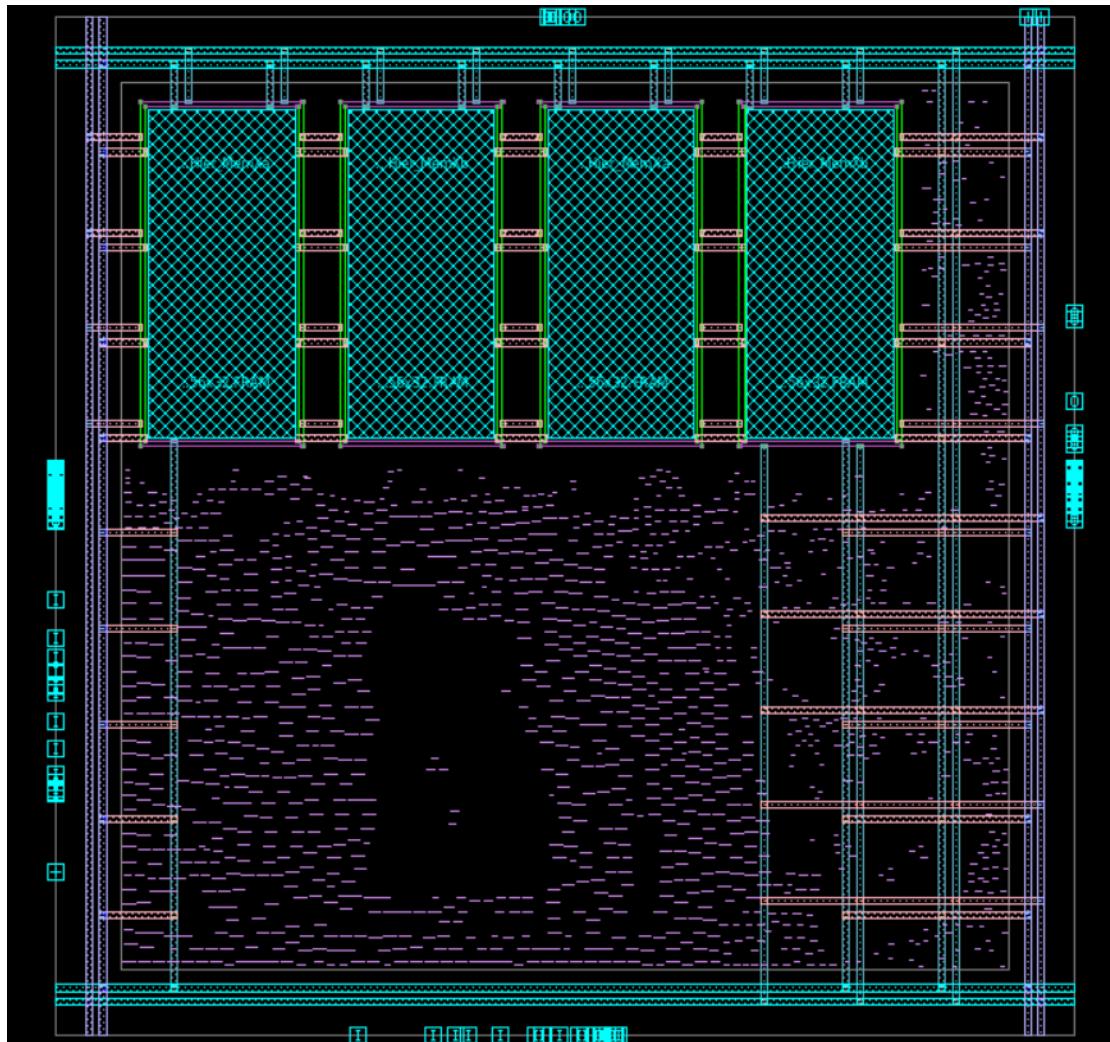


Fig. 31. Design view after compile.

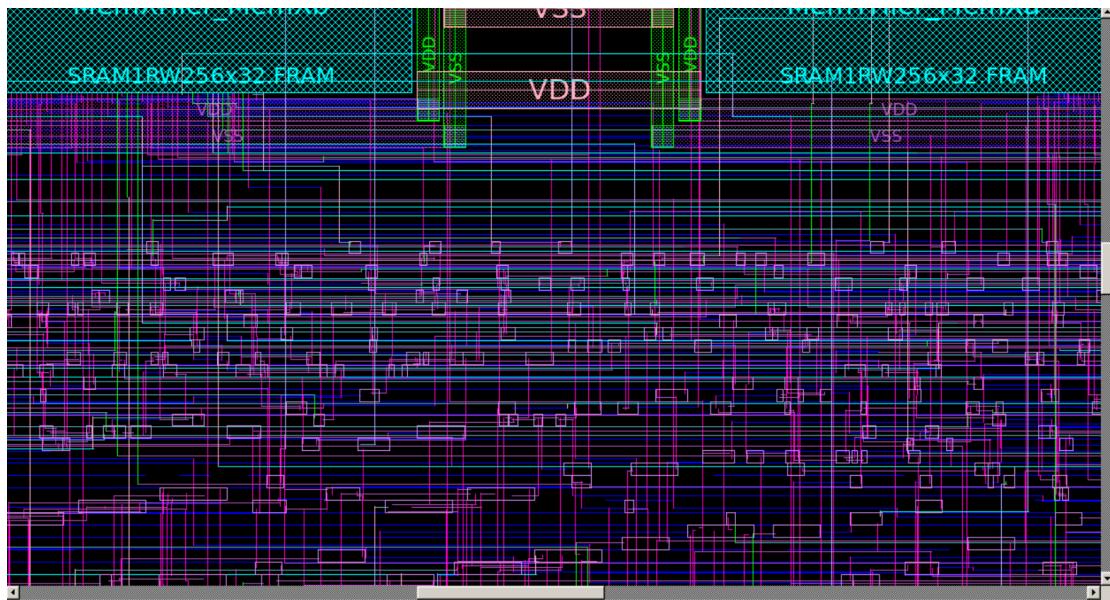


Fig. 32. Design view of standard cell routing.

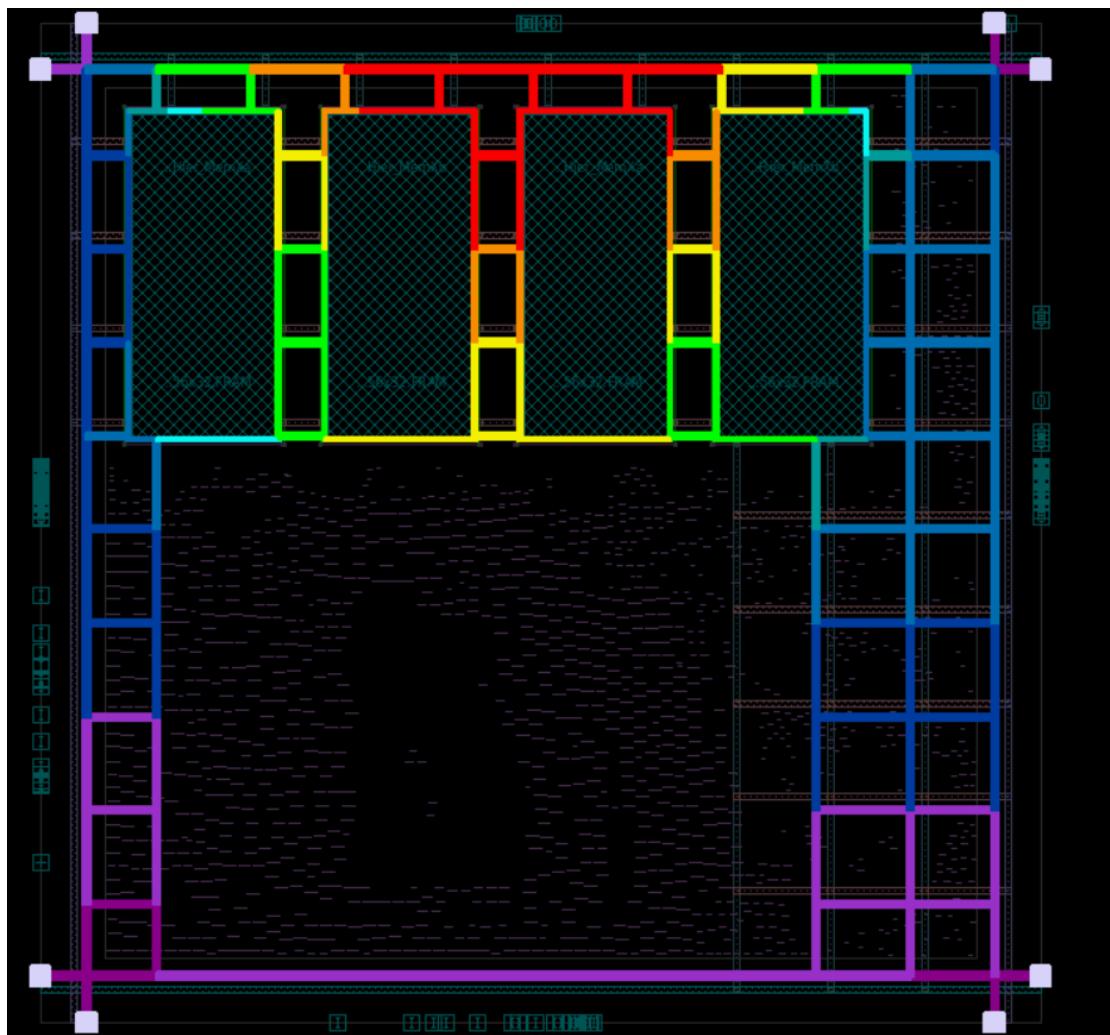


Fig. 33. Design view of leakage power density.

```
*****
Report : area
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 20:28:09 2024
*****


Library(s) Used:

    saed32rvt_ff0p85v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ff0p85v125c.db)
    saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)

Number of ports:          104
Number of nets:           1323
Number of cells:          1015
Number of combinational cells: 972
Number of sequential cells: 36
Number of macros/black boxes: 4
Number of buf/inv:         482
Number of references:     45

Combinational area:      19729.961353
Buf/Inv area:            6324.627686
Noncombinational area:   10017.339952
Macro/Black Box area:    109409.210938
Net Interconnect area:   15061.612676

Total cell area:          139156.512243
Total area:                154218.124919
```

Fig. 34. Report of area.



```
*****
Report : power
    -analysis_effort low
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 20:28:16 2024
*****


Library(s) Used:
    saed32rvt_ff0p85v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ff0p85v125c.db)
    saed32sram_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/sram/db_nldm/saed32sram_ss0p95v125c.db)
Operating Conditions: ss0p95v125c Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed
Design      Wire Load Model      Library
-----
ChipTop          ForQA          saed32rvt_dlvl_ss0p7v125c_i0p7v
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW   (derived from V,C,T units)
    Leakage Power Units = 1pW
    Cell Internal Power = -3.4581 mW (122%)
    Net Switching Power = 617.6249 uW (-21%)
    -----
    Total Dynamic Power = -2.8405 mW (100%)
    Cell Leakage Power = 96.4147 mW
Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

      Internal          Switching          Leakage          Total
Power Group      Power          Power          Power          Power  ( % )  Attrs
-----
io_pad          0.0000          0.0000          0.0000          0.0000 ( 0.00%)
memory         632.8096        45.0607          0.0000        677.8703 ( 0.72%)
black_box       0.0000          0.0000          0.0000          0.0000 ( 0.00%)
clock_network   0.0000          0.0000          0.0000          0.0000 ( 0.00%)
register        0.0000          0.0000          0.0000          0.0000 ( 0.00%)
sequential      -4.1155e+03        0.9199        2.3753e+10      1.9639e+04 ( 20.99%)
combinational   24.6002        571.6439        7.2662e+10      7.3258e+04 ( 78.29%)
    -----
Total          -3.4581e+03 uW      617.6244 uW      9.6415e+10 pW      9.3574e+04 uW
```

Fig. 35. Report of power.

```
*****
Report : timing
    -path full
    -delay max
    -max_paths 1
Design : ChipTop
Version: R-2020.09-SP5
Date   : Sun Jun 23 20:28:15 2024
*****  

* Some/all delay information is back-annotated.  

Operating Conditions: ss0p95v125c Library: saed32rvt_ss0p95v125c
    Parasitic source      : LPE
    Parasitic mode        : RealRC
    Extraction mode       : MIN_MAX
    Extraction derating  : 125/125/125  

Information: Percent of Arnoldi-based delays = 46.04%  

Startpoint: MemXHier_MemXb
            (rising edge-triggered flip-flop)
Endpoint: MemWriteBus[63]
            (output port)
Path Group: (none)
Path Type: max  

Point          Incr     Path
-----  

MemXHier_MemXb/CE (SRAM1RW256x32)      0.00    0.00 r
MemXHier_MemXb/0[28] (SRAM1RW256x32)    0.22    0.22 r
U846/Y (NBUFFX4_RVT)                    0.06 @  0.28 r
U41/Y (NBUFFX2_RVT)                     0.04 @  0.31 r
U333/Y (NAND2X0_RVT)                   0.06 &  0.38 f
U89/Y (OAI21X1_RVT)                    0.10 &  0.47 r
U337/Y (AOI21X1_RVT)                   0.05 &  0.53 f
U247/Y (OAI21X1_RVT)                   0.06 &  0.59 r
U748/Y (NBUFFX8_RVT)                   0.04 @  0.63 r
U338/Y (AOI21X1_RVT)                   0.05 @  0.68 f
```

U58/Y (OAI21X1_RVT)	0.06 &	0.74 r
U404/Y (A021X1_RVT)	0.05 &	0.78 r
U405/C0 (FADDX2_RVT)	0.06 &	0.84 r
U406/C0 (FADDX2_RVT)	0.06 &	0.90 r
U407/C0 (FADDX2_RVT)	0.06 &	0.96 r
U408/C0 (FADDX2_RVT)	0.06 &	1.02 r
U409/C0 (FADDX2_RVT)	0.06 &	1.07 r
U410/C0 (FADDX2_RVT)	0.06 &	1.13 r
U561/C0 (FADDX2_RVT)	0.06 &	1.19 r
U562/C0 (FADDX2_RVT)	0.06 &	1.25 r
U563/S (FADDX2_RVT)	0.10 &	1.35 f
U802/Y (NBUFFX4_RVT)	0.06 @	1.41 f
MemWriteBus[63] (out)	0.01 @	1.41 f
data arrival time		1.41
<hr/>		
(Path is unconstrained)		

Fig. 36. Report of timing.

2. FSIC-FIR

- Clock gating:

- DC side:



Fig. 37. Design view.

```
*****
Report : area
Design : FSIC
Version: R-2020.09-SP5
Date   : Sun Jun 23 08:54:12 2024
*****  

Library(s) Used:  

    saed32rvt_ff0p85v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ff0p85v125c.db)  

Number of ports:          9481  

Number of nets:           34311  

Number of cells:          25945  

Number of combinational cells: 14965  

Number of sequential cells: 9253  

Number of macros/black boxes: 0  

Number of buf/inv:         3742  

Number of references:      9  

Combinational area:       37791.975579  

Buf/Inv area:             7362.806175  

Noncombinational area:    61835.778271  

Macro/Black Box area:     0.000000  

Net Interconnect area:    22807.378078  

Total cell area:          99627.753850  

Total area:                122435.131928  

1
```

Fig. 38. Report of area.

Clock Gating Summary	
Number of Clock gating elements	746
Number of Gated registers	8185 (97.81%)
Number of Ungated registers	183 (2.19%)
Total number of registers	8368

Clock Gating Report by Origin	
	Actual (%) Count
Number of tool-inserted clock gating elements	746 (100.00%)
Number of pre-existing clock gating elements	0 (0.00%)
Number of gated registers	8185 (97.81%)
Number of tool-inserted gated registers	8185 (97.81%)
Number of pre-existing gated registers	0 (0.00%)
Number of ungated registers	183 (2.19%)
Number of registers	8368

Fig. 39. Report of clock gating.

```

Startpoint: wbs_cyc (input port clocked by clock)
Endpoint: U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/latch
           (gating element for clock clock)
Path Group: INPUTS
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----
FSIC                140000                 saed32rvf_ff0p85v125c
CFG_CTRL_pADDR_WIDTH15_pDATA_WIDTH32
           8000                  saed32rvf_ff0p85v125c

Point               Incr      Path
-----
clock clock (rise edge)      0.00      0.00
clock network delay (ideal)  1.50      1.50
input external delay         1.00      2.50 f
wbs_cyc (in)                0.00      2.50 f
U_CFG_CTRL0/wbs_cyc (CFG_CTRL_pADDR_WIDTH15_pDATA_WIDTH32)    0.00      2.50 f
U_CFG_CTRL0/U582/Y (AND4X1_RVT)  0.05      2.55 f
U_CFG_CTRL0/U266/Y (NAND2X0_RVT) 0.03      2.58 r
U_CFG_CTRL0/U264/Y (NAND2X0_RVT) 0.02      2.60 f
U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/EN (SNPS_CLOCK_GATE_HIGH_CFG_CTRL_pADDR_WIDTH15_pDATA_WIDTH32_24) 0.00      2.60 f
U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/latch/EN (CGLPPRX2_RVT)  0.00      2.60 f
data arrival time           0.00      2.60

clock clock (rise edge)      7.00      7.00
clock network delay (ideal)  1.50      8.50
clock uncertainty            -0.30     8.20
U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/latch/CLK (CGLPPRX2_RVT)  0.00      8.20 r
clock gating setup time     -0.08     8.12
data required time           0.00      8.12

data required time           8.12
data arrival time             -2.60

slack (MET)                 5.53

```

Fig. 40. Report of timing.

- ICC side:

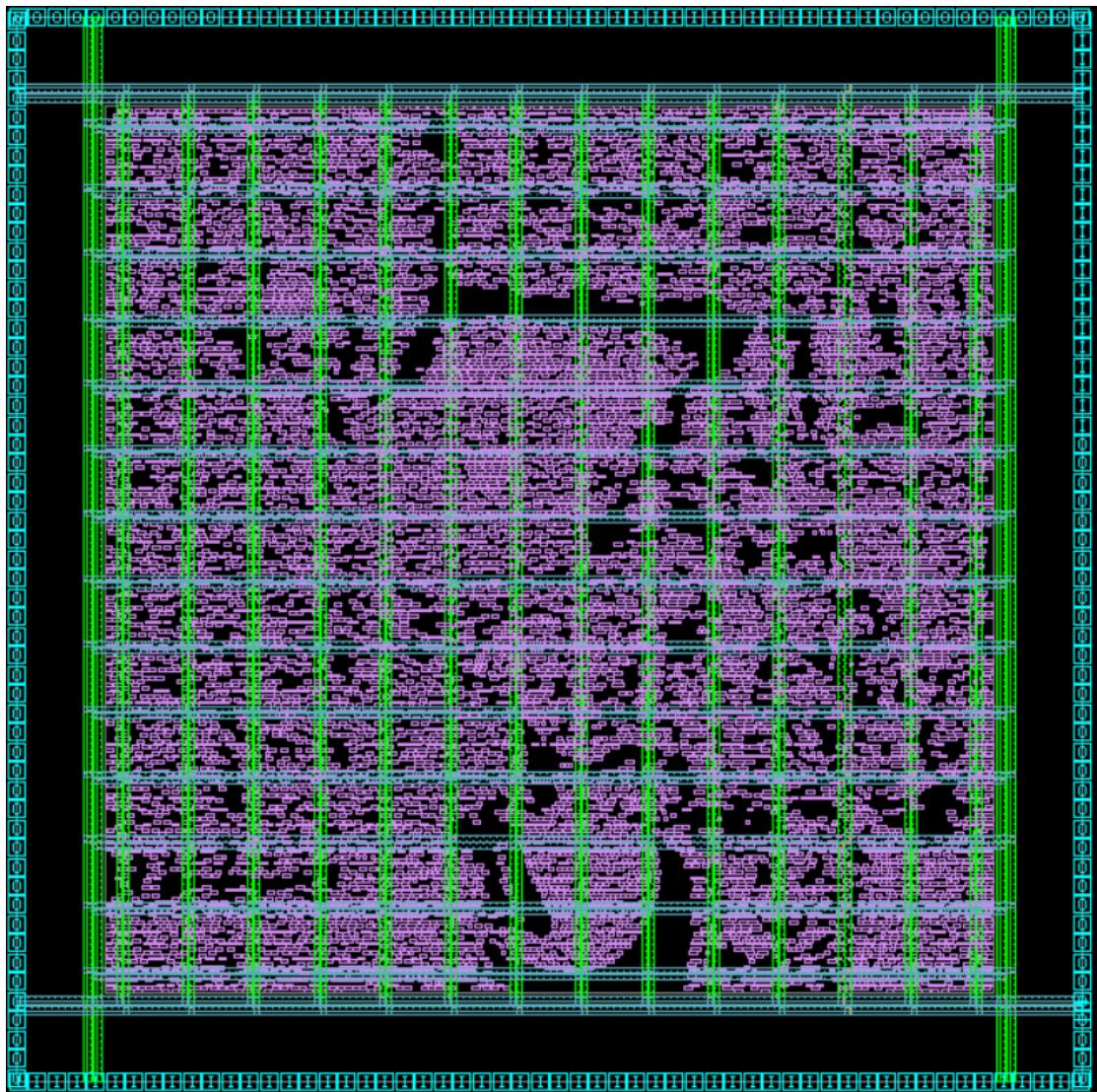


Fig. 41. Design view after Core Placement and Optimization.

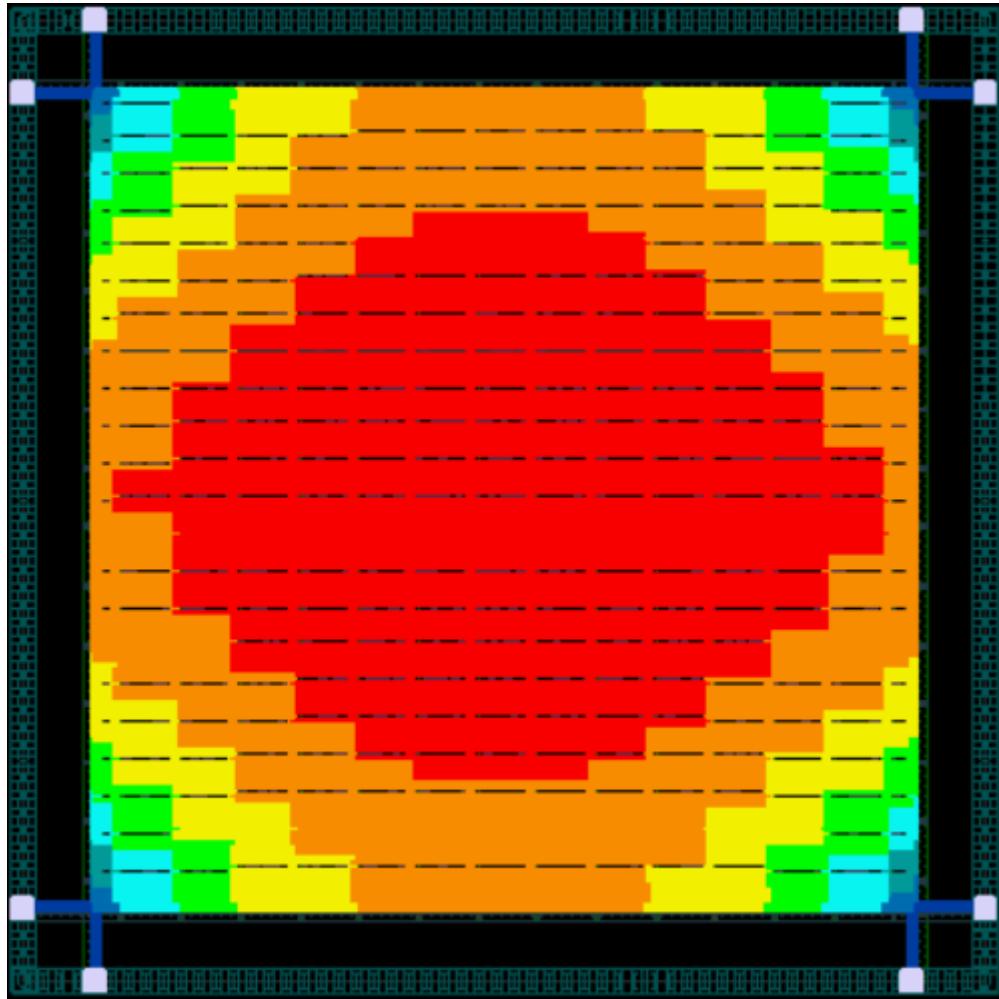


Fig. 42. Design view of Leakage Power Density window.

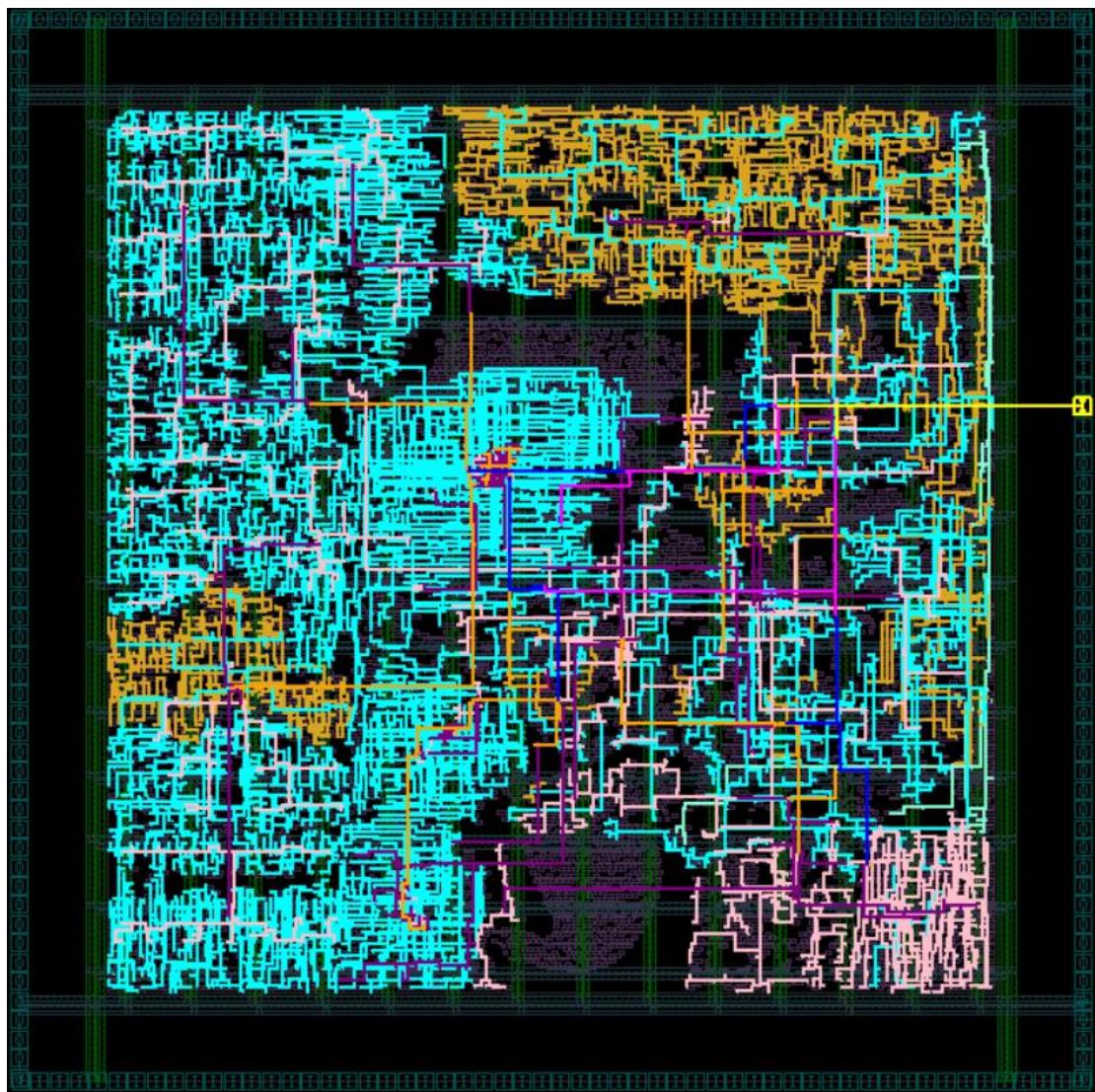


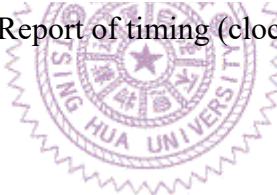
Fig. 43. Design view of after Core CTS and Optimization.

Startpoint: wbs_cyc (input port clocked by clock)		
Endpoint: U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/latch (gating element for clock clock)		
Path Group: INPUTS		
Path Type: max		
Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (ideal)	1.50	1.50
input external delay	1.00	2.50 f
wbs_cyc (in)	0.00	2.50 f
U_CFG_CTRL0/wbs_cyc (CFG_CTRL_pADDR_WIDTH15_pDATA_WIDTH32)	0.00	2.50 f
U_CFG_CTRL0/U582/Y (AND4X1_RVT)	0.06 *	2.56 f
U_CFG_CTRL0/U266/Y (NAND2X0_RVT)	0.04 *	2.60 r
U_CFG_CTRL0/U264/Y (NAND2X0_RVT)	0.02 *	2.62 f
U_CFG_CTRL0/U72/Y (DELLN1X2_RVT)	0.12 *	2.75 f
U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/EN (SNPS_CLOCK_GATE_HIGH_CFG_CTRL_pADDR_WIDTH15_pDATA_WIDTH32_24)	0.00	2.75 f
U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/latch/EN (CGLPPRX2_RVT)	0.00 *	2.75 f
data arrival time		2.75
clock clock (rise edge)	7.00	7.00
clock network delay (ideal)	1.50	8.50
clock uncertainty	-0.30	8.20
U_CFG_CTRL0/clk_gate_wb_axi_wdata_reg/latch/CLK (CGLPPRX2_RVT)	0.00	8.20 r
clock gating setup time	-0.08	8.12
data required time		8.12

data required time		8.12
data arrival time		-2.75

slack (MET)		5.38

Fig. 44. Report of timing (clock gating).



- Multi-Voltage

- DC side:

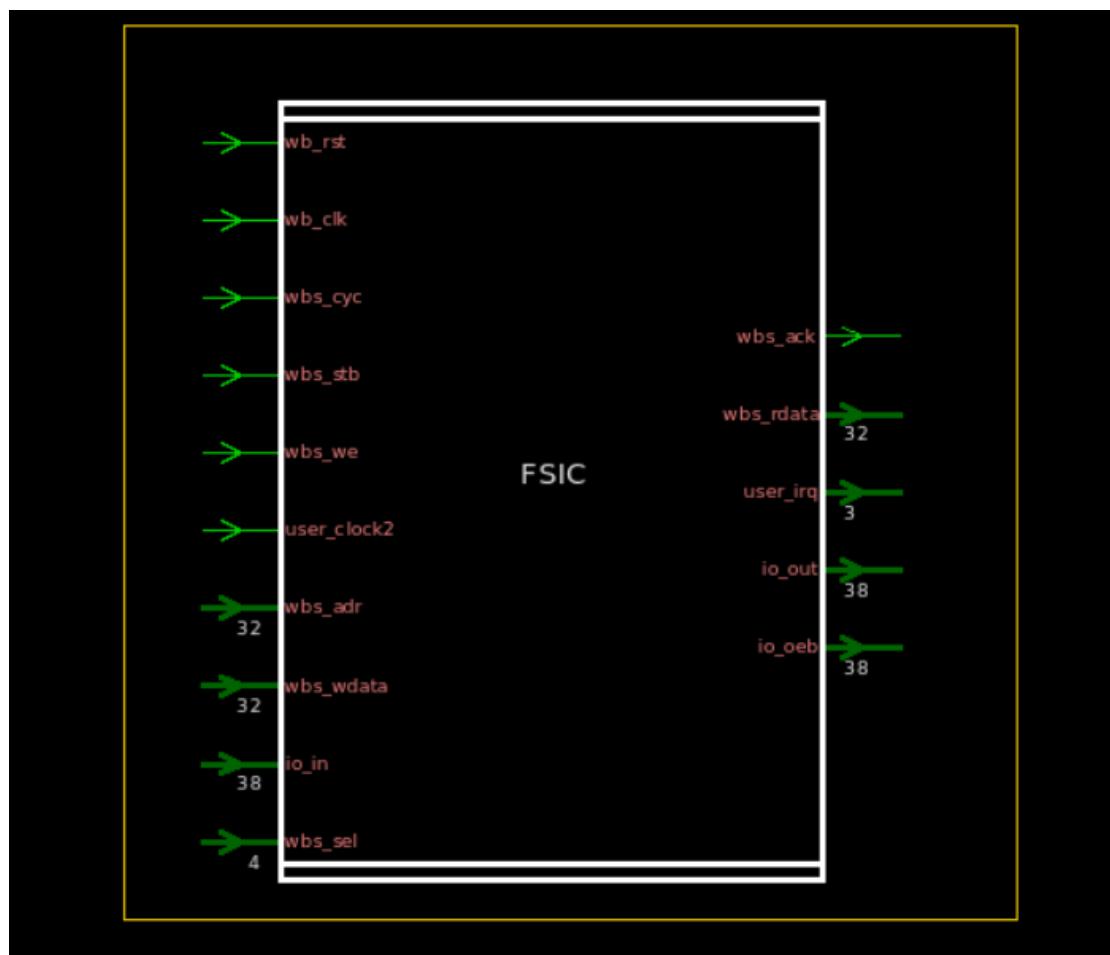


Fig. 45. Design view of symbol.

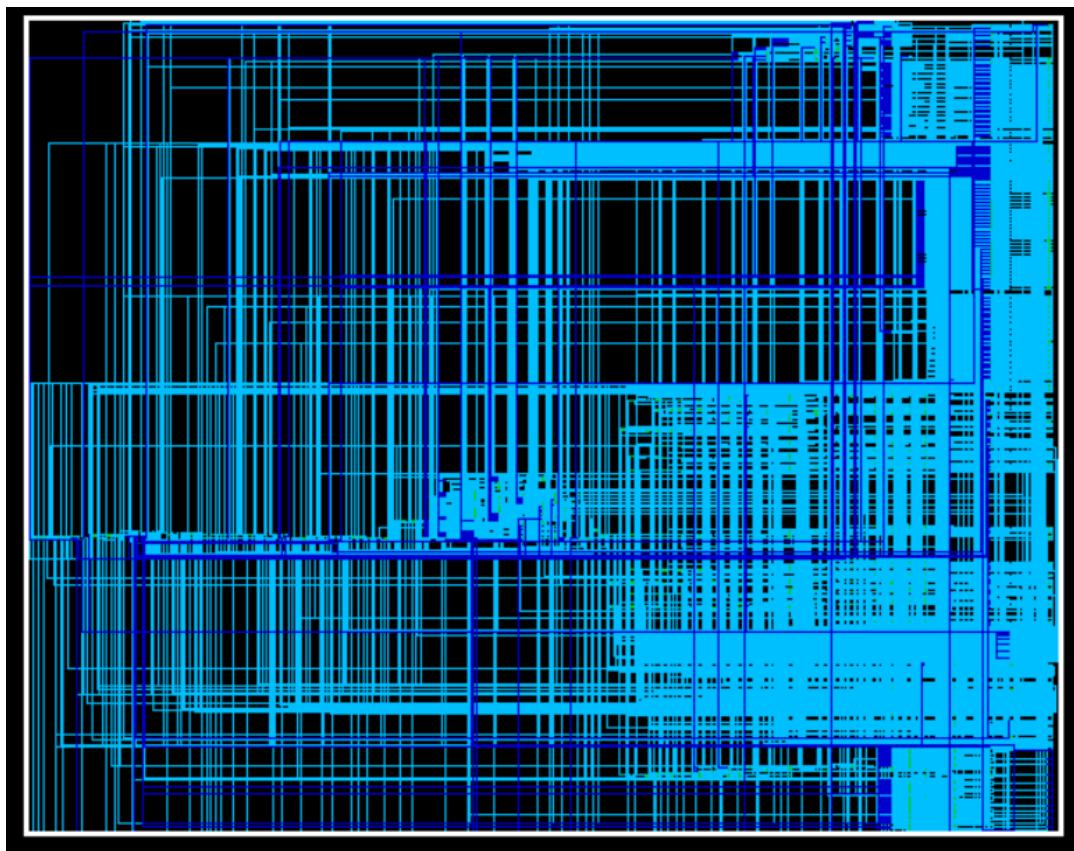


Fig. 46. Design view after compile_ultra.



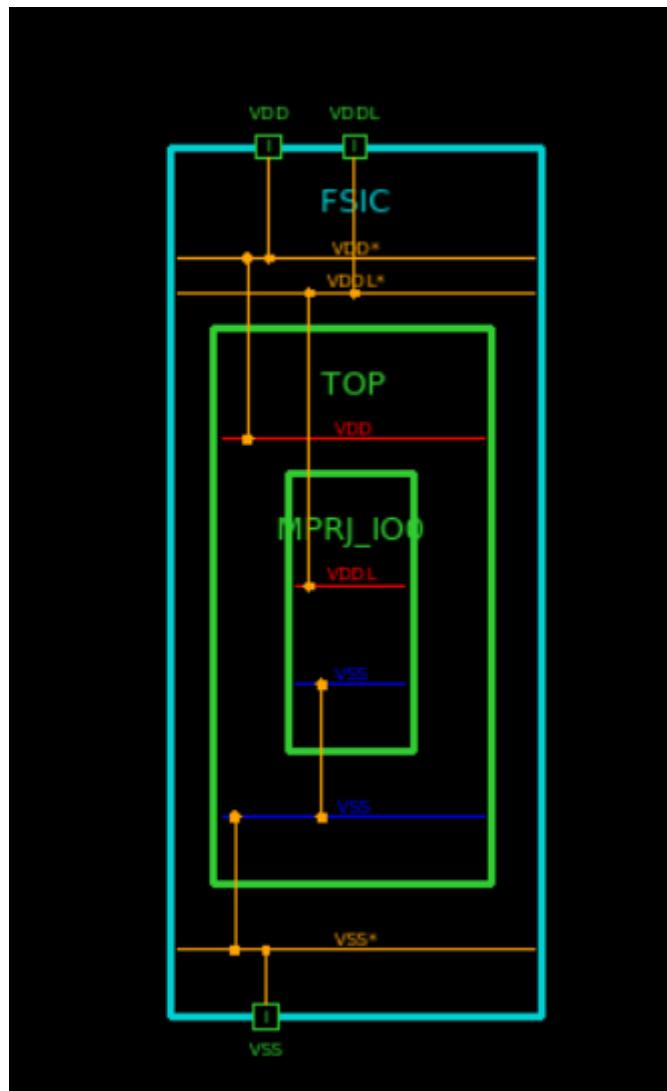


Fig. 47. UPF diagram.

```

report_area
*****
Report : area
Design : FSIC
Version: R-2020.09-SPS
Date   : Sun Jun 23 14:12:42 2024
*****  

Information: Updating design information... (UID-85)
Warning: Design 'FSIC' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
Library(s) Used:  

    saed32rvt_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ss0p95v125c.db)  

Number of ports:          2529
Number of nets:           28723
Number of cells:          26215
Number of combinational cells: 17826
Number of sequential cells: 8350
Number of macros/black boxes: 0
Number of buf/inv:         1456
Number of references:      51  

Combinational area:       44945.366562
Buf/Inv area:             2147.770964
Noncombinational area:    56104.068582
Macro/Black Box area:     0.000000
Net Interconnect area:    56878.496668  

Total cell area:          101049.435143
Total area:                157927.931812
1

```

Fig. 48. Report of area.

```
*****
Report : timing
    -path full
    -delay max
    -max_paths 1
Design : FSIC
Version: R-2020.09-SP5
Date   : Sun Jun 23 14:12:43 2024
*****
```

A fanout number of 1000 was used for high fanout net computations.

Wire Load Model Mode: enclosed

Startpoint: U_USER_SUBSYS0/U_USRPRJ1/tap_RAM/rdo_reg[3]
(rising edge-triggered flip-flop clocked by clock)

Endpoint: U_USER_SUBSYS0/U_USRPRJ1/fir_U0/sm_tdata_reg_reg[30]
(rising edge-triggered flip-flop clocked by clock)

Path Group: CLOCK

Path Type: max

Des/Clust/Port	Wire Load Model	Library
FSIC	140000	saed32rvts0p95v125c
USER_PRJ1_pUSER_PROJECT_SIDEBOARD_WIDTH5_pADDR_WIDTH12_pDATA_WIDTH32	35000	saed32rvts0p95v125c
fir	16000	saed32rvts0p95v125c



Point	Incr	Path	Voltage
clock clock (rise edge)	0.00	0.00	
clock network delay (ideal)	0.20	0.20	
U_USER_SUBSYS0/U_USRPRJ1/tap_RAM/rdo_reg[3]/CLK (DFFX1_RVT)	0.00 #	0.20 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/tap_RAM/rdo_reg[3]/Q (DFFX1_RVT)	0.21	0.41 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/tap_Do[3] (fir)	0.00	0.41 f	
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U71/Y (NBUFFX2_RVT)	0.07	0.49 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1412/Y (AND2X1_RVT)	0.07	0.55 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U113/Y (NOR2X0_RVT)	0.08	0.63 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1443/Y (OR2X1_RVT)	0.06	0.69 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U302/Y (XNOR2X1_RVT)	0.11	0.80 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U156/Y (INVX0_RVT)	0.03	0.83 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1445/Y (NOR2X0_RVT)	0.07	0.90 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U306/Y (OR2X1_RVT)	0.05	0.95 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U304/Y (XNOR2X1_RVT)	0.11	1.06 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U179/Y (XOR3X1_RVT)	0.10	1.16 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1534/CO (FADDX1_RVT)	0.11	1.27 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U13/CO (FADDX1_RVT)	0.12	1.39 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1456/Y (OA21X1_RVT)	0.07	1.46 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1457/Y (AO22X1_RVT)	0.07	1.53 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U42/Y (INVX1_RVT)	0.02	1.55 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1461/Y (NAND3X0_RVT)	0.03	1.58 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1464/Y (AO22X1_RVT)	0.07	1.65 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U464/Y (AOI22X1_RVT)	0.09	1.73 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U447/Y (AND2X1_RVT)	0.05	1.79 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U445/Y (NOR2X0_RVT)	0.08	1.86 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U444/Y (OR2X1_RVT)	0.06	1.92 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U50/Y (INVX0_RVT)	0.03	1.95 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1473/Y (OA21X1_RVT)	0.07	2.02 f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U417/Y (NOR2X0_RVT)	0.08	2.10 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1478/Y (OA21X1_RVT)	0.07	2.17 r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U362/Y (INVX0_RVT)	0.03	2.20 f	0.95

U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U421/Y (OA21X1_RVT)	0.07	2.27	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1493/Y (AND2X1_RVT)	0.05	2.32	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U219/Y (OR2X1_RVT)	0.05	2.38	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1494/Y (AO22X1_RVT)	0.06	2.43	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1496/Y (AND2X1_RVT)	0.06	2.49	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1497/Y (NOR2X0_RVT)	0.07	2.56	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1501/Y (OA22X1_RVT)	0.07	2.64	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U49/Y (INVX0_RVT)	0.02	2.66	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U222/Y (NOR2X0_RVT)	0.08	2.74	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U432/Y (AO22X1_RVT)	0.06	2.80	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U47/Y (OR2X1_RVT)	0.06	2.85	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1511/Y (NOR2X0_RVT)	0.08	2.93	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U435/Y (OAI22X1_RVT)	0.07	3.01	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U434/Y (AO21X1_RVT)	0.05	3.05	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1514/Y (NAND2X0_RVT)	0.05	3.10	f	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1515/Y (NAND2X0_RVT)	0.07	3.17	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U44/Y (XNOR2X2_RVT)	0.10	3.27	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/U1519/Y (AO22X1_RVT)	0.06	3.33	r	0.95
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/sm_tdata_reg_reg[30]/D (DFFARX1_RVT)	0.00	3.33	r	0.95
data arrival time		3.33		

clock clock (rise edge)	3.30	3.30		
clock network delay (ideal)	0.20	3.50		
clock uncertainty	-0.10	3.40		
U_USER_SUBSYS0/U_USRPRJ1/fir_U0/sm_tdata_reg_reg[30]/CLK (DFFARX1_RVT)	0.00	3.40	r	
library setup time	-0.07	3.33		
data required time		3.33		

data required time		3.33		
data arrival time		-3.33		

slack (MET)	0.00			

Fig. 49. Report of timing.

```

report_power
*****
Report : power
    -analysis_effort low
Design : FSIC
Version: R-2020.09-SP5
Date   : Sun Jun 23 14:12:43 2024
*****


Library(s) Used:

saed32rvt_ss0p95v125c (File: /home/course/ee5252/SAED32_EDK/lib/stdcell_rvt/db_nldm/saed32rvt_ss0p95v125c.db)

Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW

Cell Internal Power = 20.5566 mW (100%)
Net Switching Power = 37.0044 uW (0%)
-----
Total Dynamic Power = 20.5936 mW (100%)
Cell Leakage Power = 5.4640 mW



| Power Group   | Internal Power | Switching Power | Leakage Power | Total Power ( % )    | Attrs |
|---------------|----------------|-----------------|---------------|----------------------|-------|
| io_pad        | 0.0000         | 0.0000          | 0.0000        | 0.0000 ( 0.00%)      |       |
| memory        | 0.0000         | 0.0000          | 0.0000        | 0.0000 ( 0.00%)      |       |
| black_box     | 0.0000         | 0.0000          | 0.0000        | 0.0000 ( 0.00%)      |       |
| clock_network | 0.0000         | 0.0000          | 0.0000        | 0.0000 ( 0.00%)      |       |
| register      | 2.0507e+04     | 1.8321          | 3.7145e+09    | 2.4223e+04 ( 92.97%) |       |
| sequential    | 34.5330        | 4.6192e-02      | 2.3080e+08    | 265.3774 ( 1.02%)    |       |
| combinational | 13.5081        | 35.1261         | 1.5187e+09    | 1.5674e+03 ( 6.02%)  |       |
| Total         | 2.0555e+04 uW  | 37.0044 uW      | 5.4640e+09 pW | 2.6056e+04 uW        |       |
| 1             |                |                 |               |                      |       |


```

Fig. 50. Report of power.

- ICC side:

- Problem: I think this problem should be that I need to go to the design to check and compare where the power consumption is high, and use UPF there.

```

route_zrt_eco -max_detail_route_iterations 5
Error: Top cell not open. (ZRT-072)
0
#verify_lvs -check_open_locator -check_short_locator
save_mw_cel -as chip_top_4_routed
Error: Cannot get cellId for the current design. (UID-2)
0
derive_pg_connection
0
insert_stdcell_filler -cell_with_metal $filler_cell -cell_without_metal $filler_cell_wom -voltage_area MPRJ_I00 -connect_to_power VDDL -conn
ect_to_ground VSS
Can not get cellId for current design
#####
reports#####
report_area
Error: Current design is not defined. (UID-4)
0
report_timing
Error: Current design is not defined. (UID-4)
0
report_power
Error: Current design is not defined. (UID-4)
0
save_mw_cel -as fsic_4_finished
Error: Cannot get cellId for the current design. (UID-2)
0
change_names -rules verilog -verbose
Error: Current design is not defined. (UID-4)
0
write_verilog -pg -wire_declaration ..//output/fsic.v
Error: Current design is not defined. (UID-4)
Current design is not set
0
set_write_stream_options -flatten_via -child_depth 20 -output_filling fill -output_pin text
1
write_stream -format gds ..//output/fsic.gds
No layer map file is used during stream out!
Skip layer map file
===== TOTAL CELLS OUTPUT: 0 =====
write_gds completed successfully!
1
#close_mw_lib
icc_shell> icc_shell> █

```

Fig. 51. Problem screenshot.



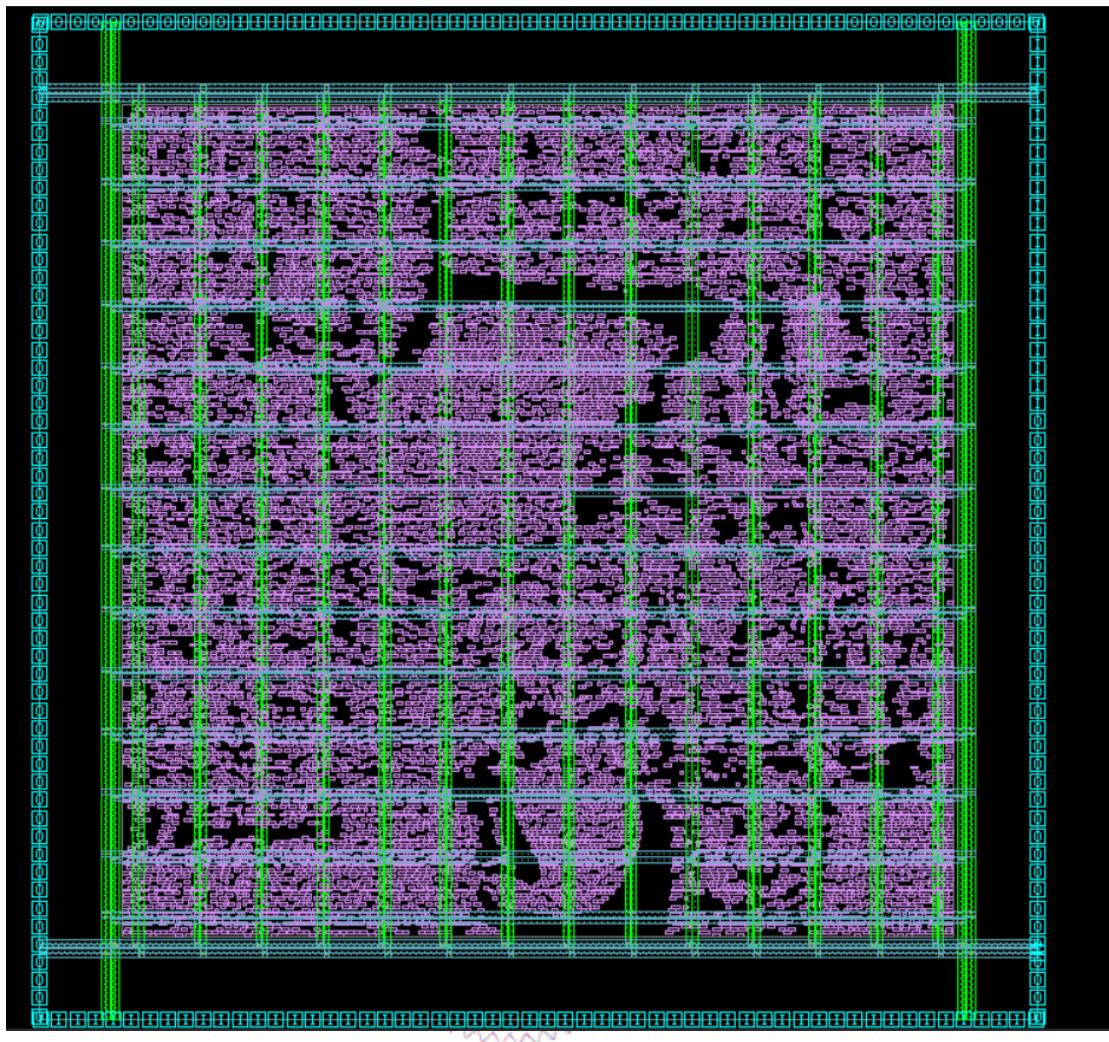


Fig. 52. Design view.

3. Conclusion:

This lab is based on the content of the workbook to complete “low power design”. I run the design flow step by step according to the lab, analyze the report and observe the tool GUI (Graphical User Interface) to strengthen impression, so that I can understand what each command means and when it should be used. After using it, I combined it with the class content during practice. I was more impressed with the experimental content. When encountering problems during the practice, I would think about how to solve them and discuss them together in the course discussion forum to get answers. I am very grateful to the teacher for his careful teaching. and carefully prepared course content and thank you to the TAs (Teaching Assistants) for patiently answering questions!!

