FIR Core ALU Design, Verification, and Analysis Report

1. Design Specifications

- The ALU serves to provide the operational support for a MAC. It should be able to add and multiply fixed-point numbers both positive and negative. The output from the ALU should be able to be later saved to and retrieved from a register.

2. RTL Code Description

- The RTL ALU is designed to take in two 16 bit inputs along with a 2 bit selector. Based on the value of the selector, the ALU takes one clock cycle to compute the output as a 32 bit signed integer through either addition or multiplication and choose which of the computed values to output.

3. Testbench Design and Verification

- This testbench reads inputs from external files, performs operations, and compares the ALU's output with reference values from MATLAB-generated files. The testbench generates a clock signal and applies reset at the beginning. It reads operands and reference results from external files, writes ALU output to a results file. There are two separate loops for testing addition and multiplication operations. Finally, it verifies ALU output against MATLAB-generated results to ensure accuracy.

4. Timing and Power Analysis

- The ALU has timing issues in the first few cycles where the output is not stable. To address this, the ALU waits three cycles before performing any operations.

Power Analysis

Power Group	**Internal Power**	**Switching Power**	**Leakage Power**	**Total Power**	**% of Total**
Clock Network	1.440e-03	0	0	1.440e-03	29.59%
Register	1.352e-04	2.262e-07	3.666e-09	1.355e-04	2.78%
Combinational	1.929e-03	1.362e-03	3.152e-08	3.291e-03	67.63%