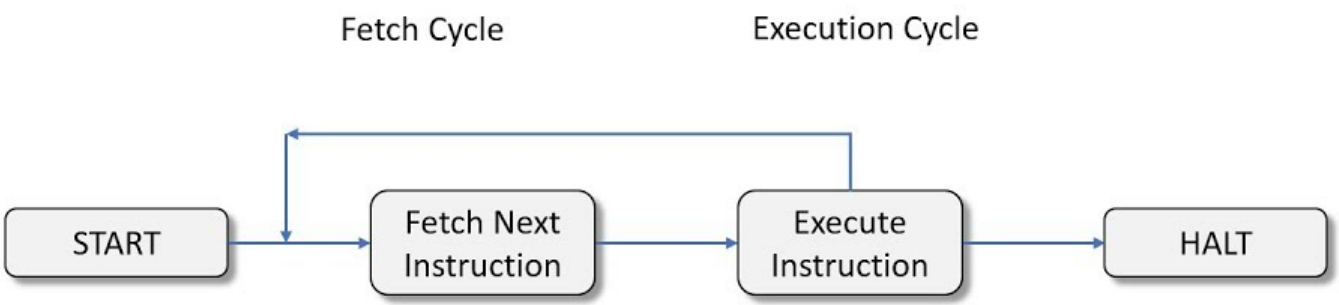
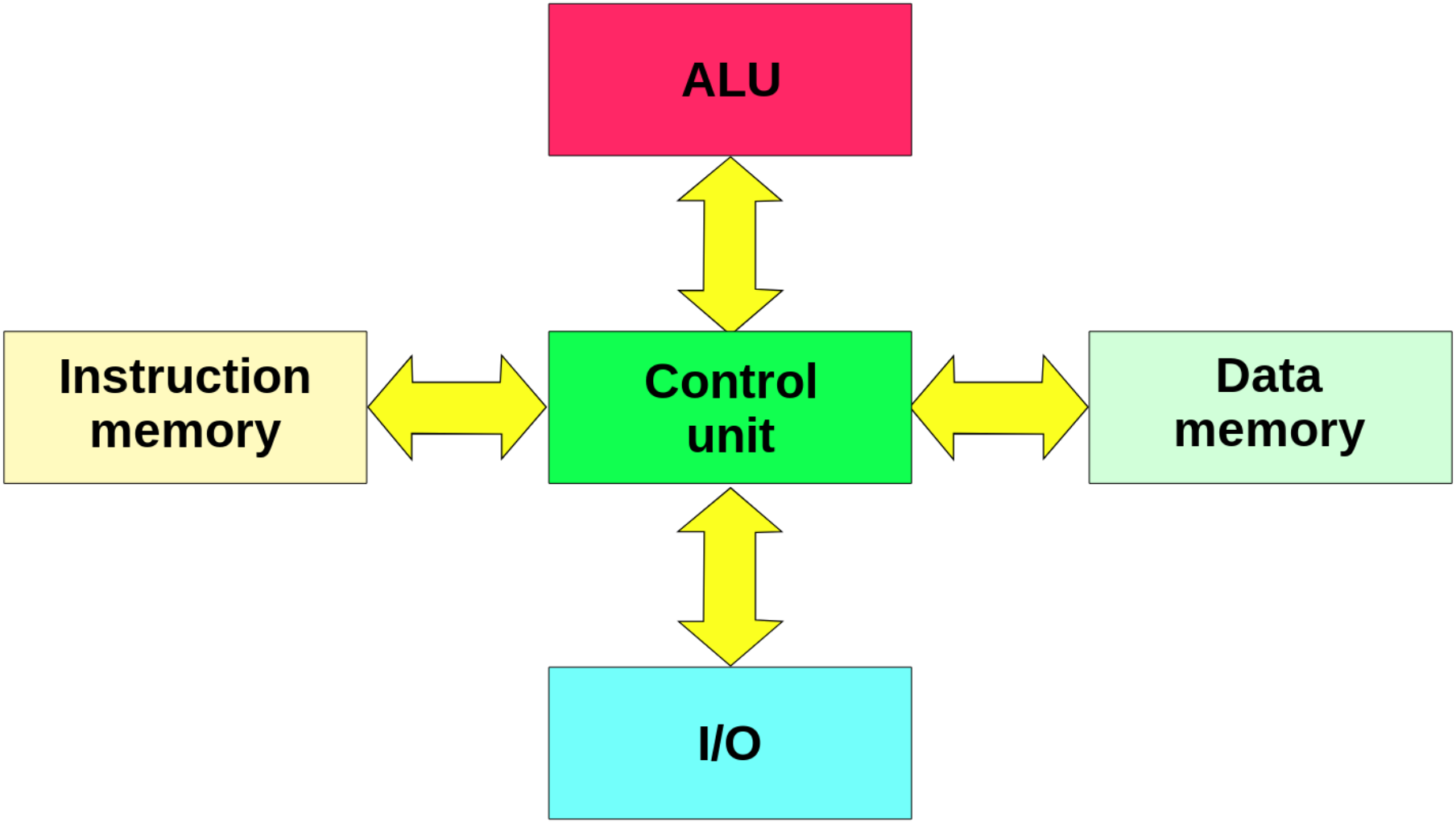
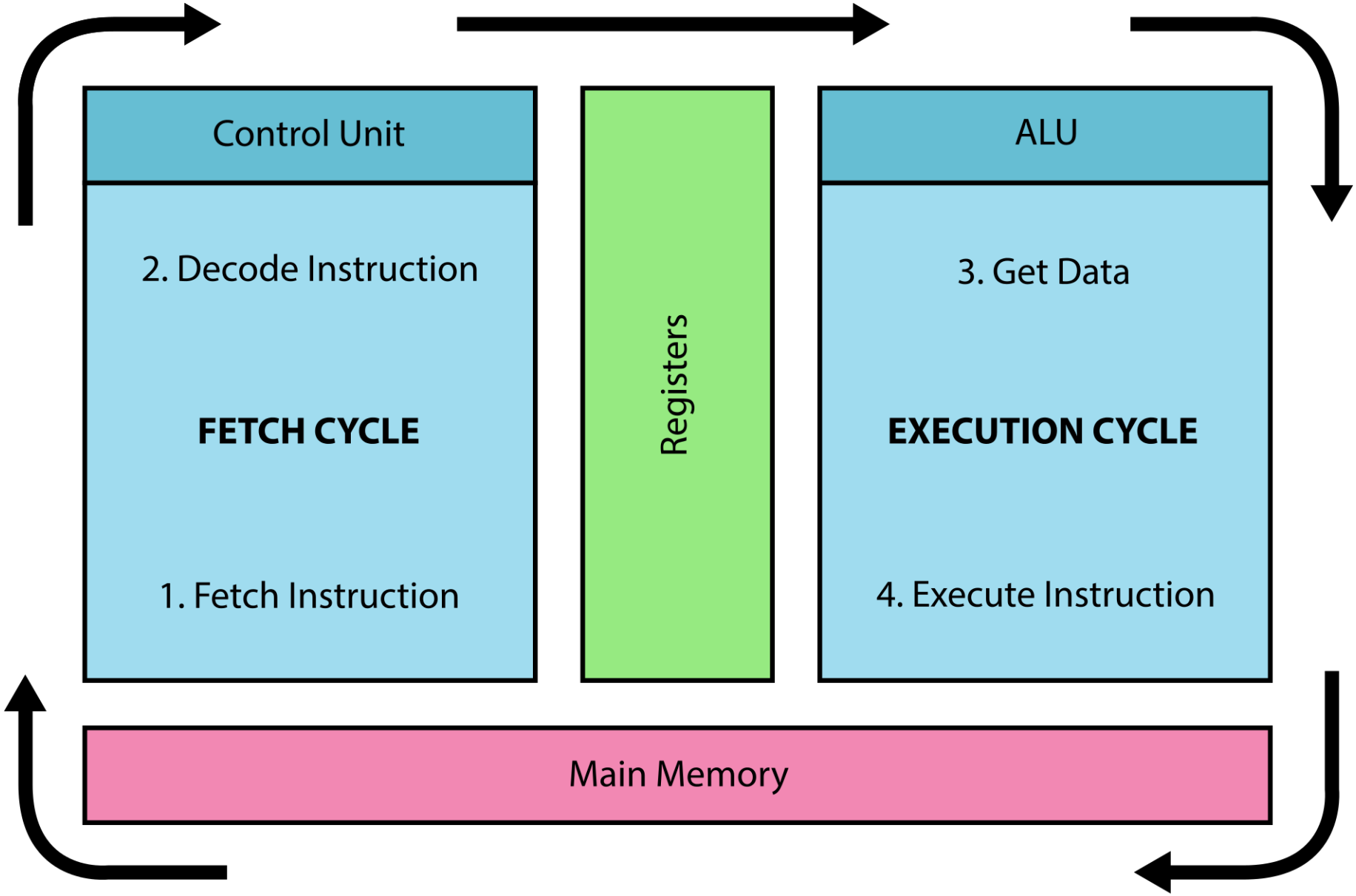
Flynn’s Taxonomy

Prof. Mike Flynn’s famous taxonomy of parallel computers

Computer Instruction Cycle




ALU
Instruction memory
Control unit
Data memory
I/O


Control Unit
2. Decode Instruction
FETCH CYCLE
1. Fetch Instruction
Registers
ALU
3. Get Data
EXECUTION CYCLE
4. Execute Instruction
Main Memory

Flynn's Taxonomy

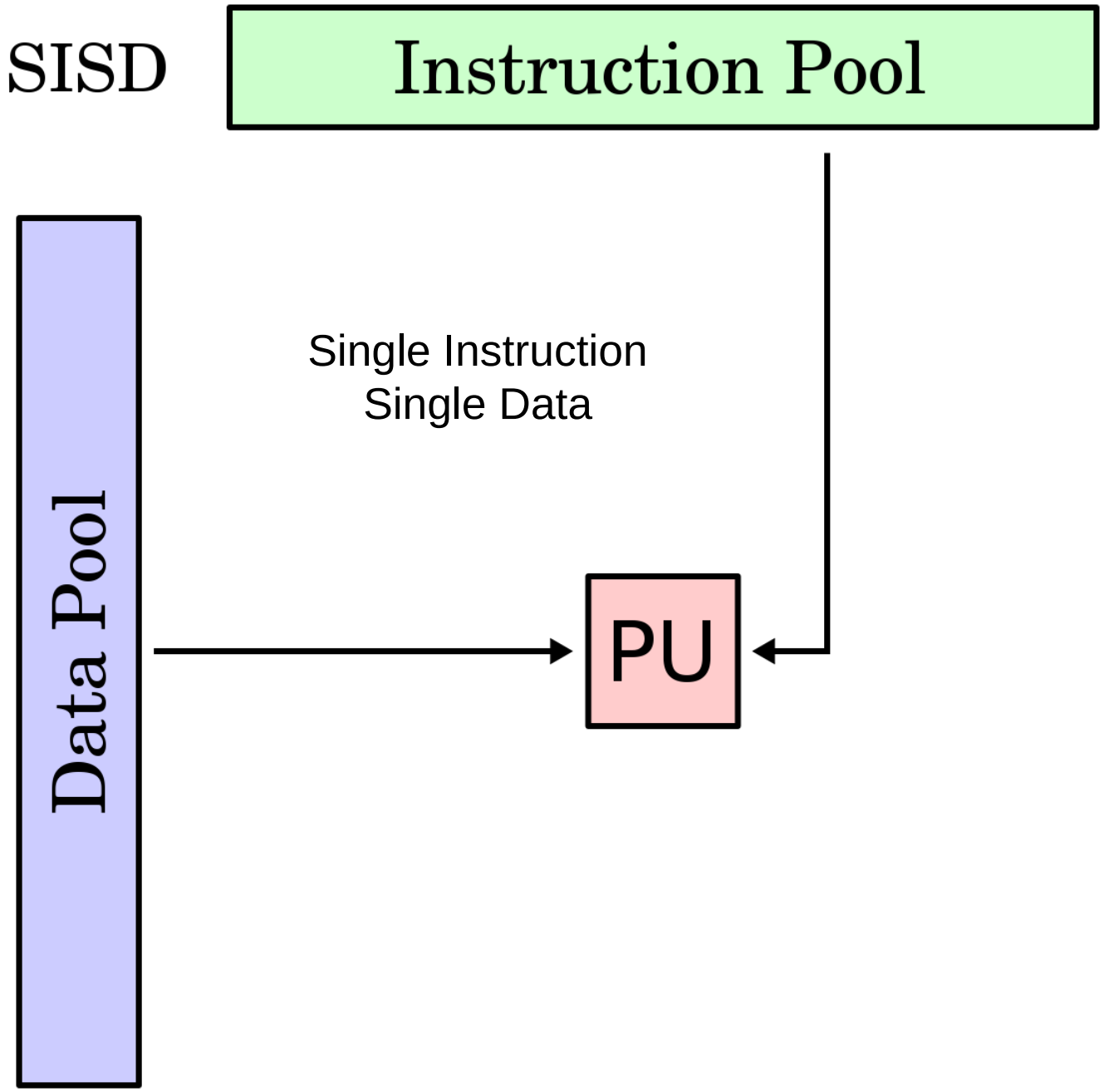
Proposed by Prof. Mike Flynn in 1966

how many instructions

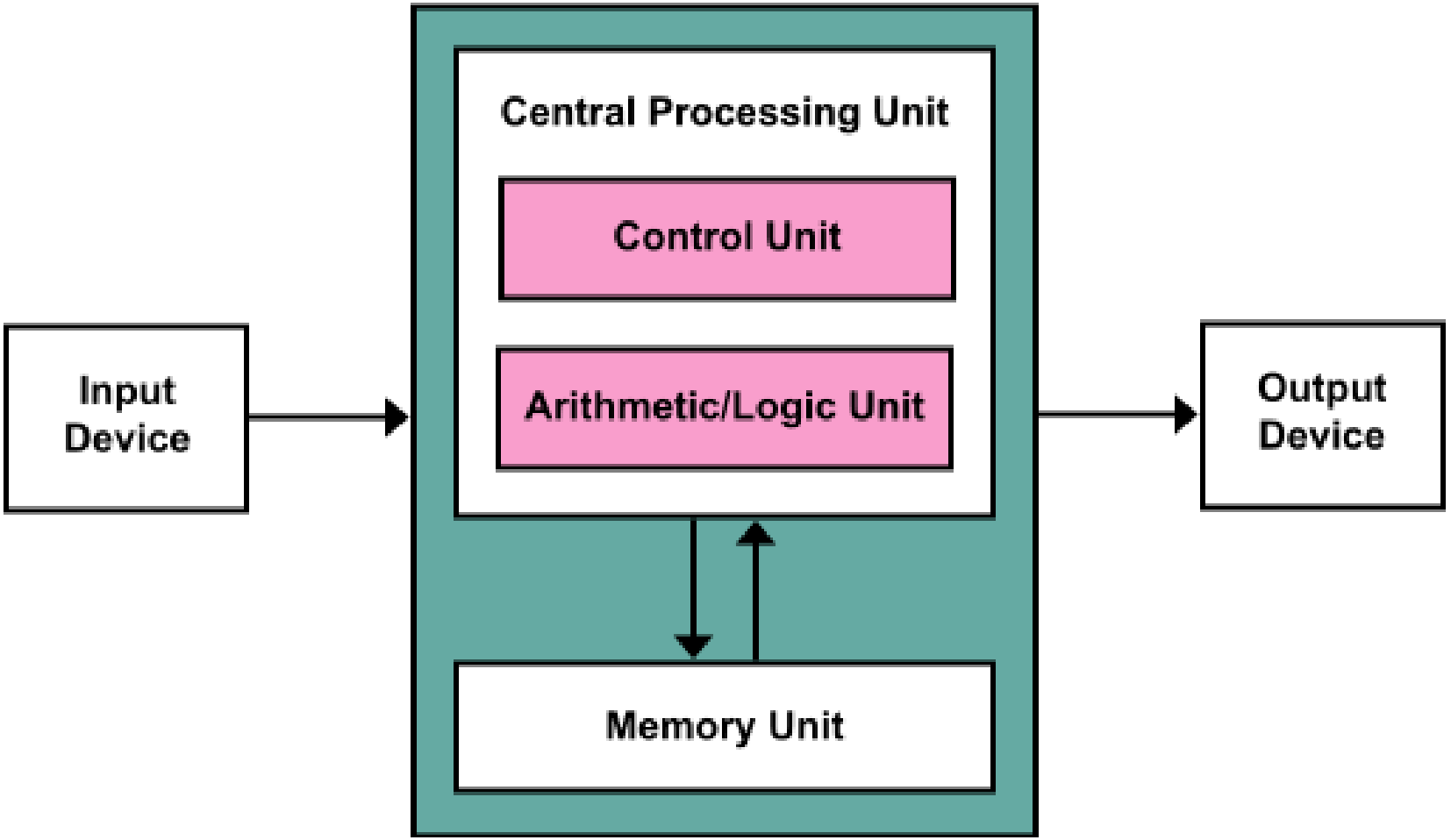
vs

how much data

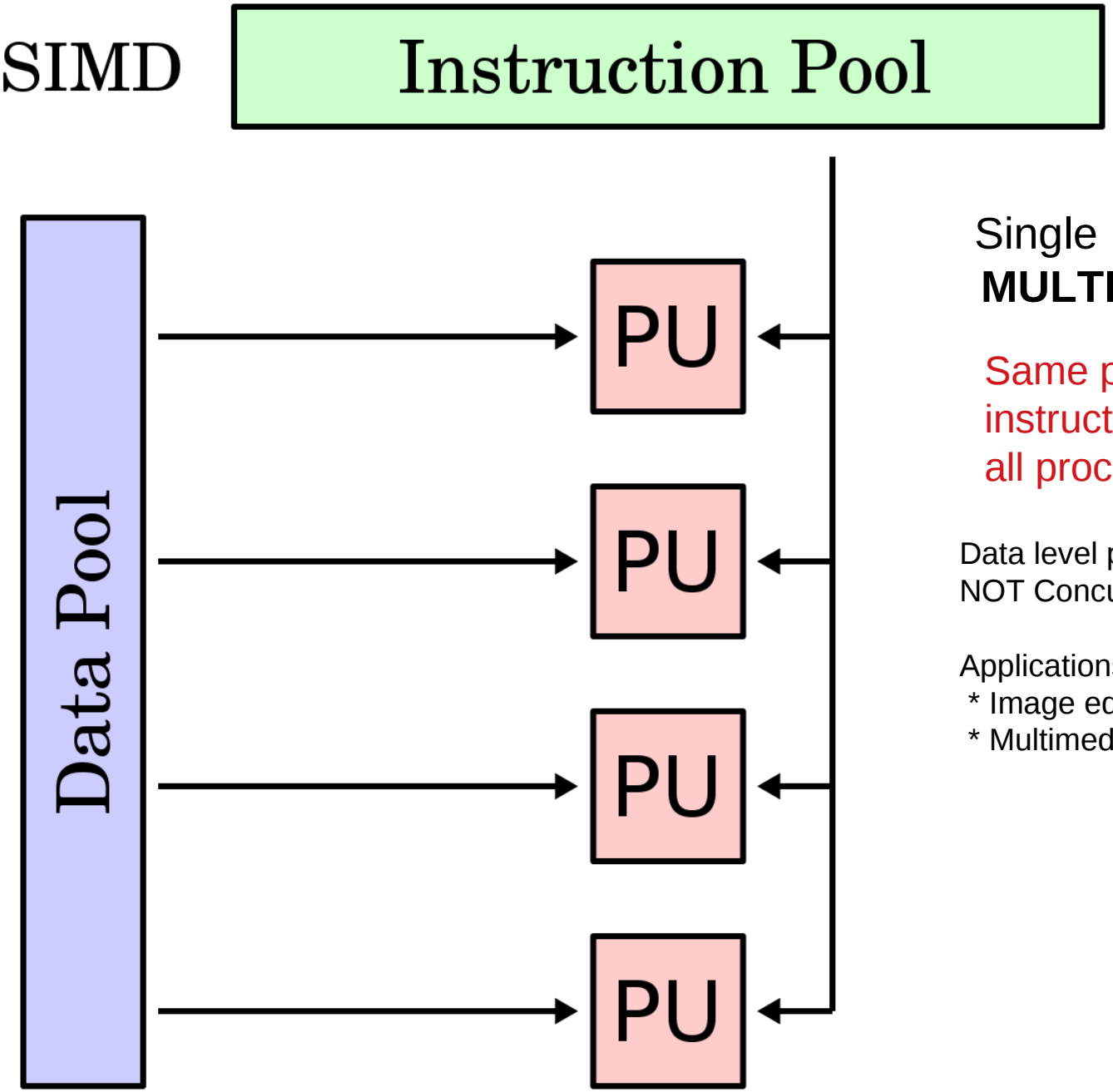
can be processed simultaneously


SISD
Instruction Pool
Data Pool
Single Instruction
Single Data
PU

Von-Neumann Architecture



SIMD

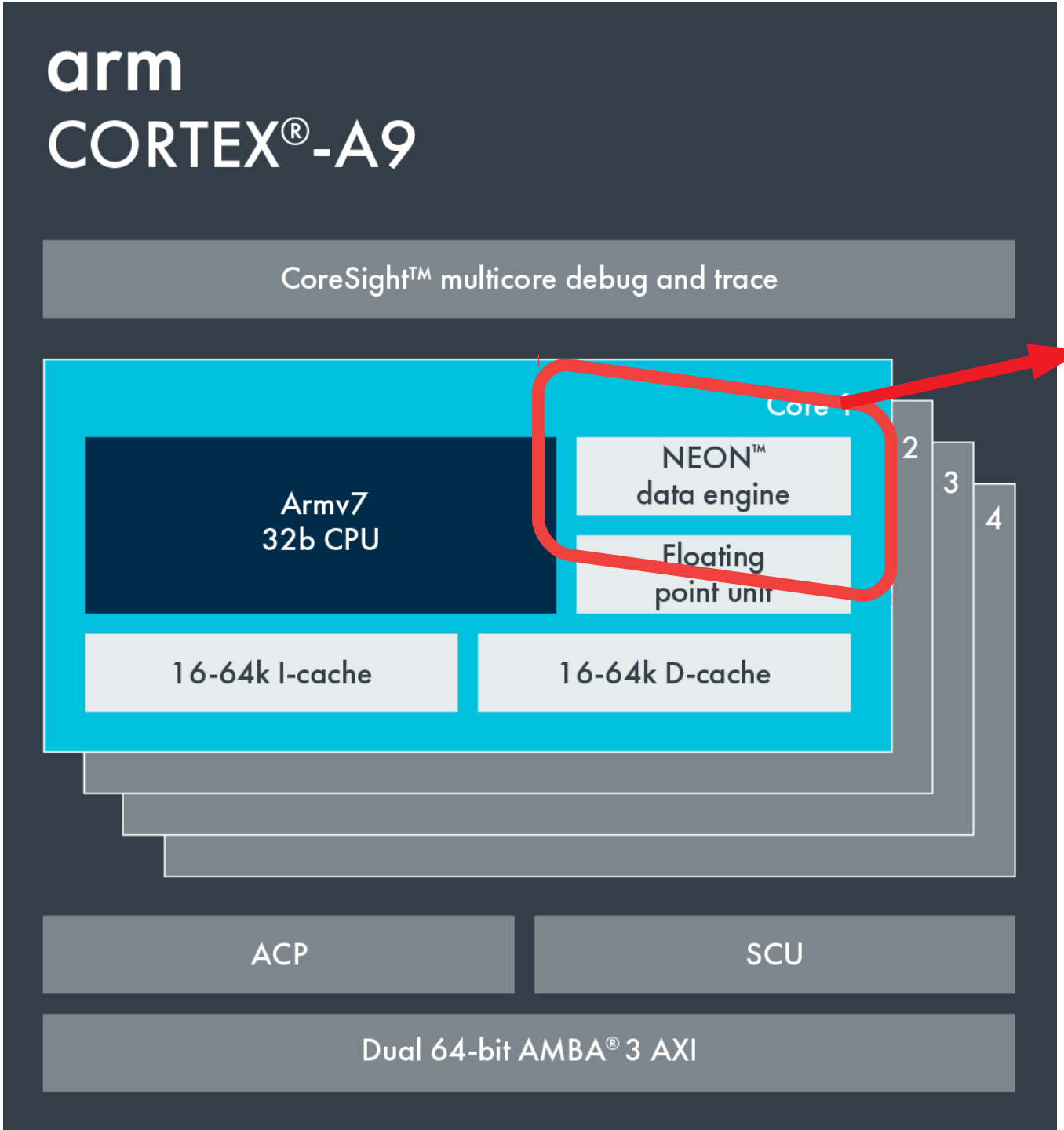


Single Instruction
MULTIPLE Data

Same processing instruction runs on all processors

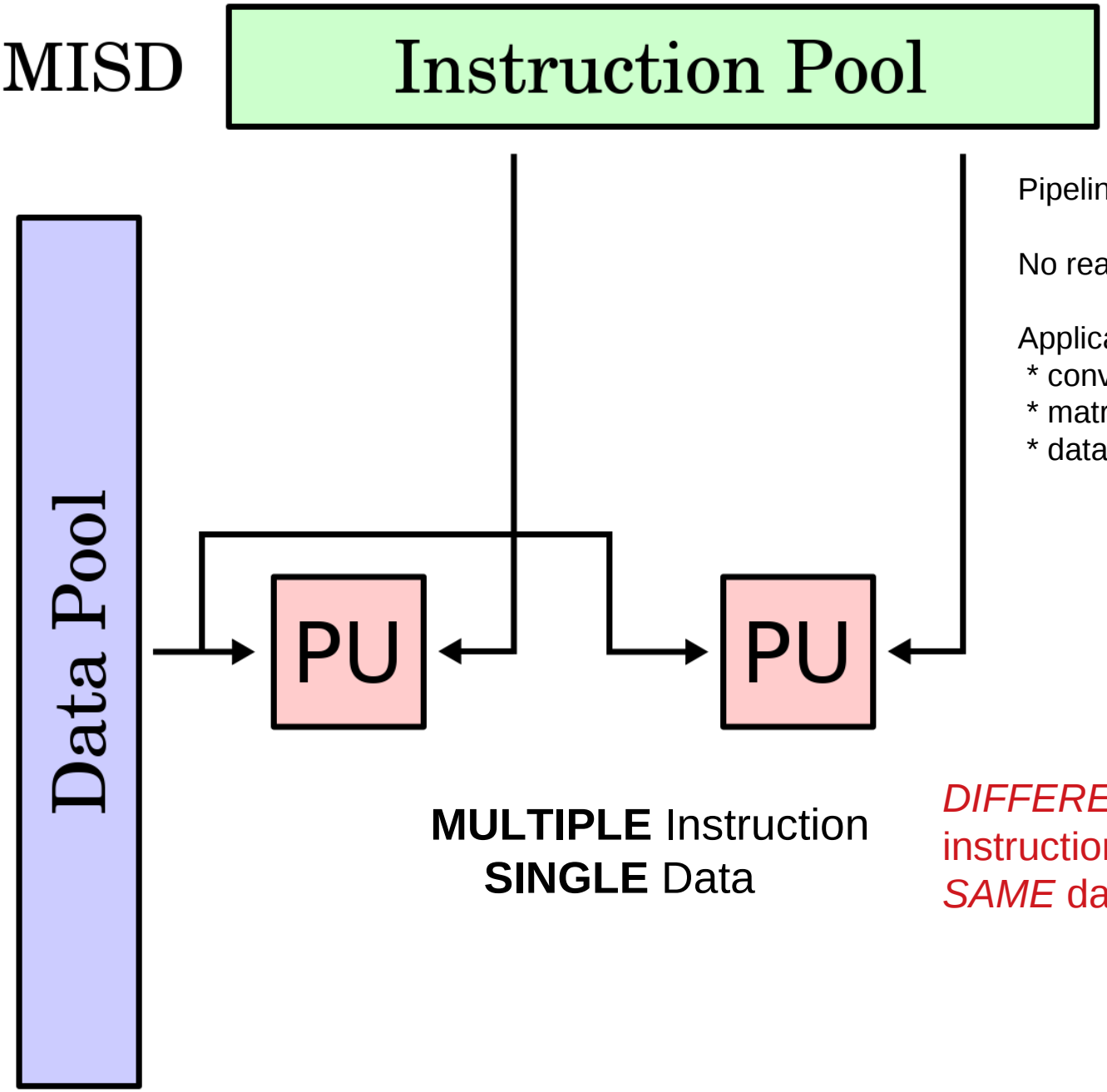
Data level parallelism
NOT Concurrency

Applications:
* Image editing
* Multimedia processing



Arm NEON technology is an advanced **SIMD (single instruction multiple data)** architecture extension for the Arm Cortex-A series

MISD



Pipelining!!!

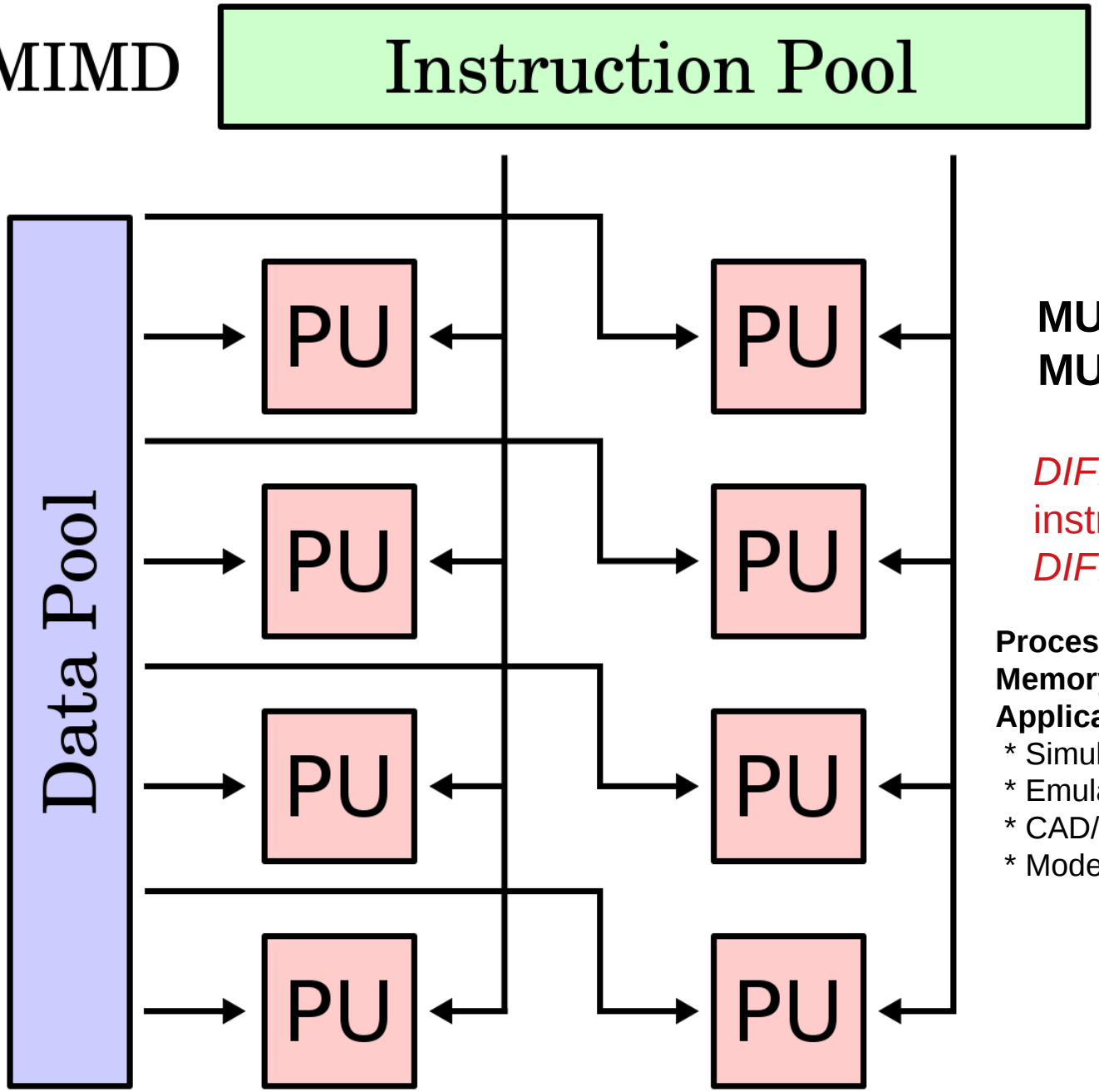
No real example in real life

Applications:
* convolution
* matrix operations
* data sorting

MULTIPLE Instruction
SINGLE Data

DIFFERENT processing instructions run on *SAME* data

MIMD

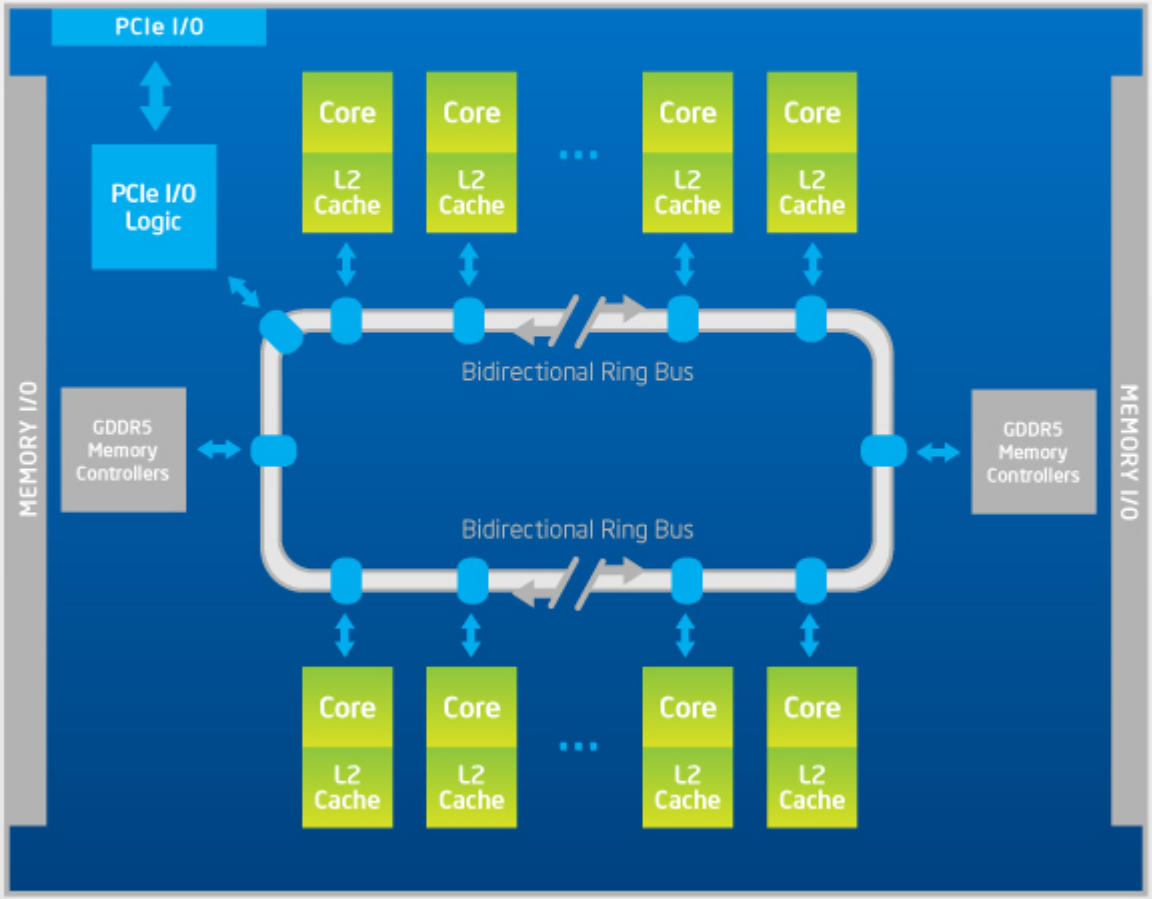


MULTIPLE Instruction
MULTIPLE Data

DIFFERENT processing instructions can run on *DIFFERENT* data

Processing: asynch, independent
Memory: shared or distributed
Applications:
* Simulation
* Emulation (VM)
* CAD/CAM
* Modeling

Intel® Xeon Phi™ Coprocessor Block Diagram



More MIMD

SPMD

- Same *program* multiple data
- Program executed at independent execution points
- Most common style of parallel programming

MPMD

- Multiple *program* multiple data
- At least 2 programs
- One program is master/controller
- Others ‘nodes’ receive program from master

SPMD

Single Program Multiple Data (SPMD)

Hasso Plattner Institut

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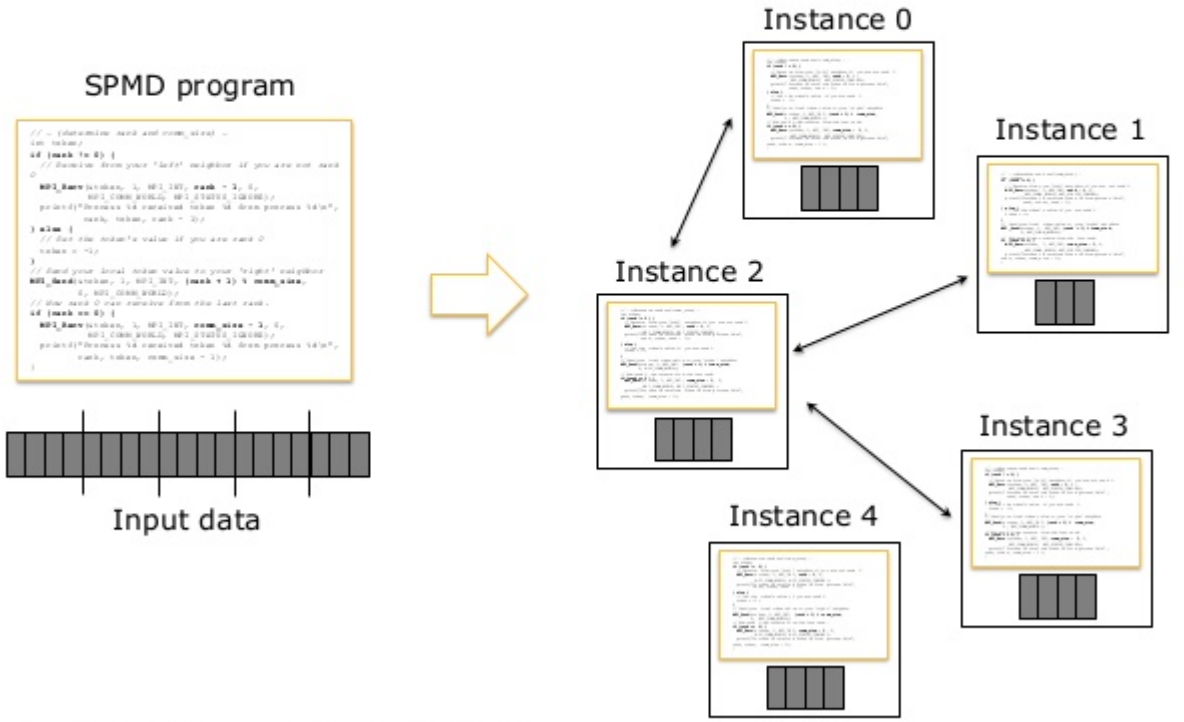
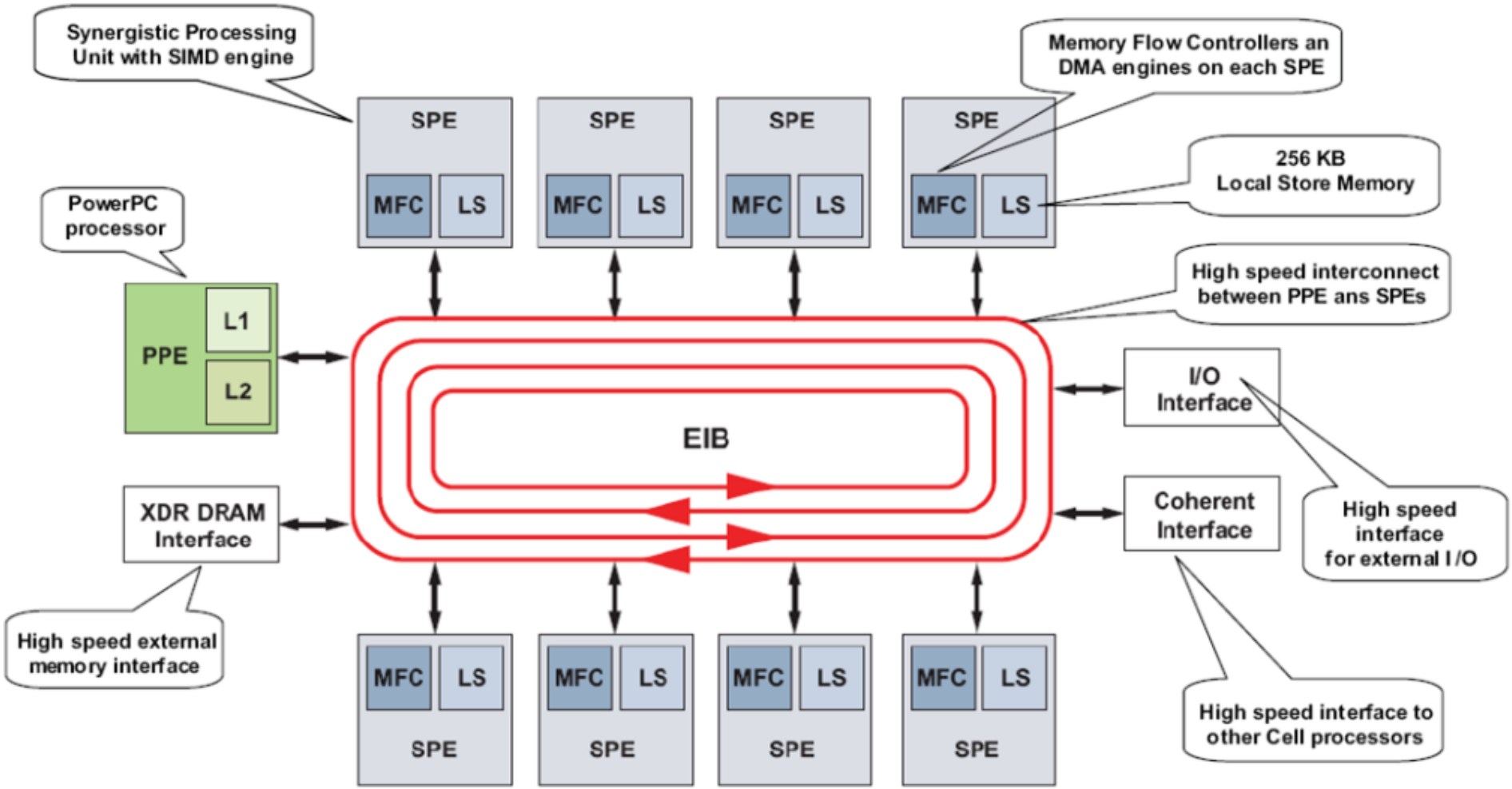


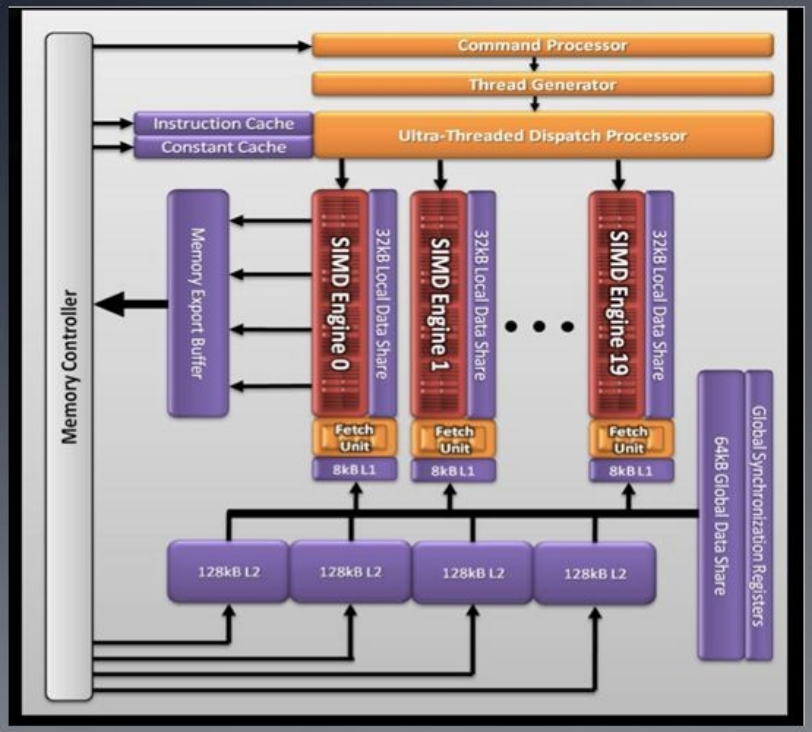
Playstation 3 – Cell Processor (MPMD)



Pop Quiz!

What architecture is this???

AMD GPU Hardware Architecture



- AMD 5870 – Cypress
- 20 SIMD engines
- 16 SIMD units per core
- 5 multiply-adds per functional unit (VLIW processing)
- 2.72 Teraflops Single Precision
- 544 Gigaflops Double Precision

Source: Introductory OpenCL *SAAHPC2010*, Benedict R. Gaster

Flynn's Taxonomy

- quite difficult to fit parallel architectures
  - Ancient – 1966!!!
  - Where do these fit??? <<< UNCLEAR
    - instruction level parallel
    - fine-grain speculative multithreading
- Most important distinction is between SIMD and MIMD