AVR 8-bit Microcontrollers

AVR42785: I/O Multiplexing Introduction with ATmega328PB

APPLICATION NOTE

Introduction

This application note describes how to configure the Atmel® ATmega328PB physical I/O pins as general purpose I/O or alternative peripheral function pins. A code example based on the ATmega328PB Xplained Mini kit can be downloaded from Atmel Start.

Features

- I/O port multiplexing
- GPIO configuration
- External interrupt pin configuration
- Oscillator/reset pin configuration
- Timer/counter pin configuration
- ADC pin configuration
- Analog comparator pin configuration
- PTC touch pin configuration
- TWI pin configuration
- SPI pin configuration
- USART pin configuration

Table of Contents

1. I/O Port Multiplexing

Each pin of ATmega328PB is default controlled as a general purpose I/O and can be alternatively assigned to one of the peripheral functions. The table below describes the peripheral signals multiplexed to the PORT I/O pins.

Table 1-1. Port Function Multiplexing

No	PAD	EXINT	PCINT	ADC/ AC	PTC X	PTC Y	OSC	T/C #0	T/C #1	USART	I^2C	SPI
1	PD[3]	INT1	PCINT19		X3	Y11		OC2A				
2	PD[4]		PCINT20		X4	Y12		T0		XCK0		
3	PE[0]		PCINT24	ACO	X8	Y16			ICP4		SDA1	
4	VCC											
5	GND											
6	PE[1]		PCINT25		X9	Y17			TC4		SCL1	
7	PB[6]		PCINT6				XTAL1/ TOSC1					
8	PB[7]		PCINT7				XTAL2/ TOSC2					
9	PD[5]		PCINT21		X5	Y13		OC0B	T1			
10	PD[6]		PCINT22	AIN0	X6	Y14		OC0A				
11	PD[7]		PCINT23	AIN1	X7	Y15						
12	PB[0]		PCINT0		X10	Y18	CLKO	ICP1				
13	PB[1]		PCINT1		X11	Y19		OC1A				
14	PB[2]		PCINT2		X12	Y20		OC1B				SS0
15	PB[3]		PCINT3		X13	Y21		OC2A		TXD1		MOSI0
16	PB[4]		PCINT4		X14	Y22				RXD1		MISO0
17	PB[5]		PCINT5		X15	Y23				XCK1		SCK0
18	AVCC											
19	PE[2]		PCINT26	ADC6		Y6		ICP3				SS1
20	AREF											
21	GND											
22	PE[3]		PCINT27	ADC7		Y7		T3				MOSI1
23	PC[0]		PCINT8	ADC0		Y0						MISO1
24	PC[1]		PCINT9	ADC1		Y1						SCK1
25	PC[2]		PCINT10	ADC2		Y2						
26	PC[3]		PCINT11	ADC3		Y3						

No	PAD	EXINT	PCINT	ADC/ AC	PTC X	PTC Y	OSC	T/C #0	T/C #1	USART	I^2C	SPI
27	PC[4]		PCINT12	ADC4		Y4					SDA0	
28	PC[5]		PCINT13	ADC5		Y5					SCL0	
29	PC[6]/ Reset		PCINT14									
30	PD[0]		PCINT16		X0	Y8		OC3A		RXD0		
31	PD[1]		PCINT17		X1	Y9			OC4A	TXD0		
32	PD[2]		PCINT18		X2	Y10		OC3B	OC4B			

2. GPIO Configuration

2.1. Overview

ATmega328PB ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction, output drive value, or input pull-up enabling/disabling of one port pin can be changed without unintentionally changing other port pins. Most port pins are multiplexed with alternate functions for the peripheral features on the device. Enabling the alternate function of some of the port pins does not affect the use of the other pins in the port as general digital I/O.

2.2. Register Description

Each port pin consists of three register bits; DDRxn, PORTxn, and PINxn (x is port number, n is bit number). DDRxn is port pin input/output direction register, PORTxn is port pin data register, and PINxn is port pin input register.

The DDRxn bit in the DDRx register selects the direction of this pin. If DDxn is written to '1', Pxn is configured as an output pin. If DDxn is written to '0', Pxn is configured as an input pin.

When the pin is configured as an output pin, if PORTxn is written to '1', the port pin is driven high; if PORTxn is written '0', the port pin is driven low.

The table below summarizes the control signals for the pin value.

Table 2-1. Table 3-1: Port Pin Configurations

DDRxn	PORTxn	PUD (pull-up disable, in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	YES	Pxn will source current if ext. pulled low
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

2.3. Configuration Code Example

```
unsigned char i;

...

/*Set outputs high */

PORTB = (1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0);

/* Define directions for port pins */
```

```
DDRB = (1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0);
no_operation();
/* Read port pins */
i = PINB;
...
```

3. External Interrupt Pin Configuration

3.1. Overview

For ATmega328PB, external Interrupts can be triggered by the INT0, INT1 pin, or any of the PCINT pins. The INT0, INT1 interrupts can be triggered by falling edge, rising edge, or low level, or any logical change, while the PCINT pins can only be triggered by enabled PCINT pin level toggle.

3.2. External INT0, INT1 Pin Configuration

To enable external INT0, INT1 pin interrupt function enable, EICRA (external interrupt control register A) register should be configured to select the sensing mode – falling edge, rising edge, logic change, or low level, and enable INT0, INT1 interrupt request bits of the EIMSK (external interrupt mask register).

Figure 3-1. External Interrupt Control Register A

Name: EICRA
Offset: 0x69
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					ISC11	ISC10	ISC01	ISC00

Bits 3:2 – ISC1n: Interrupt Sense Control 1 [n = 1:0]

Value	Description
00	The low level of INT1 generates an interrupt request
01	Any logical change on INT1 generates an interrupt request
10	The falling edge of INT1 generates an interrupt request
11	The rising edge of INT1 generates an interrupt request

Bits 1:0 – ISC0n: Interrupt Sense Control 0 [n = 1:0]

Value	Description
00	The low level of INT0 generates an interrupt request
01	Any logical change on INT0 generates an interrupt request
10	The falling edge of INT0 generates an interrupt request
11	The rising edge of INT0 generates an interrupt request

Figure 3-2. External Interrupt Mask Register

Name: EIMSK
Offset: 0x3D
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x1D

Bit	7	6	5	4	3	2	1	0
							INT1	INT0

Bit 1 – INT1: External Interrupt Request 1 Enable.

Bit 0 – INT0: External Interrupt Request 0 Enable.

3.3. External INT0 Configuration Code Example

```
/* Disable CPU IRQ*/
cli();
/* Rising edge of INT0 to trigger interrupt*/
EICRA |= 0x03;
/*INT0 interrupt enable*/
EIMSK |= 0x01;
...
/* Enable CPU IRQ*/
sei();
```

3.4. Pin Change Interrupt Configuration

For enabling a PCINT pin change interrupt function, first the pin direction input mode must be configured; secondly, it needs to set the PCINTn bit to “1” in the PCMSK register, and finally it needs to set the corresponding PCIE0~3 bit in PCICR register.

Figure 3-3. Pin Change Interrupt Control Register

Name: PCICR
Offset: 0x68
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					PCIE3	PCIE2	PCIE1	PCIE0

Bit 3 – PCIE3: Pin Change Interrupt Enable 3

When the PCIE3 bit is set, any change on any enabled PCINT[27:24] pin will cause an interrupt. PCINT[27:24] pins are enabled individually by the PCMSK3 Register.

Bit 2 – PCIE2: Pin Change Interrupt Enable 2

When the PCIE2 bit is set, any change on any enabled PCINT[23:16] pin will cause an interrupt. PCINT[23:16] pins are enabled individually by the PCMSK2 Register.

Bit 1 – PCIE1: Pin Change Interrupt Enable 1

When the PCIE1 bit is set, any change on any enabled PCINT[15:8] pin will cause an interrupt. PCINT[15:8] pins are enabled individually by the PCMSK1 Register.

Bit 0 – PCIE0: Pin Change Interrupt Enable 0

When the PCIE0 bit is set, any change on any enabled PCINT[7:0] pin will cause an interrupt.

PCINT[7:0] pins are enabled individually by the PCMSK0 Register.

4. Oscillator/reset Pin Configuration

4.1. XTAL1,XTAL2 Pin Configuration

For the ATmega328PB device, the PB6,PB7 can be multiplexed into the XTAL1,XTAL2 pin of internal inverting oscillator amplifier with clock fuse setting to Crystal oscillator as shown in the table below. As the table shows, an external clock can be input from the XTAL1 pin once the CKSEL fuse is programmed to “External clock” option.

Table 4-1. Device Clocking Options Select

Device clocking option	CKSEL[3:0]
Low Power Crystal Oscillator	1111 - 1000
Low Frequency Crystal Oscillator	0101 – 0100
Internal 128kHz RC Oscillator	0011
Calibrated Internal RC Oscillator	0010
External Clock	0000
Reserved	0001

4.2. TOSC1,TOSC2 Pin Configuration

Except multiplexing internal inverting amplifier oscillator XTAL1,XTAL2 pins, the PB6,PB7 can also be used as Timer2/Counter2 oscillator TOSC1,TOSC2 pins. The Timer/Counter Oscillator can only be used when the Calibrated Internal RC Oscillator is selected as system clock source. So for the TOSC multiplexing function selection, it needs to program the CKSEL fuse to “calibrated internal RC oscillator” and AS2 bit in ASSR register for enabling asynchronous clocking of Timer2/Counter2.

The Timer2/Counter2 clock can also be input externally. Once the “EXCLK” bit in the ASSR register is set, the external clock can be input from the TOSC1 pin.

Figure 4-1. Asynchronous Status Register

Name: ASSR
Offset: 0xB6
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB

Bit 6 – EXCLK: Enable External Clock Input

When EXCLK is written to one, and asynchronous clock is selected, the external clock input buffer is enabled and an external clock can be input on Timer Oscillator 1 (TOSC1) pin instead of a 32kHz crystal.

Bit 5 – AS2: Asynchronous Timer/Counter2

When AS2 is written to zero, Timer/Counter2 is clocked from the I/O clock, clkI/O. When AS2 is written to one, Timer/Counter2 is clocked from a crystal Oscillator connected to the Timer Oscillator pin.

4.3. CLKO Pin Configuration

Once the CKOUT fuse is programmed, the PB0 will be the system clock output pin.

4.4. Reset Pin Configuration

If the RSTDISBL fuse is programmed, the PC6/RESET is used as I/O pin; if the RSTDISBL fuse is unprogrammed, the PC6 is used as reset pin.

5. Timer/Counter Pin Configuration

5.1. Input Capture Pin--ICPn Configuration

The Input Capture Register can capture the Timer/Counter value when a change of the logic level (an event) occurs on either the Input Capture pin (ICPn) or alternatively on the Analog Comparator output (ACO). To select the ICPn pin, the ACSR.ACIC should first be cleared to disable the Analog Comparator input capture function. Secondly, the users need to set the WGM[3:0] value for choosing the Timer/ counter operation mode not using the ICRn register as Timer/counter TOP value. For more information about WGM[3:0] setting, see the table below.

Table 5-1. Waveform Generation Mode Bit Description

WGM[3:0]	Timer/Counter mode of operation	TOP
0	Normal	0xFFFF
1	PWM,Phase Correct, 8 BIT	0x0FFF
2	PWM, Phase Correct, 9 BIT	0x01FF
3	PWM, Phase Correct, 10 BIT	0x03FF
4	CTC	OCR4A
5	Fast PWM, 8 BIT	0x00FF
6	Fast PWM, 9 BIT	0x01FF
7	Fast PWM, 10 BIT	0x03FF
8	PWM, Phase, and Frequency Correct	ICR1
9	PWM, Phase, and Frequency Correct	OCR4A
10	PWM, Phase, and Frequency Correct	ICR1
11	PWM, Phase, and Frequency Correct	OCR4A
12	CTC	ICR1
13	Reserved	-
14	Fast PWM	ICR1
15	Fast PWM	OCR4A

Figure 5-1. Analog Comparator Control and Status Register

Name: ACSR
Offset: 0x50
Reset: N/A
Property: When addressing as I/O Register: address offset is 0x30

Bit	7	6	5	4	3	2	1	0
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0

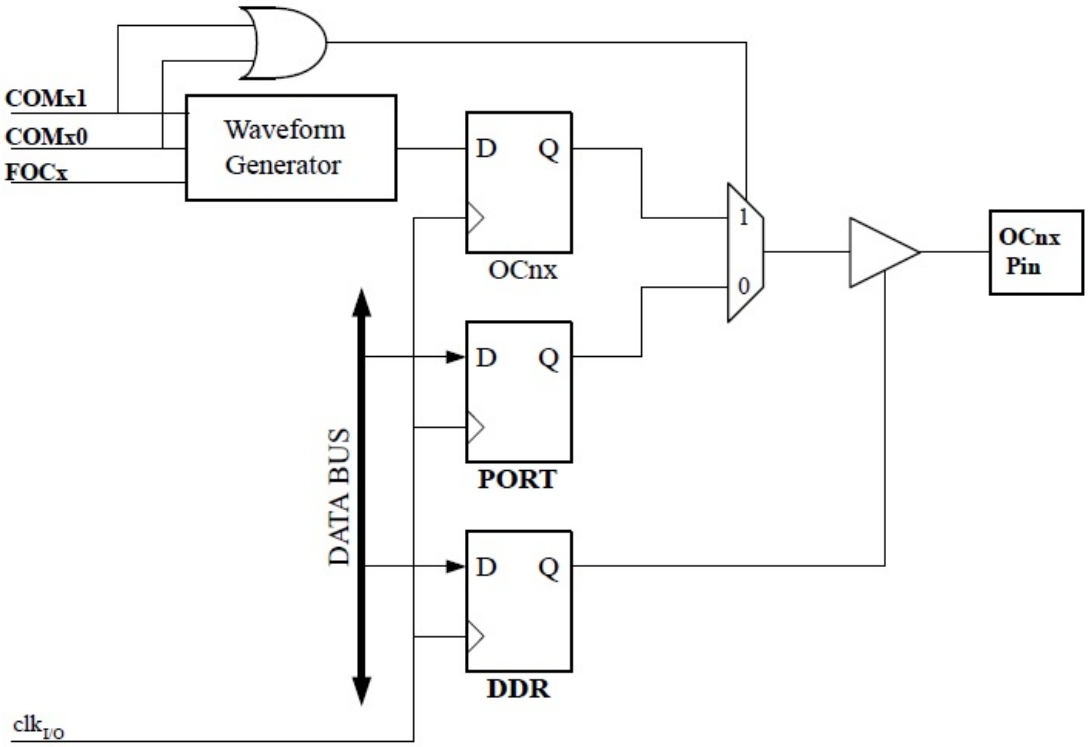
Bit 2 – ACIC: Analog Comparator Input Capture Enable

When written logic one, this bit enables the input capture function in Timer/Counter to be triggered by the Analog Comparator; When written logic zero, no connection between the Analog Comparator and the input capture function exists.

5.2. Output Compare Match Output Pin--OCnA,OCnB Configuration

5.2.1. Register Description

Figure 5-2. Compare Match Output Unit, Schematic



As the above figure shows, the OCnA,OCnB pin behavior depends on both COMx[1:0] bits settings in the TCCRnA register and compare output (OCnX) from waveform generator, which is controlled by the WGM[3:0] bits setting in the TCCRnA, TCCRnB registers. However, the OCnx pin direction (input or output) is still controlled by the Data Direction Register (DDR). For altering to compare output function, DDR_OCnx should be set output.

Figure 5-3. Timer/Counter Control Register A

Name: TCCRnA
Offset: 0x80 + n*0x10 [n=0..2]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	COMA[1:0]		COMB[1:0]				WGM[1:0]	

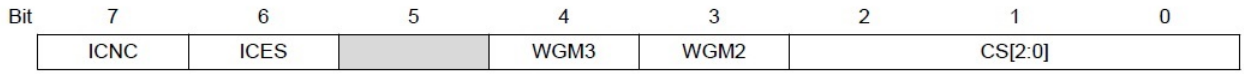
Bits 7:6 – COMA[1:0]: Compare Output Mode for Channel A [n = 1:0]

Bits 5:4 – COMB[1:0]: Compare Output Mode for Channel B [n = 1:0]

The COMA[1:0] and COMB[1:0] control the Output Compare pins (OCnA and OCnB respectively) behavior. If one or both of the COMA[1:0] bits are written to one, the OCnA output overrides the normal port functionality of the I/O pin it is connected to. If one or both of the COMB[1:0] bit are written to one, the OCnB output overrides the normal port functionality of the I/O pin it is connected to.

Figure 5-4. Timer/Counter Control Register B

Name: TCCRnB
Offset: 0x81 + n*0x10 [n=0..2]
Reset: 0x00
Property: -



Bits [1:0] of TCCRnA + Bits [4:3] of TCCRnB– WGM[3:0] bits control the counting sequence of the counter, the source for maximum (TOP) counter value, and what type of waveform generation to be used. The table below shows the COMx[1:0] bits functionality when the WGM[3:0] bits are set to normal mode or CTC mode. For more detailed description, refer to the ATmega328PB datasheet.

Table 5-2. Compare Output Mode, Non-PWM Mode

COMA1/COMB1	COMA0/COMB0	Description
0	0	Normal port operation, OCnA/OCnB disconnected
0	1	Toggle OCnA/OCnB on Compare Match
1	0	Clear OCnA/OCnB on Compare Match (set output to low level)
1	1	Set OCnA/OCnB on Compare Match (set output to high level)

5.2.2. Pin Configuration Example

This example configures Timer1/Counter1 normal mode and toggling PB1/OC1A pin when compare match.

```
……..

/* Set PB1/OC1A pin output direction */

DDR1B |= 0x02;

/* Configure TC1 normal mode, toggling OC1A pin when compare match */

TCCR1A = 0x40;

TCCR1B = 0x01;

……
```

5.3. External Timer/Counter Clock Source--T0,T1,T3,T4 Pin Configuration

For TC0/1/3/4, the external clock source can be applied on the T0/1/3/4 pin by configuring the CS[2:0] bits of the TCCRnB register to "111" or "110".

Figure 5-5. Timer/Counter Control Register B

Name: TCCRnB
Offset: 0x81 + n*0x10 [n=0..2]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ICNC	ICES		WGM3	WGM2	CS[2:0]		

CS[2:0]—Clock selection bits description

CS2	CS1	CS0	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	clkI/O/1 (no prescaling)
0	1	0	clkI/O/8 (from prescaler)
0	1	1	clkI/O/64 (from prescaler)
1	0	0	clkI/O/256 (from prescaler)
1	0	1	clkI/O/1024 (from prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

6. ADC Pin Configuration

After setting the ADEN bit of the ADC control status register A, port PC[5:0],PE2,PE3 can be used as ADC input pin ADC[7:0] by configuring the MUX bits of the ADMUX register.

Figure 6-1. ADC Control Status Register A

Name: ADCSRA
Offset: 0x7A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0

Bit 7 – ADEN: ADC Enable

Figure 6-2. ADC Multiplexer Selection Register

Name: ADMUX
Offset: 0x7C
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	REFS1	REFS0	ADLAR		MUX3	MUX2	MUX1	MUX0

Bits 3:0—MUXn: Analog Channel Selection[n=3:0]

The value of these bits selects which analog inputs are connected to the ADC as the following table.

MUX[3:0]	Single ended input
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6
0111	ADC7
1000	Temperature sensor
1001	Reserved
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved

MUX[3:0]	Single ended input
1110	1.1V (VBG)
1111	0V (GND)

7. Analog Comparator Pin Configuration

The analog comparator compares the positive pin AIN0 and negative pin AIN1, and output compare result on ACO.

7.1. Comparator Output-ACO Pin Configuration

When the ACOE bit in the analog comparator control and status B (ACSRB) register is set, port PE0 pin will alter to analog compare output ACO pin.

Figure 7-1. Analog Comparator Control and Status Register B

Name: ACSRB
Offset: 0x4F
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x2F

Bit	7	6	5	4	3	2	1	0
								ACOE

Bit 0 – ACOE: Analog Comparator Output Enable

7.2. Positive Input-AIN0 Pin Configuration

When the ACBG bit of the ACSR is cleared, the AIN0 pin is applied to the positive input of the Analog Comparator.

Figure 7-2. Analog Comparator Control and Status Register

Name: ACSR
Offset: 0x50
Reset: N/A
Property: When addressing as I/O Register: address offset is 0x30

Bit	7	6	5	4	3	2	1	0
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0

Bit 7 – ACD: Analog Comparator Disable

This bit can be set at any time to turn off the Analog Comparator.

Bit 6 – ACBG: Analog Comparator Bandgap Select

When this bit is cleared, AIN0 is applied to the positive input of the Analog Comparator; When this bit is set, a fixed bandgap reference voltage replaces the positive input to the Analog Comparator.

7.3. Negative Input-AIN1 Pin Configuration

Except AIN1 pin directly applied to negative input of analog comparator, any of the ADC[7..0] pins can also be applied to replace the negative input to the Analog Comparator, as shown in the table below. The ADC multiplexer is used to select this input, and consequently, the ADC must be switched off to utilize this feature. If the Analog Comparator Multiplexer Enable bit in the ADC Control and Status Register B

(ADCSRB.ACME) is '1' and the ADC is switched off (ADCSRA.ADEN=0), the three least significant Analog Channel Selection bits in the ADC Multiplexer Selection register (ADMUX.MUX[2..0]) select the input pin to replace the negative input to the Analog Comparator, when ADCSRB.ACME=0 or ADCSRA.ADEN=1, AIN1 is applied to the negative input of the Analog Comparator.

Table 7-1. Analog Comparator Multiplexed Negative Input

ACME	ADEN	MUX[2:0]	Analog Comparator Negative Input
0	x	xxx	AIN1
1	1	xxx	AIN1
1	0	000	ADC0
1	0	001	ADC1
1	0	010	ADC2
1	0	011	ADC3
1	0	100	ADC4
1	0	101	ADC5
1	0	110	ADC6
1	0	111	ADC7

8. PTC Touch Pin Configuration

The PTC module supports both self- and mutual-capacitance sensors. For mutual-capacitance mode, the PTC requires one X-pin to connect the X-pattern part of a mutual cap sensor and one Y-pin to connect the Y-pattern part of the mutual cap sensor. For self-capacitance mode, the PTC requires only one Y-pin to connect a touch sensor. The QTouch® library includes the touch sensor I/O configuration and other touch processing APIs to access the PTC. For more information on PTC touch design, refer to the Atmel Qtouch Library Peripheral Touch Controller User Guide.pdf.

9. TWI Pin Configuration

ATmega328PB has two TWI modules and each module has two pins; SDA and SCL. When the TWEN bit in the TWCRn is set (one) to enable the 2-wire Serial Interface, the pins are disconnected from the I/O port and become the Serial Clock (SCL) or Data (SDA). In this mode, there is a spike filter on the pin to suppress spikes shorter than 50ns on the input signal, and the pin is driven by an open drain driver with slew-rate limitation. Note that the internal pull-ups in the AVR® pads can be enabled by setting the PORT bits corresponding to the SCL and SDA pins, eliminating the need for external pull-up in some systems.

Figure 9-1. TWI Control Register n

Name: TWCRn
Offset: 0xBC + n*0x20 [n=0..1]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN		TWIE

Bit 2 – TWEN: TWI Enable

10. SPI Pin Configuration

10.1. Overview

ATmega328PB has two SPI peripherals. When SPI enable—SPE bit of SPI control register n—SPICRn is set, the SPI multiplexing I/O pins will be altered to SPI function, and the data direction of the MOSI, MISO, SCK, SS pins is overridden as shown in the table below. For the "User Defined" pin in the table, the users need to configure it to output direction; if the pin is forced by the SPI module to be an input, the pull-up can still be controlled by the port registers.

Table 10-1. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User defined	Input
MISO	Input	User defined
SCK	User defined	Input
SS	User defined	Input

10.2. SPI Configuration Example

The following code examples show how to initialize the ATmega328PB SPI as master or slave. The DDR_SPI needs to be replaced by the actual port direction registers, and the DD_SS, DD_MOSI, DD_MISO, and DD_SCK to be replaced by the actual port direction register bits. For example, if the MOSI0/PB3 pin is used as MOSI, replace the DDR_SPI with the DDRB, and the DD_MOSI with the DDB3.

SPI Master configuration code example:

```
void SPI_MasterInit(void)
{
/* Set SS, MOSI and SCK output, all others input */
DDR_SPI = (1<<DD_SS) |(1<<DD_MOSI)|(1<<DD_SCK);
/* Enable SPI, Master, set clock rate fck/16 */
SPCR = (1<<SPE)|(1<<MSTR)|(1<<SPR0);
}
```

SPI Slave configuration code example:

```
void SPI_SlaveInit(void)
{
/* Set MISO output, all others input */
DDR_SPI = (1<<DD_MISO);
/* Enable SPI */
SPCR = (1<<SPE);
```

```
}
```

11. USART Pin Configuration

The ATmega328PB USART peripheral supports three operation modes; asynchronous USART, synchronous USART, and Master SPI mode. The USART communication uses the TXD, RXD pin at asynchronous mode and uses the TXD, RXD, XCK pin at synchronous mode or Master SPI mode.

11.1. TXD,RXD Pin Configuration

When the TXEN,RXEN bit of the UCSRnB register is set, the TXD,RXD pin will be selected. When the USART Receiver is enabled, the RXD pin is configured as an input regardless of the value of the DDxn bit and the RXD pin pull-up can still be controlled by the PORTxn bit. When the USART Transmitter is enabled, the TXD pin is configured as an output regardless of the value of the DDxn bit.

Figure 11-1. USART Control and Status Register n

Name: UCSR0B, UCSR1B
Offset: 0xC1 + n*0x08 [n=0..1]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8

Bit 4 – RXEN: Receiver Enable

Writing this bit to one enables the USART Receiver. The Receiver will override normal port operation for the RxDn pin when enabled.

Bit 3 – TXEN: Transmitter Enable

Writing this bit to one enables the USART Transmitter. The Transmitter will override normal port operation for the TxDn pin when enabled.

11.2. XCK Pin Configuration

As the table Table 11-1 shows, when UMSEL[1:0] bits are set to "01", the USART will operate in master or slave synchronous mode; when UMSEL[1:0] bits are set to "11", the USART will operate at master SPI mode. When the USART operates at master synchronous or SPI mode, users need configure the XCK pin output direction; when the USART operates at slave synchronous mode, users need configure the XCK pin input direction.

Figure 11-2. USART Control and Status Register n C

Name: UCSR0C, UCSR1C
Offset: 0xC2 + n*0x08 [n=0..1]
Reset: 0x06
Property: -

Bit	7	6	5	4	3	2	1	0
	UMSEL[1:0]		UPM[1:0]		USBS	UCSZ1 / UDORD	UCSZ0 / UCPHA	UCPOL

Bits 7:6 – UMSEL[1:0]: USART Mode Select as shown in the table below.

Table 11-1. USART Mode Selection

UMSEL[1:0]	Mode
00	Asynchronous USART
01	Synchronous USART
10	Reserved
11	Master SPI (MSPIM)

12. Example Project

This application note provides a code example to show GPIO configuration and I/O pin change interrupt enabling on ATmega328PB. The source code is available for download from Atmel START. An ATmega328PB kit is used to demonstrate the example project.

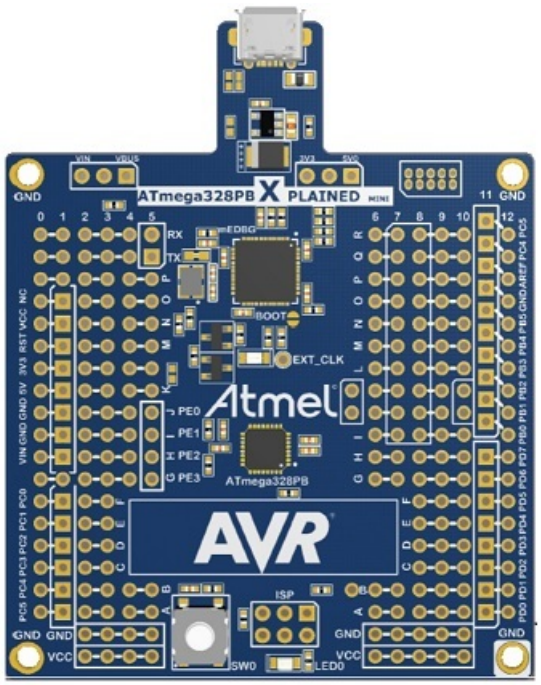
12.1. Prerequisites

The example project discussed in this document requires:

- Atmel Studio 7.0 or later
- ATmega328PB Xplained Mini kit
- Example Source Code downloaded from Atmel START

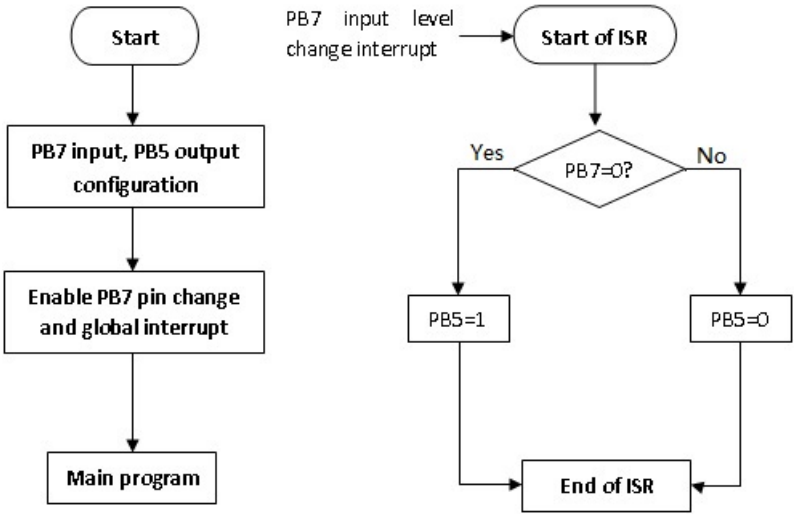
12.2. ATmega328PB Xplained Mini Kit Introduction

The ATmega328PB Xplained Mini evaluation kit is a hardware platform to evaluate the ATmega328PB microcontroller. The evaluation kit integrates a mechanical button, which connects to PB7 and a LED which connects to PB5 of the ATmega328PB chip. For more details about this kit, refer to the ATmega328PB_Mini_Kit_User_Guide.pdf.



12.3. Project Introduction

This example uses the port pin change interrupt feature to monitor the PB7 level change. Every PB7 level change will trigger an interrupt to change the PB5 output according to the PB7 level status. The following is an example application firmware flow.


Start
PB7 input, PB5 output configuration
Enable PB7 pin change and global interrupt
Main program
PB7 input level change interrupt
Start of ISR
Yes
PB7=0?
No
PB5=1
PB5=0
End of ISR

13. References

- ATmega328PB datasheet (http://www.atmel.com/devices/ATMEGA328PB.aspx)
- ATmega328PB Xplained Mini kit (http://www.atmel.com/tools/MEGA328PB-XMINI.aspx)
- Atmel Studio (http://www.atmel.com/tools/atmelstudio.aspx?tab=overview)
- Atmel START (http://start.atmel.com)

14. Revision history

Doc. Rev.	Date	Comments
42785A	10/2016	Initial document release

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