Team BIB Reference Data

Core Instruction Set:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Format | Mnemonic | Operation (Verilog) | OP / FUNCT |
| Add | R | add | R[rd] = R[rs] + R[rt] | 0 / 000 |
| Add immediate | I | addi | R[rt] = R[rs] + immediate | 011 |
| And | R | and | R[rd] = R[rs] & R[rt] | 0 / 010 |
| Branch on Equal | I | beq | if(R[rs] == R[rt])  PC = 2 + BranchAddr | 100 |
| Jump | J | jump | PC = jumpaddr | 110 |
| Load Word | I | lw | R[rt] = M(R[rs]) | 001 |
| Nor | R | nor | R[rd] = ~(R[rs] | R[rt]) | 0 / 101 |
| Or | R | or | R[rd] = R[rs] | R[rt] | 0 / 011 |
| Set less than | R | slt | R[rd] = (R[rs] < R[rt]) ? 1 : 0 | 0 / 100 |
| Set less than imm. | I | slti | R[rt] = (R[rs] < immediate) ? 1 : 0 | 101 |
| Subtract | R | sub | R[rd] = R[rs] – R[rt] | 0 / 001 |
| Store word | I | sw | M(R[rs]) = R[rt] | 010 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction sets | | | | | |
| Instruction | 3 bits | 3 bits | 3 bits | 3 bits | 4 bits |
| R Type | op code | rs | rt | rd | funct |
| I Type | op code | rs | rt | Address / immediate | |
| J Type | op code | address | | | |

|  |  |  |
| --- | --- | --- |
| Register | Number | Use |
| $zero | 0 | Constant value zero |
| $t1 | 1 | Temporary register #1 |
| $t2 | 2 | Temporary register #2 |
| $t3 | 3 | Temporary register #3 |
| $s1 | 4 | Saved temporary register #1 |
| $s2 | 5 | Saved temporary register #1 |
| $s3 | 6 | Saved temporary register #1 |
| $ra | 7 | Return address |

Other useful values, controls, operations, and codes.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Control Values | | | | | | | | |
| Instruction | Reg Write | Reg Dest | ALU Src | Branch | Mem Write | Mem to Reg | Jump | ALU op |
| R-type | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 00 |
| LW | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 11 |
| SW | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 11 |
| Addi | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 11 |
| BEQ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10 |
| STLI | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 01 |
| jump | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 00 |

|  |  |  |  |
| --- | --- | --- | --- |
| ALU controls | | | |
| Alu control | Alu op code | function | Alu control value |
| addi | 11 | xxxx | 000 |
| subi | 10 | xxxx | 001 |
| slti | 01 | xxxx | 010 |
| add | 00 | 0000 | 000 |
| sub | 00 | 0001 | 001 |
| and | 00 | 0010 | 010 |
| or | 00 | 0011 | 011 |
| slt | 00 | 0100 | 100 |
| nor | 00 | 0101 | 101 |

|  |  |
| --- | --- |
| Operations and OP Codes | |
| Operation | Opcode |
| R-type instruction | 000 |
| I: Load Word | 001 |
| I: Store Word | 010 |
| I: addi | 011 |
| I: branch equal | 100 |
| I: set if less than immediate | 101 |
| J: jump | 110 |