Darius Fantozzi and Alvee Ahmed 5/11/24
ECE251 ISA Documentation

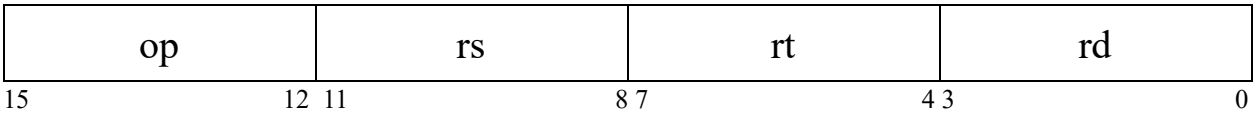
Team Nah We'd Know Verilog Green Card

Instruction Set

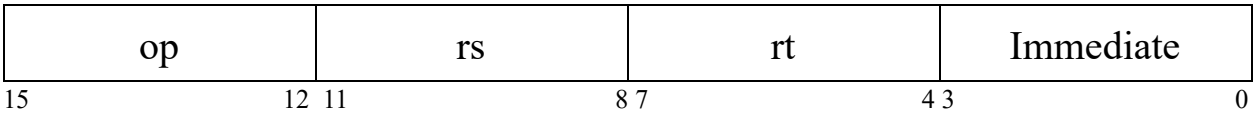
OpCode	Instruction	Type	Function Description
0000	add	R	R[rd] = R[rs] + R[rt]
0001	or	R	R[rd] = R[rs] OR R[rt]
0010	slt	R	R[rd] = (R[rs] < R[rt]) ? 1 : 0
0011	and	R	R[rd] = R[rs] AND R[rt]
0100	addi	I	R[rt] = R[rs] + SignExtImm
0101	ori	I	R[rt] = R[rs] OR SignExtImm
0110	lw	I	R[rt] = M[R[rs] + SignExtImm]
0111	sw	I	M[R[rs]+SignExtImm] = R[rt]
1000	sll	R	R[rd] = R[rs] << R[rt]
1001	srl	R	R[rd] = R[rs] >> R[rt]
1010	sub	R	R[rd] = R[rs] - R[rt]
1011	nor	R	R[rd] = ~(R[rs] OR R[rt])
1100	j	J	PC = R[rs] + Address
1101	save	S	R[rs] = PC
1110	N/A	X	Illegal Operation
1111	beq	I	PC = (R[rs] == R[rt]) ? (PC + 1 + SignExtImm) : (PC + 1)

Instruction Formats

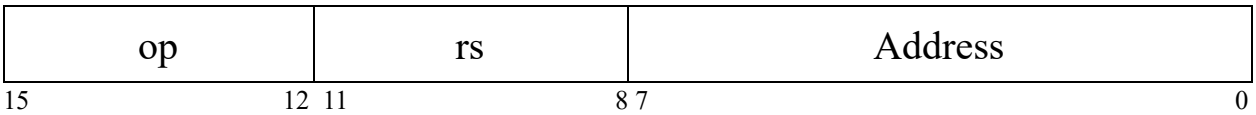
R-Type:



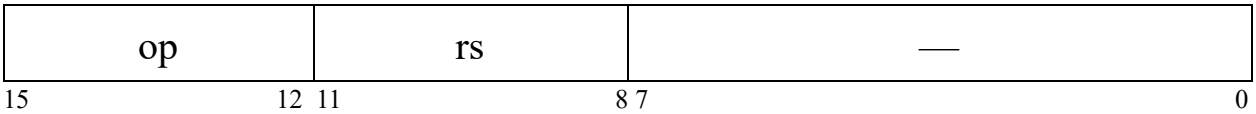
I-Type:



J-Type:



S-Type:



Registers

Register #	Register Name
0	$zero
1 - 4	$s0 - $s3
5 - 8	$t0 - $t3
9 - 12	$a0- $a3
13	$v0
14	$sp
15	$ra