

NWEN 303 Assignment 2

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1 Readers and Writers

1.1 a

For this problem we only need modify the StartR and EndR operations

```
1: procedure STARTR
2:   if  $nw \neq 0$  then waitC(OKR)
3:    $nr \leftarrow nr + 1$ 
4:    $signalC(OKR)$ 
5: procedure ENDR
6:    $nr \leftarrow nr + 1$ 
7:   if  $nr == 0$  then signalC(OKW)
```

When a process starts a read and gains permission to read then nr is incremented by 1.

If there are currently processes reading then $nr > 0$. If another process attempts to start a read then as $nr > 0$ we know $nw = 0$ the process will be allowed to read even if there are writers waiting. So we see the rule is satisfy.

1.2 b

For this problem we only need to modify the EndW operations

```
1: procedure ENDW
2:    $nw \leftarrow nw - 1$ 
3:   if  $empty(OKW)$  then
4:      $signalC(OKR)$ 
5:   else
6:      $signalC(OKW)$ 
```

When ever we end write operation we first check if there are any processes waiting on the OKW condition, if there are none then we will signal a read process. Otherwise we signal a write process. Giving any waiting write process priority. Satisfying the rule.

1.3 c

For this problem we need to modify the monitor init, EndR and EndW operations.

```
1: procedure MONITOR RW
2:   int nr  $\leftarrow$  0
3:   int nw  $\leftarrow$  0
4:   int writeCount  $\leftarrow$  0
5:   cond OKR OKW
6: procedure ENDR
7:   nr  $\leftarrow$  nr - 1
8:   writeCount  $\leftarrow$  0
9:   if nr == 0 then
10:    signalC(OKW)
11: procedure ENDW
12:   nw  $\leftarrow$  nw - 1
13:   writeCount  $\leftarrow$  writeCount + 1
14:   if writeCount  $\geq$  2 or empty(OKW) then
15:    writeCount  $\leftarrow$  0
16:    signalC(OKR)
17:   else
18:    signalC(OKW)
```

When ever a write ends we increment the writeCount variable by 1. If this variable ever reaches 2 then we have reached the write limits so we reset it to 0 and signal a read process. We see this satisfy the rule as only two consecutive writes can occur.

2 Critical Section Problem

2.1 a

We define a monitor and two operations, Start and End. We will use the monitor to track how many processes are in there critical section at a time.

```

1: procedure MONITOR C
2:    $n \leftarrow 0$ 
3:   cond OK
4: procedure START
5:   if  $n = M$  then
6:     waitC(OK)
7:    $n \leftarrow n + 1$ 
8: procedure END
9:    $n \leftarrow n - 1$ 
10:  signalC(OK)

```

We want to show that only M processes can be in there critical section at once. When a process calls the start operation, the count is incremented. If a process is uses the start operation when there are already M processes with access then the process waits for the OK condition to be signaled. The OK condition is signaled when one process calls the End operation. Meaning there can only be at most M processes in there critical section at once.

2.2 b

```

1: procedure SEMAPHORE S
2:    $s.value \leftarrow M$ 
3:    $s.waitSet \leftarrow \{\}$ 
4: procedure PROCESS
5:   while true do
6:     non critical section
7:     wait(S)
8:     critical section
9:     signal(S)

```

We create a semaphore with a value of M (so there are M permissions). And we initialize the wait set to empty. We see this must satisfy the give rule. Any process attempting to gain a permission will be blocked (and added to the wait set) if the semaphore has already given out M permissions. When another process exits its critical section it will signal the semaphore, giving its permission to another process.

3 Producers and Consumers Revisited

We use a monitor to solve this problem, with a signaling policy of signal and continue. We have a buffer of size N . We want this buffer (of size K) to be circular, so when the head (or tail) reaches the end it should wrap around to overwrite old elements that we have "removed". So we will assume our monitor has two functions $increment(i, K)$ which will increment i and if it is equal to K reset it to 0. and $size$ which will give us the number of elements in the buffer.

Starting a read or starting a write will give you an index to read from or write to. When a read or write is started the head or tail is updated so that the next process won't be given the same index.

Of course this causes an issue. What happens if a process starts a read operation and gets given index i . Then while it is still reading some operations occur causing the buffer to wrap around, since we have already incremented the head, position i can be written to while a process is still reading from it.

To solve this the monitor will keep track of whether a buffer index is being accessed and will have a condition variable for each of the buffer positions. So when starting a read or a write before we let the process access the buffer we check if there currently is a process accessing the given position, if there is then we wait for the condition variable assigned to that buffer position to be signaled. When finishing an operation we update a value to say that now that position doesn't have a process accessing it and we signal the condition variable for that buffer position.

```

1: buffer  $\leftarrow [K]$ 
2: procedure MONITOR RW
3:   head  $\leftarrow 0$ 
4:   tail  $\leftarrow 0$ 
5:   cond conds[K]
6:   cond notEmpty, notFull
7:   num[N]
8: procedure STARTR
9:   pos  $\leftarrow head$ 
10:  if length() == 0 then
11:    waitC(notEmpty)
12:  increment(head, K)
13:  signalC(notFull)
14:  if num[pos] == 1 then
15:    waitC(conds[pos])
16:  num[pos]  $\leftarrow 0$ 
17:  returnpos
18: procedure ENDR(int pos)
19:  num[pos]  $\leftarrow 0$ 
20:  signalC(conds[pos])
21: procedure STARTW
22:  pos  $\leftarrow tail$ 
23:  if length() == N then
24:    waitC(notFull)
25:  increment(tail, N)
26:  signalC(notEmpty)
27:  if num[pos] == 1 then
28:    waitC(conds[pos])
29:  num[pos]  $\leftarrow 1$ 
30:  returnpos
31: procedure ENDW(int pos)
32:  num[pos]  $\leftarrow 0$ 
33:  signalC(conds[pos])

```

Now we will make a more rigorous argument about why is solution satisfy the rule given. We see we can have multiple

We want to have multiple readers and writers accessing the buffer at the same time but ensure that no two processes can access the same position in

the buffer. If a process is reading or writing to position i then $num[i]$ will be equal to 1, indicating that that buffer position is currently being accessed. So if a new process attempts to start an operation that will involve index i it will be forced to wait until the $conds[i]$ condition is signaled. This condition is signaled when the process accessing position i ends its operation. For each of the condition variables in the $conds$ array we will use a wait queue so we can ensure actions will happen in the order which they started waiting, this is so if we get a read, then a write then a read to the same index we want the operations to execute in that order otherwise the two read threads could read the same value. This argument guarantees that no two processes will be accessing the same.

If the buffer is full and a process attempts a write then the process will be forced to wait until a read is started at which point the buffer will not be full. Similar for if a read is attempted while the buffer is empty, the process will be waited until a write has started. Note that while it might not make sense to signal the waiting process when the operation starts but remember that the process will be forced to wait until the current operation at that index is finished.

4 Double Buffering

For this we use a monitor with a signal and continue policy, to handout permissions for two buffers. The monitor keeps track of whether reads and writes have occurred as to know when a process is allowed to read or write data, it will also handle swapping the buffers.

```

1: readBuffer
2: writeBuffer
3: procedure MONITOR RW
4:   read  $\leftarrow$  true
5:   written  $\leftarrow$  false
6:   cond OKR, OKW
7: procedure STARTR
8:   if read == true then waitC(OKR)
9: procedure ENDR
10:  read  $\leftarrow$  true
11:  if written == true then
12:    swap()
13:    signalC(OKW)
14: procedure STARTW
15:  if written == true then
16:    waitC(OKW)
17: procedure ENDW
18:  written  $\leftarrow$  true
19:  if read == true then
20:    swap()
21:    signalC(OKR)
22: procedure SWAP
23:  readBuffer  $\leftarrow$  writeBuffer
24:  read  $\leftarrow$  false
25:  writen  $\leftarrow$  false

```

Now we show this solution satisfy the given correctness property's. The two variables *read* and *written* keep track of whether a read or write operation has occurred since the last swap. This is so if the consumer attempts to read but the data has already been read then we are forced to wait for a swap to occur (we don't want to read the same data twice), same for writes. Only when a read and a write have both occurred do we then swap the buffers around. So the read buffer can be read from and the write buffer can be written to at the same time.