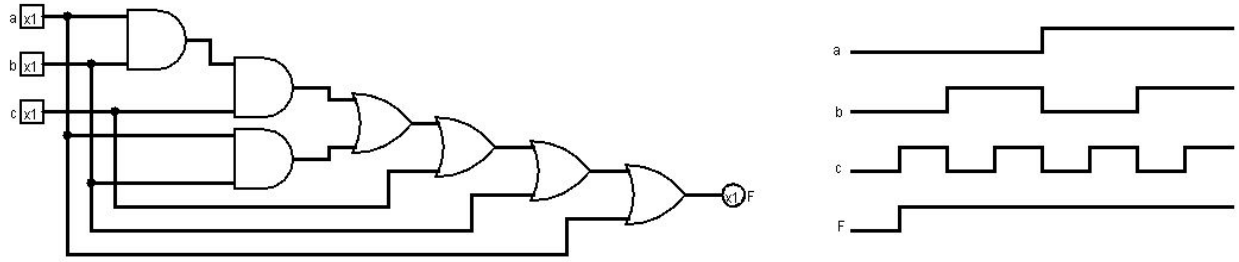
Cora English | 127007634

CSCE 312-201 Lab 2

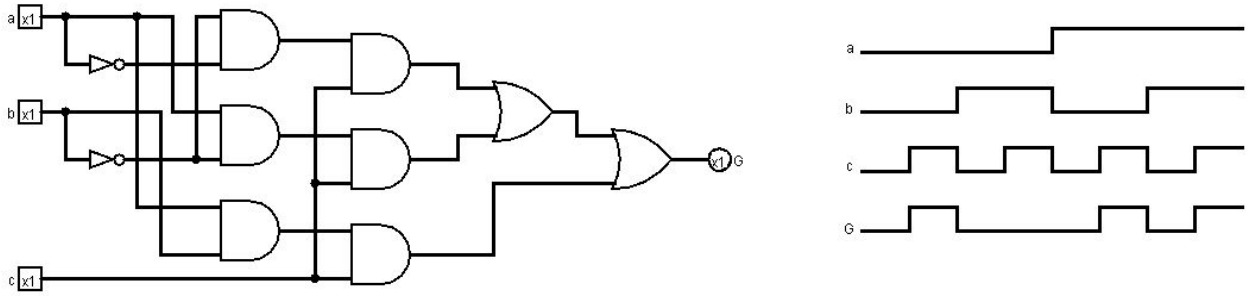
Problem 1:

1. Using one and two input gates draw and verify the digital circuit for the functions. Do not simplify/reduce the equations.

   a. F = abc + ab + a + b + c



   b. G = a'b'c + ab'c + abc



2. What are the names of the 74xx series logic gates that you should use to do the above problem in real-life situations?

- 74LS08 - 2 input AND gate
- 74LS32 - 2 input OR gate
- 74LS05 - inverter NOT gate

3. Calculate the delay performance (time delay between the change of any input which leads to a change of the output) of the two circuits designed above. Assume that you have used 74Fxx or 74LSxx series gates to implement the circuit. Use respective datasheets for the required chips.

- $F_{max\ delay}$ = 2 * AND (12ns) + 4 * OR (11ns) = 68 ns
- $G_{max\ delay}$ = 2 * NOT (17.5ns) + 2 * AND (12ns) + 2 * OR (11ns) = 81 ns

AND Data Sheet

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

OR Data Sheet

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

NOT Data Sheet

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

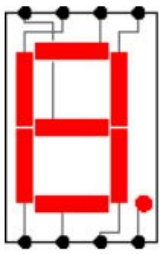
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

4. Which datasheet parameter(s) did you use to calculate the delay performance and why?

- The highlighted parameters were averaged and then used to calculate the delay. I used these because they were the higher end of the lower capacitance emittance. I averaged the LH and HL delays since this is a scenario that covers all general cases.

Problem 2:

1. Identify the following design parameters –
    a. Number of switches that will be required.
        - 7 switches are required.
    b. Number of the bits/wires required in the data bus.
        - 3 bits are required in the bus.
    c. Size of the encoder and decoder.
        - The encoder is 7x3 and decoder is 3x7.



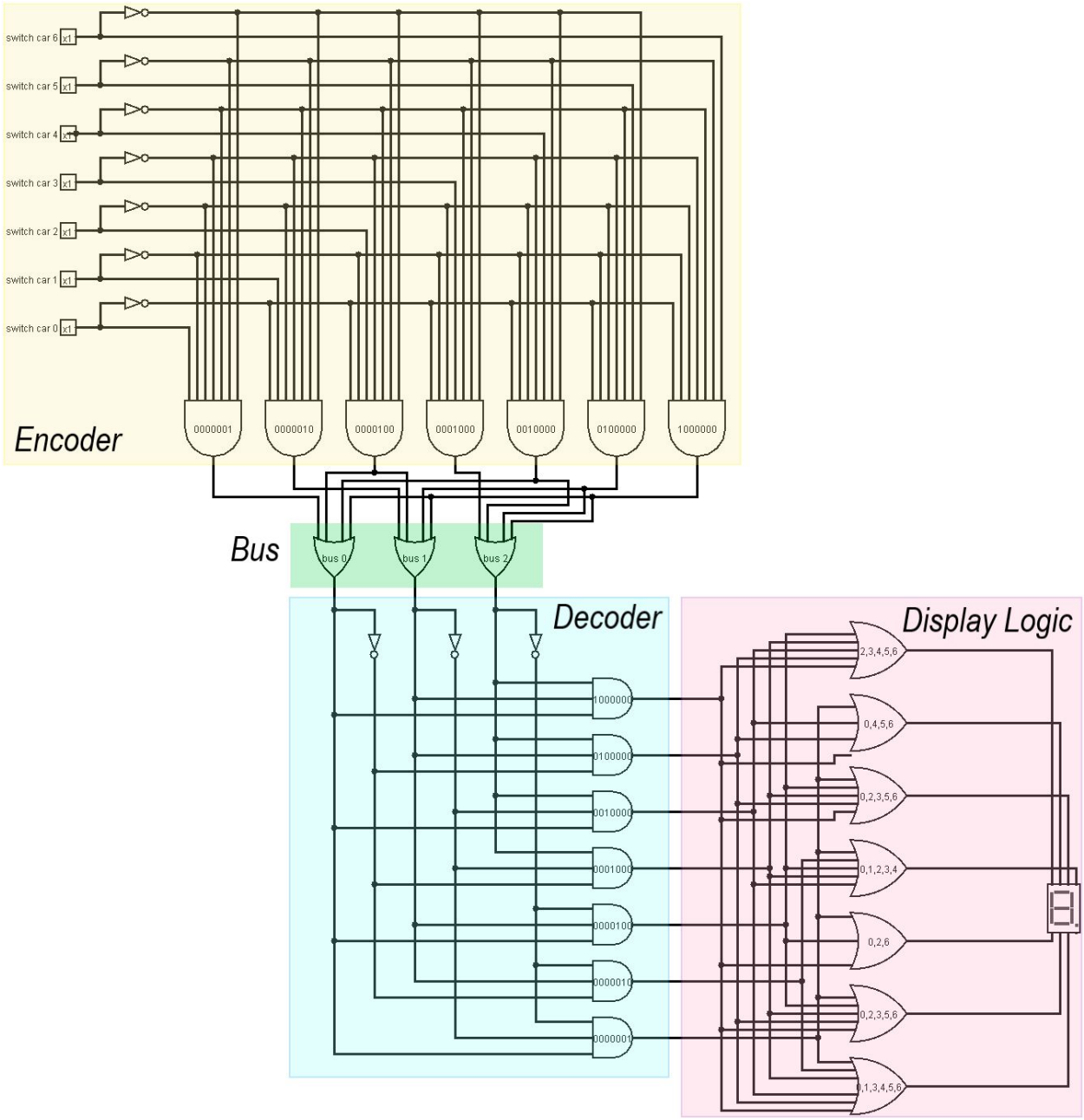
2. Read one of the 7 segment LED display datasheet, try to understand how to use it.
    - The 7 segment display has 8 input spots which each lights up a certain segment as shown above. I will have 7 OR gates attaching to each input with the corresponding outputs from the decoders feeding into the appropriate OR gate.

3. Design the encoder and decoder blocks with basic logic gates then incorporate the same into a complete digital system on Logisim. (Rough design of the basic logic implemented in logism)

Car:	Inputs:	Bus:	Decoder:
(0)	0000001	001	0000001
(1)	0000010	010	0000010
(2)	0000100	011	0000100
(3)	0001000	100	0001000
(4)	0010000	101	0010000
(5)	0100000	110	0100000
(6)	1000000	111	1000000

bus1 = 0000001+0000100+0010000+1000000
bus2 = 0000010+0000100+0100000+1000000
bus3 = 0001000+0010000+0100000+1000000

4. Submit your design with a brief text explanation/description of how it will actually work. You must explain the working of your system to get full credit.
    - The encoder takes 7 bits as inputs from the 6 cars and 1 motor car. If the input is 0000001 then the 0 (motor car) signal would light up. This pattern continues for the remaining 6 cars and can be seen above. The encoder outputs 3 bits which travel over the data bus and are then used as inputs in the decoder. This works in essentially the reverse way of the encoder in the fact that it has 3 bits of input and outputs 7 bits. These outputs determine what number should be shown on the 7 segment display. The display logic is highlighted in pink and uses or gates that correspond to the different segments on the display. The outputs from the decoder are fed into the or gates which use those outputs to display the corresponding car number.


switch car 6
x1
switch car 5
x1
switch car 4
x1
switch car 3
x1
switch car 2
x1
switch car 1
x1
switch car 0
x1
Encoder
0000001
0000010
0000100
0001000
0010000
0100000
1000000
Bus
bus 0
bus 1
bus 2
Decoder
1000000
0100000
0010000
0001000
0000100
0000010
0000001
Display Logic
2,3,4,5,6
0,4,5,6
0,2,3,5,6
0,1,2,3,4
0,2,6
0,2,3,5,6
0,1,3,4,5,6