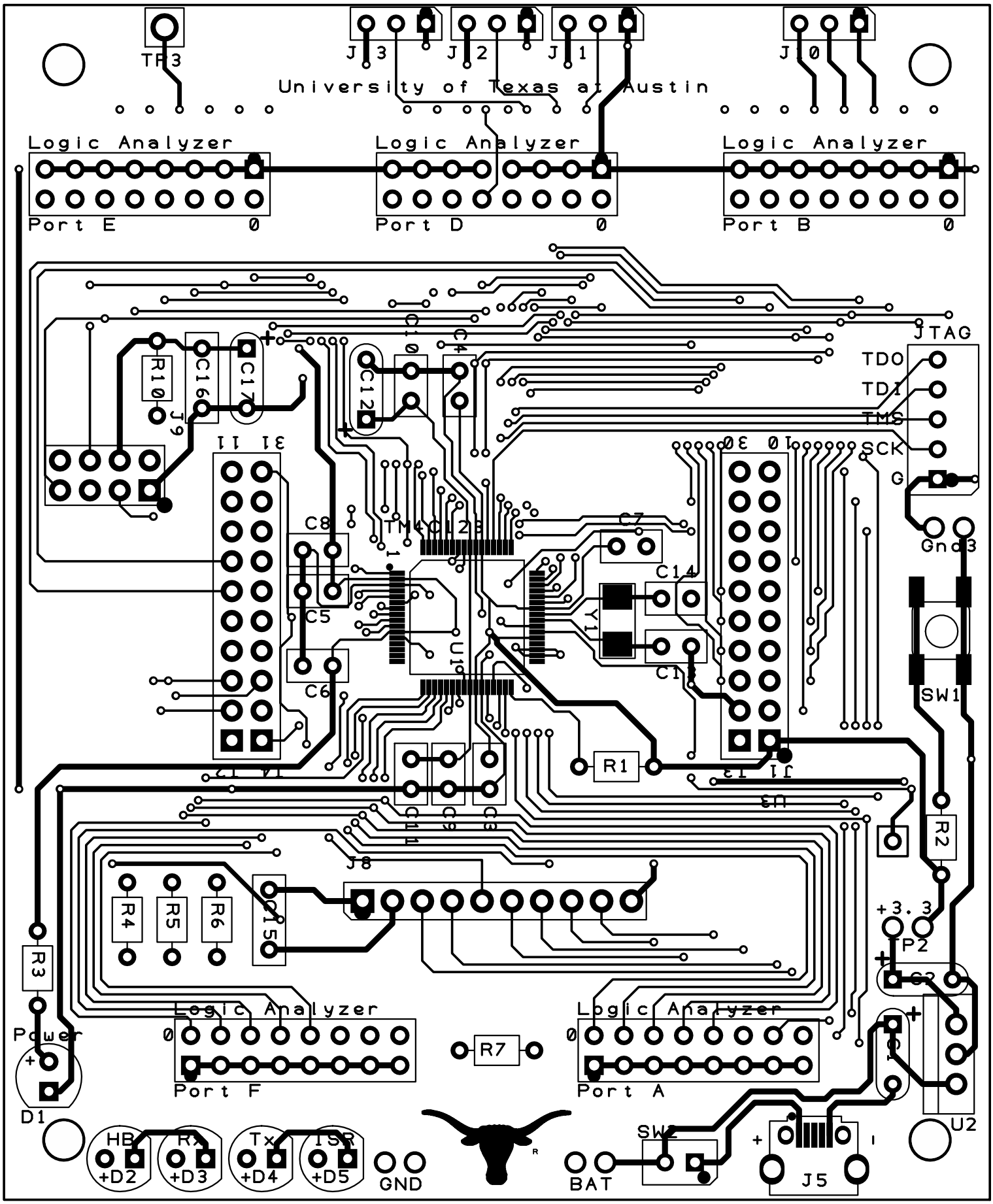
TP3
J3
J2
J1
J0
University of Texas at Austin
Logic Analyzer
Port E
Port D
Port B
JTAG
TDO
TDI
TMS
SCK
G
Gnd3
R10
C16
C17
J9
C10
C4
C12
C8
C5
C6
TM4C123
U10
C7
C14
Y1
C13
SW1
R1
J1
U3
R2
C11
C9
C3
J8
R4
R5
R6
C15
R3
+3.3
P2
C2
Power
D1
Port F
Port A
R7
U2
HB
RX
Tx
ISR
+D2
+D3
+D4
+D5
GND
BAT
SW2
J5