

## APPENDIX D INSTRUCTION SET LIST

### D.1 Conventions

#### (1) Register symbols used to describe operands

Register Symbol	Explanation
reg1	General-purpose registers: Used as source registers.
reg2	General-purpose registers: Used mainly as destination registers. Also used as source register in some instructions.
reg3	General-purpose registers: Used mainly to store the remainders of division results and the higher 32 bits of multiplication results.
bit#3	3-bit data for specifying the bit number
immX	X bit immediate data
dispX	X bit displacement data
regID	System register number
vector	5-bit data that specifies the trap vector (00H to 1FH)
cccc	4-bit data that shows the conditions code
sp	Stack pointer (r3)
ep	Element pointer (r30)
listX	X item register list

#### (2) Register symbols used to describe opcodes

Register Symbol	Explanation
R	1-bit data of a code that specifies reg1 or regID
r	1-bit data of the code that specifies reg2
w	1-bit data of the code that specifies reg3
d	1-bit displacement data
l	1-bit immediate data (indicates the higher bits of immediate data)
i	1-bit immediate data
cccc	4-bit data that shows the condition codes
CCCC	4-bit data that shows the condition codes of Bcond instruction
bbb	3-bit data for specifying the bit number
L	1-bit data that specifies a program register in the register list

**(3) Register symbols used in operations**

Register Symbol	Explanation
←	Input for
GR [ ]	General-purpose register
SR [ ]	System register
zero-extend (n)	Expand n with zeros until word length.
sign-extend (n)	Expand n with signs until word length.
load-memory (a, b)	Read size b data from address a.
store-memory (a, b, c)	Write data b into address a in size c.
load-memory-bit (a, b)	Read bit b of address a.
store-memory-bit (a, b, c)	Write c to bit b of address a.
saturated (n)	Execute saturated processing of n (n is a 2's complement). If, as a result of calculations, n ≥ 7FFFFFFFH, let it be 7FFFFFFFH. n ≤ 80000000H, let it be 80000000H.
result	Reflects the results in a flag.
Byte	Byte (8 bits)
Halfword	Half word (16 bits)
Word	Word (32 bits)
+	Addition
−	Subtraction
	Bit concatenation
×	Multiplication
÷	Division
%	Remainder from division results
AND	Logical product
OR	Logical sum
XOR	Exclusive OR
NOT	Logical negation
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

**(4) Register symbols used in execution clock**

Register Symbol	Explanation
i	If executing another instruction immediately after executing the first instruction (issue).
r	If repeating execution of the same instruction immediately after executing the first instruction (repeat).
l	If using the results of instruction execution in the instruction immediately after the execution (latency).

**(5) Register symbols used in flag operations**

Identifier	Explanation
(Blank)	No change
0	Clear to 0
X	Set or cleared in accordance with the results.
R	Previously saved values are restored.

**(6) Condition codes**

Condition Code (cccc)	Condition Formula	Explanation
0 0 0 0	$OV = 1$	Overflow
1 0 0 0	$OV = 0$	No overflow
0 0 0 1	$CY = 1$	Carry Lower (Less than)
1 0 0 1	$CY = 0$	No carry Not lower (Greater than or equal)
0 0 1 0	$Z = 1$	Zero
1 0 1 0	$Z = 0$	Not zero
0 0 1 1	$(CY \text{ or } Z) = 1$	Not higher (Less than or equal)
1 0 1 1	$(CY \text{ or } Z) = 0$	Higher (Greater than)
0 1 0 0	$S = 1$	Negative
1 1 0 0	$S = 0$	Positive
0 1 0 1	–	Always (Unconditional)
1 1 0 1	$SAT = 1$	Saturated
0 1 1 0	$(S \text{ xor } OV) = 1$	Less than signed
1 1 1 0	$(S \text{ xor } OV) = 0$	Greater than or equal signed
0 1 1 1	$((S \text{ xor } OV) \text{ or } Z) = 1$	Less than or equal signed
1 1 1 1	$((S \text{ xor } OV) \text{ or } Z) = 0$	Greater than signed

## D.2 Instruction Set (in Alphabetical Order)

(1/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
ADD	reg1,reg2	rrrrr001110RRRRR	GR[reg2]←GR[reg2]+GR[reg1]	1	1	1	x	x	x	x	
	imm5,reg2	rrrrr010010iiii	GR[reg2]←GR[reg2]+sign-extend(imm5)	1	1	1	x	x	x	x	
ADDI	imm16,reg1,reg2	rrrrr110000RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)	1	1	1	x	x	x	x	
AND	reg1,reg2	rrrrr001010RRRRR	GR[reg2]←GR[reg2]AND GR[reg1]	1	1	1		0	x	x	
ANDI	imm16,reg1,reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]AND zero-extend(imm16)	1	1	1		0	x	x	
Bcond	disp9	ddddd1011dddcccc <b>Note 1</b>	if conditions are satisfied then PC←PC+sign-extend(disp9)	2	2	2					
			When conditions are satisfied	<b>Note 2</b>	<b>Note 2</b>	<b>Note 2</b>					
			When conditions are not satisfied	1	1	1					
BSH	reg2,reg3	rrrrr11111100000 wwwwww01101000010	GR[reg3]←GR[reg2] (23 : 16)    GR[reg2] (31 : 24)    GR[reg2] (7 : 0)    GR[reg2] (15 : 8)	1	1	1	x	0	x	x	
BSW	reg2,reg3	rrrrr11111100000 wwwwww01101000000	GR[reg3]←GR[reg2] (7 : 0)    GR[reg2] (15 : 8)    GR [reg2] (23 : 16)    GR[reg2] (31 : 24)	1	1	1	x	0	x	x	
CALLT	imm6	0000001000iiii	CTPC←PC+2(return PC) CTPSW←PSW adr←CTBP+zero-extend(imm6 logically shift left by 1) PC←CTBP+zero-extend(Load-memory(adr,Halfword))	4	4	4					
CLR1	bit#3,disp16[reg1]	10bbb111110RRRRR dddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,0)	3	3	3				x	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100100	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,0)	3	3	3				x	
CMOV	cccc,imm5,reg2,reg3	rrrrr111111iiii wwwwww01100cccc0	if conditions are satisfied then GR[reg3]←sign-extended(imm5) else GR[reg3]←GR[reg2]	1	1	1					
	cccc,reg1,reg2,reg3	rrrrr111111RRRRR wwwwww011001cccc0	if conditions are satisfied then GR[reg3]←GR[reg1] else GR[reg3]←GR[reg2]	1	1	1					
CMP	reg1,reg2	rrrrr001111RRRRR	result←GR[reg2]−GR[reg1]	1	1	1	x	x	x	x	
	imm5,reg2	rrrrr010011iiii	result←GR[reg2]−sign-extend(imm5)	1	1	1	x	x	x	x	
CTRET		000001111100000 0000000101000100	PC←CTPC PSW←CTPSW	3	3	3	R	R	R	R	R
DBRET		000001111100000 0000000101000110	PC←DBPC PSW←DBPSW	3	3	3	R	R	R	R	R

# APPENDIX D INSTRUCTION SET LIST

(2/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
DBTRAP		1111100001000000	DBPC←PC+2 (restored PC) DBPSW←PSW PSW.NP←1 PSW.EP←1 PSW.ID←1 PC←00000060H	3	3	3					
DI		0000011111100000 0000000101100000	PSW.ID←1	1	1	1					
DISPOSE	imm5,list12	0000011001iiiiL LLLLLLLLLLL00000	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	imm5,list12,[reg1]	0000011001iiiiL LLLLLLLLLLLRRRRR Note 5	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded PC←GR[reg1]	n+3 Note 4	n+3 Note 4	n+3 Note 4					
DIV	reg1,reg2,reg3	rrrrr11111RRRRR wwwwww01011000000	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		x	x	x	
DIVH	reg1,reg2	rrrrr000010RRRRR	GR[reg2]←GR[reg2]÷GR[reg1] <sup>Note 6</sup>	35	35	35		x	x	x	
	reg1,reg2,reg3	rrrrr11111RRRRR wwwwww01010000000	GR[reg2]←GR[reg2]÷GR[reg1] <sup>Note 6</sup> GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		x	x	x	
DIVHU	reg1,reg2,reg3	rrrrr11111RRRRR wwwwww01010000010	GR[reg2]←GR[reg2]÷GR[reg1] <sup>Note 6</sup> GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		x	x	x	
DIVU	reg1,reg2,reg3	rrrrr11111RRRRR wwwwww01011000010	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		x	x	x	
EI		1000011111100000 0000000101100000	PSW.ID←0	1	1	1					
HALT		0000011111100000 0000000100100000	Stop	1	1	1					
HSW	reg2,reg3	rrrrr11111100000 wwwwww01101000100	GR[reg3]←GR[reg2](15 : 0)    GR[reg2] (31 : 16)	1	1	1	x	0	x	x	
JARL	disp22,reg2	rrrrr11110ddddd dddddddddddddd0 Note 7	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)	2	2	2					
JMP	[reg1]	00000000011RRRRR	PC←GR[reg1]	3	3	3					
JR	disp22	0000011110ddddd dddddddddddddd0 Note 7	PC←PC+sign-extend(disp22)	2	2	2					
LD.B	disp16[reg1],reg2	rrrrr111000RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 11					
LD.BU	disp16[reg1],reg2	rrrrr11110bRRRRR dddddddddddddd1 Notes 8, 10	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 11					

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
LD.H	disp16[reg1],reg2	rrrrr111001RRRRR dddddddddddddd0 <b>Note 8</b>	adr←GR[reg1]+sign-extend(displ6) GR[reg2]←sign-extend(Load-memory(adrl,Halfword))	1	1	<b>Note 11</b>					
LDSR	reg2,regID	rrrrr11111RRRRR 0000000000100000 <b>Note 12</b>	SR[regID]←GR[reg2]	1	1	1					
			Other than regID = PSW regID = PSW	1	1	1	×	×	×	×	×
LD.HU	disp16[reg1],reg2	rrrrr11111RRRRR dddddddddddddd1 <b>Note 8</b>	adr←GR[reg1]+sign-extend(displ6) GR[reg2]←zero-extend(Load-memory(adrl,Halfword))	1	1	<b>Note 11</b>					
LD.W	disp16[reg1],reg2	rrrrr111001RRRRR dddddddddddddd1 <b>Note 8</b>	adr←GR[reg1]+sign-extend(displ6) GR[reg2]←Load-memory(adrl,Word)	1	1	<b>Note 11</b>					
MOV	reg1,reg2	rrrrr00000RRRRR	GR[reg2]←GR[reg1]	1	1	1					
	imm5,reg2	rrrrr010000iiii	GR[reg2]←sign-extend(imm5)	1	1	1					
	imm32,reg1	00000110001RRRRR iiiiiiiiiiiiiiii iiiiiiiiiiiiiiii	GR[reg1]←imm32	2	2	2					
MOVEA	imm16,reg1,reg2	rrrrr110001RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)	1	1	1					
MOVHI	imm16,reg1,reg2	rrrrr110010RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+(imm16 ll 0 <sup>16</sup> )	1	1	1					
MUL	reg1,reg2,reg3	rrrrr11111RRRRR wwwww01000100000 <b>Note 14</b>	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]	1	4	5					
	imm9,reg2,reg3	rrrrr111111iiii wwwww01001111100 <b>Note 13</b>	GR[reg3] ll GR[reg2]←GR[reg2]xsign-extend(imm9)	1	4	5					
MULH	reg1,reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2] <sup>Note 6</sup> xGR[reg1] <sup>Note 6</sup>	1	1	2					
	imm5,reg2	rrrrr010111iiii	GR[reg2]←GR[reg2] <sup>Note 6</sup> xsign-extend(imm5)	1	1	2					
MULHI	imm16,reg1,reg2	rrrrr110111RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1] <sup>Note 6</sup> ximm16	1	1	2					
MULU	reg1,reg2,reg3	rrrrr11111RRRRR wwwww01000100010 <b>Note 14</b>	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]	1	4	5					
	imm9,reg2,reg3	rrrrr111111iiii wwwww0100111110 <b>Note 13</b>	GR[reg3] ll GR[reg2]←GR[reg2]xzero-extend(imm9)	1	4	5					
NOP		0000000000000000	Pass at least one clock cycle doing nothing.	1	1	1					
NOT	reg1,reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])	1	1	1		0	×	×	
NOT1	bit#3,disp16[reg1]	01bbb111110RRRRR dddddddddddddd	adr←GR[reg1]+sign-extend(displ6) Z flag←Not(Load-memory-bit(adrl,bit#3)) Store-memory-bit(adrl,bit#3,Z flag)	3 <b>Note 3</b>	3 <b>Note 3</b>	3 <b>Note 3</b>				×	
	reg2,[reg1]	rrrrr11111RRRRR 0000000011100010	adr←GR[reg1] Z flag←Not(Load-memory-bit(adrl,reg2)) Store-memory-bit(adrl,reg2,Z flag)	3 <b>Note 3</b>	3 <b>Note 3</b>	3 <b>Note 3</b>				×	

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
OR	reg1,reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2]OR GR[reg1]	1	1	1		0	×	×	
ORI	imm16,reg1,reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]OR zero-extend(imm16)	1	1	1		0	×	×	
PREPARE	list12,imm5	0000011110iiiiL LLLLLLLLLLLL00001	Store-memory(sp−4,GR[reg in list12],Word) sp←sp−4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5)	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	list12,imm5, sp/imm <sup>Note 15</sup>	0000011110iiiiL LLLLLLLLLLLLff011 imm16/imm32 <b>Note 16</b>	Store-memory(sp−4,GR[reg in list12],Word) sp←sp+4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend (imm5) ep←sp/imm	n+2 Note 4 Note 17	n+2 Note 4 Note 17	n+2 Note 4 Note 17					
RETI		000001111100000 000000010100000	if PSW.EP=1 then PC ←EIPC PSW ←EIPSW else if PSW.NP=1 then PC ←FEPC PSW ←FEPSW else PC ←EIPC PSW ←EIPSW	3	3	3	R	R	R	R	R
SAR	reg1,reg2	rrrrr11111RRRRR 000000001010000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010101iiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend (imm5)	1	1	1	×	0	×	×	
SASF	cccc,reg2	rrrrr111110cccc 000000100000000	if conditions are satisfied then GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000001H else GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000000H	1	1	1					
SATADD	reg1,reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	1	1	1	×	×	×	×	×
	imm5,reg2	rrrrr010001iiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5))	1	1	1	×	×	×	×	×
SATSUB	reg1,reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]−GR[reg1])	1	1	1	×	×	×	×	×
SATSUBI	imm16,reg1,reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]−sign-extend(imm16))	1	1	1	×	×	×	×	×
SATSUBR	reg1,reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]−GR[reg2])	1	1	1	×	×	×	×	×
SETF	cccc,reg2	rrrrr111110cccc 000000000000000	If conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H	1	1	1					

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SET1	bit#3,disp16[reg1]	00bbb11110RRRRR dddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr11111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr11111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr11111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110dddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd Note 18	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000dddddd Note 19	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd Notes 18, 20	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010dddddd0 Note 21	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111dddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001dddddd Note 19	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010dddddd1 Note 21	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR dddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR dddddddddddddd0 Note 8	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Halfword)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR dddddddddddddd1 Note 8	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Word)	1	1	1					
STSR	regID,reg2	rrrrr11111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					



Mnemonic	Operand	Opcode	Operation	Execution Clock		Flags					
				i	r	l	CY	OV	S	Z	SAT
SUB	reg1,reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]−GR[reg1]	1	1	1	x	x	x	x	
SUBR	reg1,reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]−GR[reg2]	1	1	1	x	x	x	x	
SWITCH	reg1	0000000010RRRRR	adr←(PC+2) + (GR [reg1] logically shift left by 1) PC←(PC+2) + (sign-extend (Load-memory (adr,Halfword)) logically shift left by 1	5	5	5					
SXB	reg1	00000000101RRRRR	GR[reg1]←sign-extend (GR[reg1] (7 : 0))	1	1	1					
SXH	reg1	00000000111RRRRR	GR[reg1]←sign-extend (GR[reg1] (15 : 0))	1	1	1					
TRAP	vector	0 0 0 0 0 1 1 1 1 1 1 i i i i i 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	EIPC ←PC+4 (Restored PC) EIPSW ←PSW ECR.EICC ←Interrupt code PSW.EP ←1 PSW.ID ←1 PC ←00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1,reg2	rrrrr001011RRRRR	result←GR[reg2] AND GR[reg1]	1	1	1		0	x	x	
TST1	bit#3,disp16[reg1]	11bbb111110RRRRR ddddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit (adr,bit#3))	3	3	3	Note 3	Note 3	Note 3		x
	reg2, [reg1]	rrrrr111111RRRRR 0000000011100110	adr←GR[reg1] Z flag←Not (Load-memory-bit (adr,reg2))	3	3	3	Note 3	Note 3	Note 3		x
XOR	reg1,reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1		0	x	x	
XORI	imm16,reg1,reg2	rrrrr110101RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1] XOR zero-extend (imm16)	1	1	1		0	x	x	
ZXB	reg1	00000000100RRRRR	GR[reg1]←zero-extend (GR[reg1] (7 : 0))	1	1	1					
ZXH	reg1	00000000110RRRRR	GR[reg1]←zero-extend (GR[reg1] (15 : 0))	1	1	1					

- Notes**
1. dddddddd: Higher 8 bits of disp9.
  2. 3 if there is an instruction that rewrites the contents of the PSW immediately before.
  3. If there is no wait state (3 + the number of read access wait states).
  4. n is the total number of list12 load registers. (According to the number of wait states. Also, if there are no wait states, n is the total number of list12 registers. If n = 0, same operation as when n = 1)
  5. RRRRR: other than 00000.
  6. The lower halfword data only are valid.
  7. dddddddddddddddddddd: The higher 21 bits of disp22.
  8. dddddddddddddddd: The higher 15 bits of disp16.
  9. According to the number of wait states (1 if there are no wait states).
  10. b: bit 0 of disp16.
  11. According to the number of wait states (2 if there are no wait states).

**Notes 12.** In this instruction, for convenience of mnemonic description, the source register is made reg2, but the reg1 field is used in the opcode. Therefore, the meaning of register specification in the mnemonic description and in the opcode differs from other instructions.

rrrrr = regID specification

RRRRR = reg2 specification

**13.** iiii: Lower 5 bits of imm9.

IIII: Higher 4 bits of imm9.

**14.** Do not specify the same register for general-purpose registers reg1 and reg3.

**15.** sp/imm: specified by bits 19 and 20 of the sub-opcode.

**16.** ff = 00: Load sp in ep.

01: Load sign expanded 16-bit immediate data (bits 47 to 32) in ep.

10: Load 16-bit logically left shifted 16-bit immediate data (bits 47 to 32) in ep.

11: Load 32-bit immediate data (bits 63 to 32) in ep.

**17.** If imm = imm32, n + 3 clocks.

**18.** rrrrr: Other than 00000.

**19.** ddddddd: Higher 7 bits of disp8.

**20.** dddd: Higher 4 bits of disp5.

**21.** ddddddd: Higher 6 bits of disp8.