ECE 385

Fall 2023

Experiment #1

Introductory Experiment

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GL/1:45-2:00
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Introduction

This lab is an introductory experiment of ECE385, the goal of this lab is to introduce the how the lab works and the equipment in the class. From this lab, we get to familiarize ourselves with the function generator and the oscilloscope, which we would need in later labs. In this lab, rather than demo the circuit ourselves the lab report will be based on Professor Chen's circuit construction and testing data.

Purpose of Circuit

This lab is mainly about static hazard. The goal of the circuit is to design a 2 to 1 multiplexor using only quad 2-input NAND gate chips (7400) From the given circuit in the lab description, we will encounter the static-1 hazard glitch and other noises, so we must redesign the circuit to eliminate propagation delay.

Written Description of Circuit

In the circuit, we have 4 signals: A, B, C, and Z. A and C are the two inputs of the mux, Z is the output, and B is the select signal to decide between A or C. When B = 0, the mux will output the signal of C, and when B = 1, the mux will output the signal of A. From this intended behavior, we can draw the truth table.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table for 2 to 1 Mux

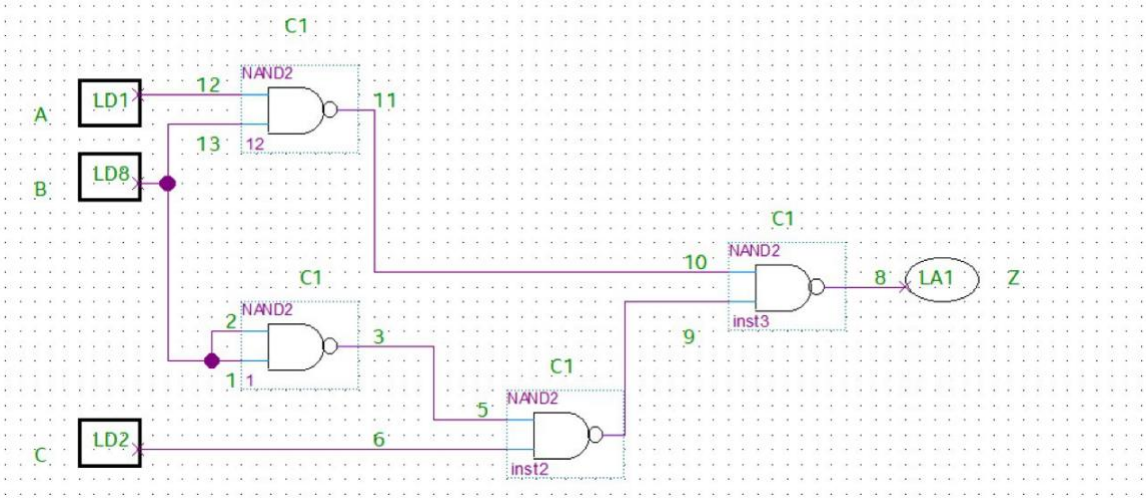
We can draw out the kmap from the truth table.

		A,C			
	Z	0,0	0,1	1,1	1,0
B	0	0	1	1	0
	1	0	0	1	1

Expression = B'C + AC + AB

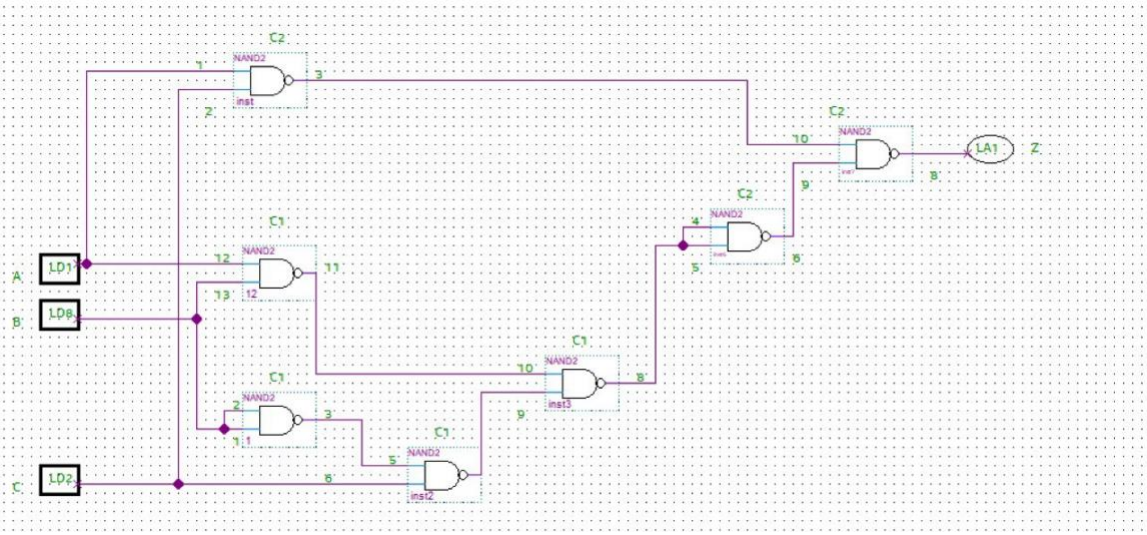
The given circuit diagram has an expression of B'C + AB, but to eliminate the static hazard, we include the extra term AC, making it B'C + AC + AB. Now the inputs A, B, and C will be travelling through the same number of gates.

This is the original circuit:



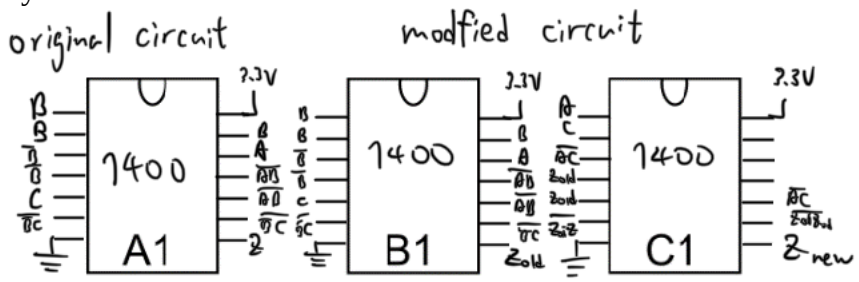
(Logic Diagram graphed on Quartus)

This is the new modified circuit:

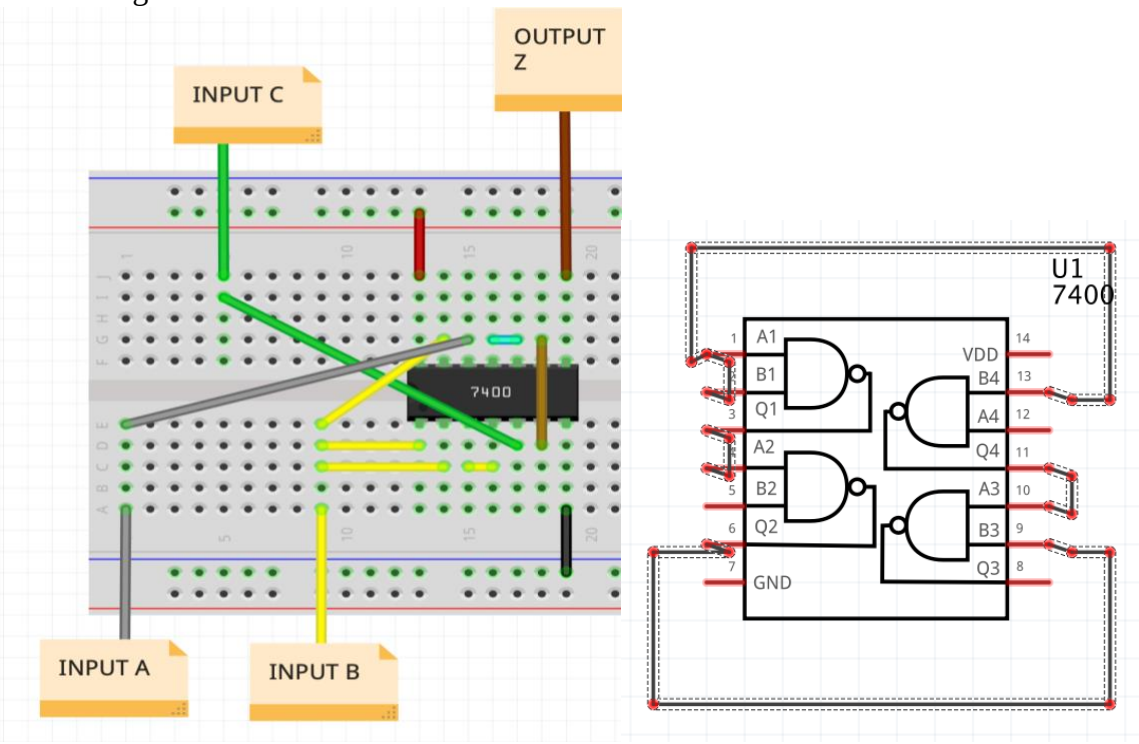


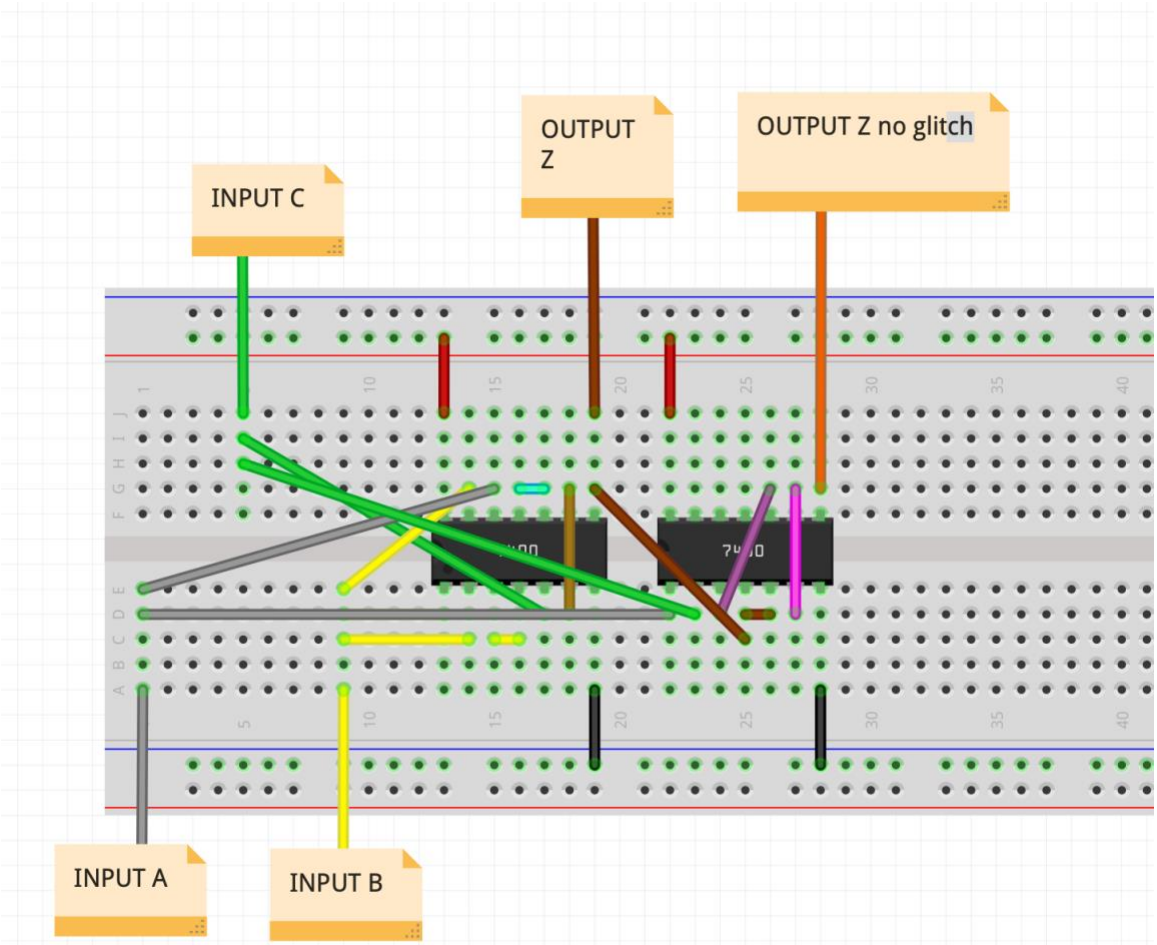
(Logic Diagram graphed on Quartus)

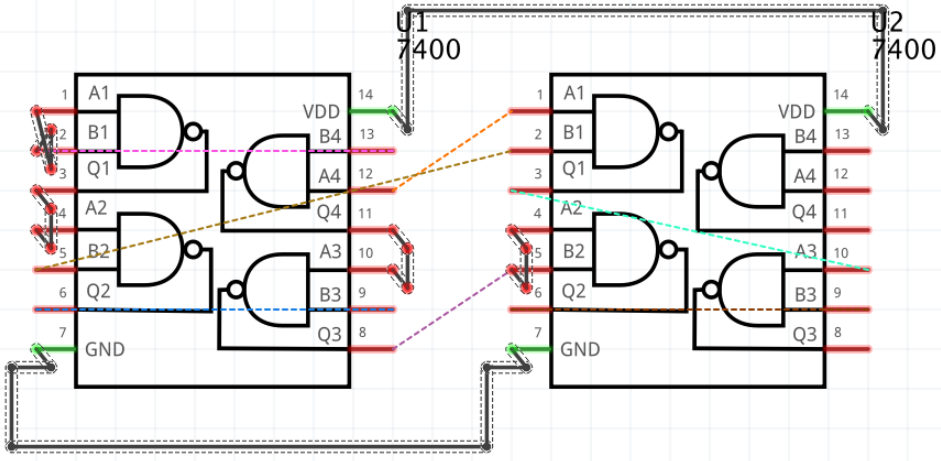
Pin Layout:



The fritzing:




INPUT C
OUTPUT Z
OUTPUT Z no glitch
INPUT A
INPUT B


U1
7400
U2
7400
A1
B1
Q1
A2
B2
Q2
GND
VDD
B4
A4
Q4
A3
B3
Q3

Answers to Pre-Lab Questions

Not all groups may observe static hazards (why?) :

The reason why not every group may observe static hazards is that every gate has a different gate delay. For the original Z = BA + B'C, the signal A and C has to go through 2 NAND gates to get to the output Z; however, the signal B, when doing the term B'C, has to go through three NAND gates to get to output Z. Since the output B has to go through more gates, there might be a moment when A and C remains 1, and B changes from 1 to 0, the output Z will become 0 for a short amount of time, since the NAND gate for A and B output 1, the NAND gate for C and the last B outputs also outputs 1, which makes Z into 0 before the new B signal catch up.

However, this will not happen every time, since sometimes the last output of B will generate the desired signal anyways, so people can't tell the difference. For example, when A and C remains 1, and B changes from 0 to 1, we won't see the static hazard since the static hazard's output is the correct output we want. On B's rising edge, the output both before and after the delay is what we wanted. This is why not all groups may observe static hazards.

Also another reason why some groups might observe static hazard is that the gates are guaranteed to have a gate delay between a range, so in some case the (AB)' might take a longer time to output the signal and it might be the same time as the other longer pat. If this happens, there won't be static hazard as well.

If you do not observe a static hazard, chain an odd number of inverters together in place of the single inverter from Figure 17 or add a small capacitor to the output of the inverter until you observe a glitch. Why does the hazard appear when you do this?

The capacitor will increase the inverter's delay because in order for the signal to go to the next gate, the circuit have to first charge the capacitor, which will take more time than directly going through a wire. The increase of time will help us see the static hazard more clearly. Also, the small capacitor in this case acts as a decoupling capacitor, which will absorb the noise. In this lab, we are using the CMOS chips, and when CMOS is switching, there will momentarily

have a short circuit between Vdd and ground. This is going to create a lot of noise between the logic gates. However, when we have the decoupling capacitor, it can absorb the sudden voltage change.

We can also add an odd number of inverters, so now the signal must go through more gates to get to the output. This will make static hazard even more obvious. The reason why we need an odd number of inverters in place of the single inverter is just that we don't want to change the result we have, so we have to add odd number of inverters.

Answers to Lab Questions

1. **Unit test each integrated circuit (chip) required for this lab.**

   This should be tested in the lab portion, which Professor covered.

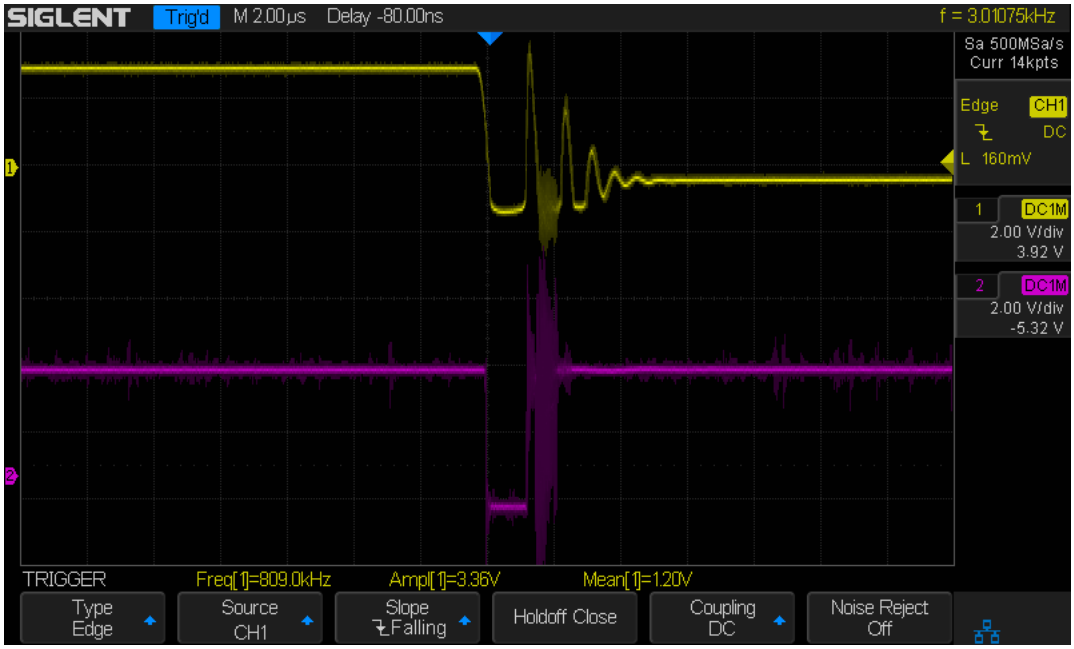
2. **Complete a truth table of the output as a function of the three inputs.**

   Same as the table above.

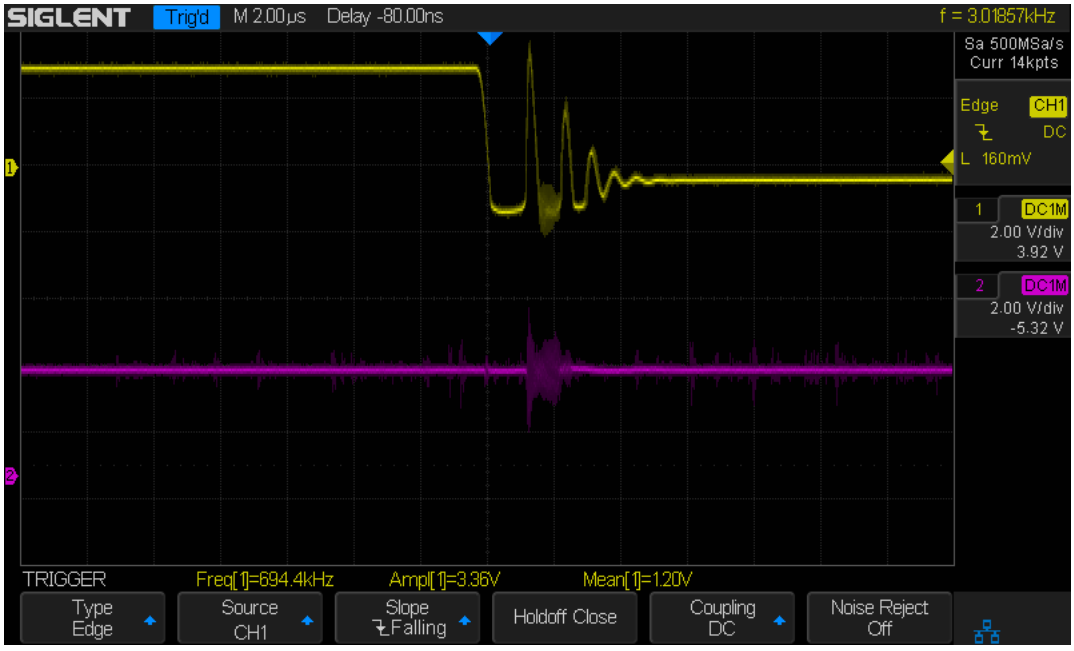
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table for 2 to 1 Mux

Oscilloscope output from Part A



Oscilloscope output from Part B



Using the three input switches, test the circuit in part B of the pre-lab. Complete a truth table of the output. Does it respond like the circuit of part A?

For part B's circuit, we get the same truth table as we get in part A. Since the static hazard won't really be reflected on the truth table. However, part A's circuit will still experience static hazard whereas part B's circuit will not.

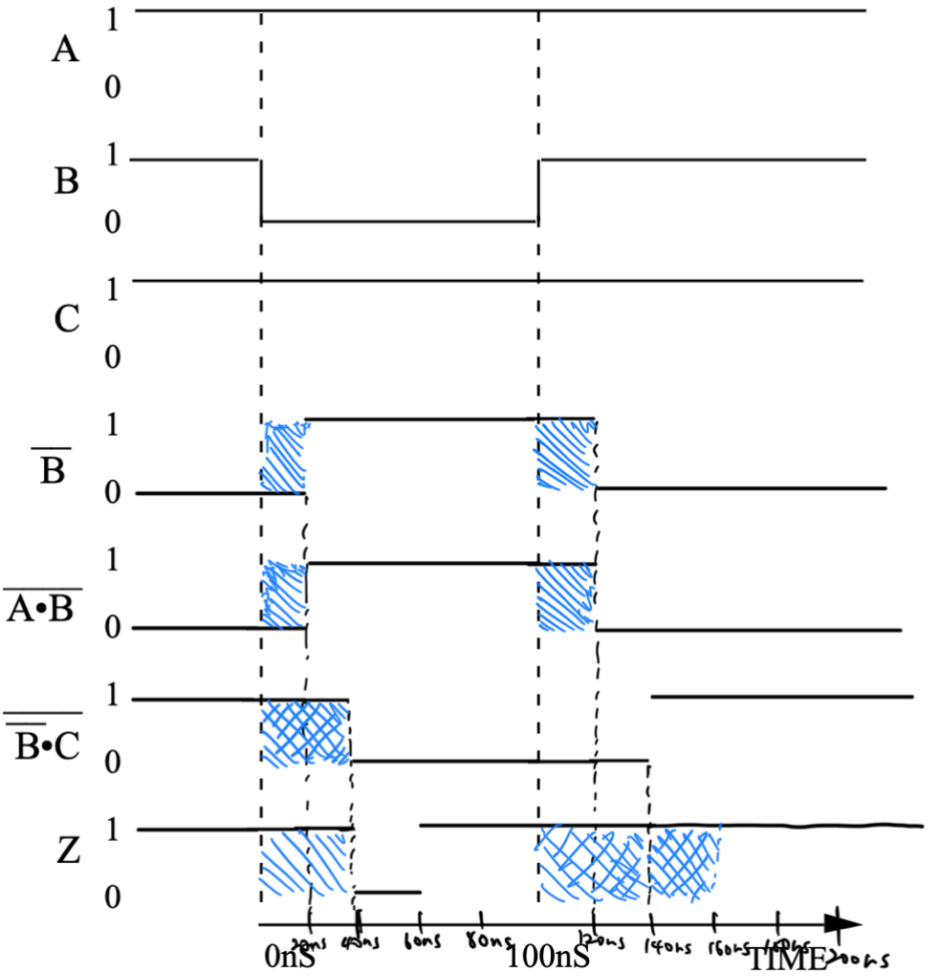
With inputs A and C high, observe input B and the circuit output on the oscilloscope. Describe and save the output and explain any differences between it and the results obtained in part 2. Consider the following question and explain: for the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?

When the input B is connected to the pulse generator, for the circuit in part A, we will see the static hazard every time the B signals drop to 0. The output voltage will stay 0 for a few nanoseconds and then go back to normal. However, for the rising voltage, we won't really see any hazards. At the falling edge of input B, we are more likely to see a glitch.

Answers to Post-Lab Questions

Given that the guaranteed minimum propagation delay of a 7400 is 0ns and that its guaranteed maximum delay time is 20ns, complete the timing diagram below for the circuit of part A. (See GG.17 if you are not sure how to proceed.)

TIMING DIAGRAM



How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

They will both take 60ns to stabilize since the signal has to go through 3 gates and each has a maximum of 20ns delay. However, the glitches will only occur on the falling edge, we will see the signal Z goes to 0 for 20ns and goes back to 1 after that. The reason why the glitches occur is that the Z NAND gate takes in two input from (AB)' and (B'C)', and the (AB)' changes first while the (B'C)' has not changed yet, so the output signal Z, at the falling edge will become 0 for a short amount of time during falling edge. But during rising edge the glitched input will be the same as the correct input so we can't tell the difference.

Explain how and why the debouncer circuit given in General Guide (Figure 22) works. Specifically, what makes it behave like a switch and how the ill effect of mechanical contact bounces is eliminated?

The ill effect of mechanical contact bounces happens because when the switch is pressed, the contact force is too strong that the switches will momentarily separate from each other before it goes to rest. First, the switch right now will no longer be bouncing between on and off because it is no longer a single wire closing and opening. Now the signal will only bounce between A and C or in the other case B and C. The debouncing circuit creates a smooth transition between high and low by also using a pull up resistor and ground to make sure the signal is 1 and 0.

Answers to General Guide Questions

What is the advantage of a larger noise immunity?

Noise immunity is describing the logic gate's threshold of what voltage is 1 and what voltage is 0. The reason why we need to have the noise immunity is because we don't want the noises to change a logic gates' output. Consequently, having a larger noise immunity allows the logic gate to filter out unrelated noises and only read the input as 1 when the actual input is 1.

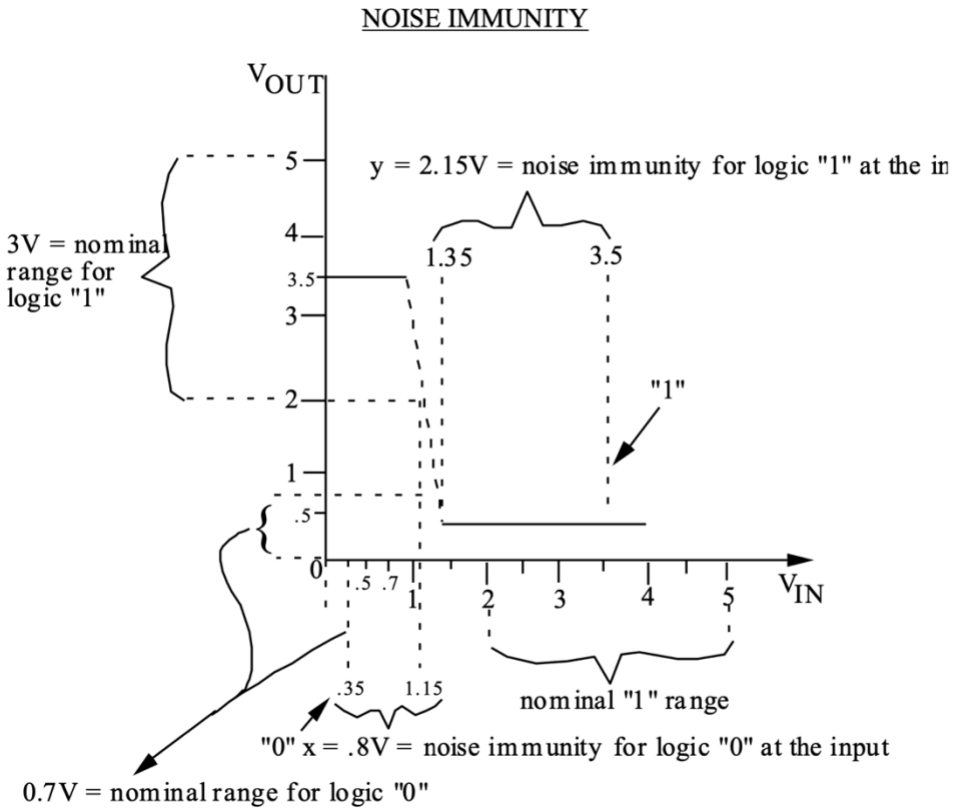
Why is the last inverter observed rather than simply the first?

This is because there will be noise generated throughout all the inverters, and by observing the last one, we can see a more significant result (the noises from all the inverters added up). The last inverter will carry a lot of noises if the noise immunity is low.

Given a graph of output voltage (VOUT) vs. inputvoltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter?

When given a graph of output voltage and input voltage, we first need to find the max voltage and the min voltage that be take in as low, and subtract the max by the min voltage, we'll get the noise immunity for logic 0 at the input. In the graph below, 1.15-0.35=0.8. After that, we do the same thing for the max and min voltage that will be take in as high. 3.5-1.35=2.15, 2.15 is the noise

immunity for logic 1.



Irrespective of which polarity you choose for your LEDs, it is important that each LED has its own resistor. If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?

Having the same resistor for all the LEDs is bad because that'll mean we must connect all the LEDs in parallel, which will make the voltage across all the LEDs the same. This might burn some of the LEDs since not all LEDs have the same turn on voltage. If one of the LEDs has a high turn on voltage while the other has a low turn on voltage, all the current will go through the low-turn-on LED and burn it.

Conclusions

In this lab, we can observe the glitch of static hazard. We used several ways like adding extra capacitor or inverters to make the pattern show up on the diagram. We found out that in this Lab1 circuit, static hazard will happen on the falling edge, but we can eliminate the glitch by adding the redundant term. Also, we learned to read the oscilloscope and draw the timing diagram. We were also introduced to the concept of noise immunity and some tips while wiring the LEDs.