Corey Waxman

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Summary

Computer engineer with a background in digital hardware, FPGAs, electronic design automation (EDA), and computer architecture.

Education

Tokyo Institute of Technology Tokyo, Japan 2019 - *(present)*
Doctoral Student, *Information and Communications Engineering*

University of Pennsylvania Philadelphia, PA, USA 2009 - 2011
MS, *Electrical Engineering*

Binghamton University Binghamton, NY, USA 2002 - 2007
BS, *Computer Engineering*

Technical Skills

Computer Languages: C/C++, Scala, Java, Verilog, VHDL, Python, Tcl, Bash scripting, LaTeX
Tools: Eclipse, Xilinx ISE/PlanAhead/Vivado, Altera Quartus II, Synopsys Synplify, ModelSim, Git, GDB
Operating Systems: Linux, Windows

Employment Experience

Fixstars Corporation Tokyo, Japan October 2019 - March 2020
Software Engineer (Internship)

- Surveyed existing FPGA backends for an image-processing domain-specific language (Halide).
- Explored alternative datatype representations for deep learning, working with various machine learning frontends (PyTorch, TensorFlow) and interfacing them with backend runtimes via ONNX.

Synopsys Israel Herzliya, Israel February 2017 - September 2018
R&D Engineer

- Worked on internal netlist representation and graph traversal algorithms powering static analysis tools.
- Developed EDA tools in the back-end compiler flow of a popular ASIC emulation platform.
- Took part in large C++ code bases using requisite design practices (code reviews, regression testing, etc.).

Israel Defense Forces Israel June 2013 - June 2016
Electronics Engineer

- Served as an Academic Officer in the IDF at a technological unit in the field of digital hardware design.
- Engaged in design and development of FPGA-based solutions using Verilog and industry-standard EDA tools.
- Developed, simulated, and debugged designs implementing high-speed interfaces.
- Performed both manual and automated testing through scripted control of test equipment in a lab setting.
- Built prototype designs to evaluate migrating to newer technologies such as recently-released FPGA families, new EDA tools, and runtime-reconfigurable toolflows.

Cigol Digital Systems Yokneam, Israel January 2013 - June 2013
Verification Engineer

- Performed black-box and white-box testing of all aspects of a combined hardware/software EDA system.
- Scripted the Tcl interface between the company's flagship product and several major third-party EDA tools.

University of Pennsylvania Philadelphia, PA, USA September 2009 - July 2011
Graduate Research Assistant

- Participated in a research group dedicated to FPGAs and other reconfigurable substraits, studying physical architecture, compute models, and electronic design automation.
- Researched the parallel/sequential tradeoff for energy minimization on reconfigurable multicontext devices.
- Extended a time-multiplexed router to map logical netlists to achievable hardware implementations.
- Integrated placement, clustering, and routing tools to build up new electronic design automation toolchains.
- Performed extensive design space exploration over various hardware- and software-based parameters, automating the execution and data collection of thousands of experiments at a time.

Lockheed Martin King of Prussia, PA, USA September 2007 - September 2009
Systems Integration / Test Engineer

- Acted in a variety of temporary roles across the corporation, including IT, information security, and R&D.

Air Force Research Laboratory Rome, NY, USA June 2007 - August 2007
Student Researcher

- Researched hardware-based enforcement of buffer bounds to make software more secure.
- Developed a working VHDL prototype, integrating the new technique onto an existing architecture.
- Specified and implemented ISA extensions, modifying microcode to control the newly-developed hardware.
- Co-authored publication (Ghose et al., *Architectural Support for Low Overhead Detection…*, DATE '09)

Personal Information

Spoken Languages: English (*native*), Hebrew (*advanced*), Japanese (*intermediate*)