## **Data Cache State Diagram**

Memory

Read From

Memory

if ~arbiter\_resp

if arbiter\_resp

if arbiter\_resp

LD\_valid = 1

if arbiter\_resp

DEFAULT
mem\_w\_cache = 0;
cpu\_w\_cache = 0;
LD\_dirty = 0;
LD\_valid = 0;
LD\_LRU = 0;
mem\_resp\_cpu = 0;
write i = 0;

if ~dirty

LD LRU = HIT

mem\_resp\_cpu = <

HIT

LD\_dirty = HIT & write

if arbiter\_resp read\_i =1

if ~arbiter\_resp read\_i =1

if arbiter\_resp

read\_i =0

-wew I 8 -wew w HALT if mem\_r/mem\_w HIT &~mem\_r & ~mem\_w > if mem\_r/mem\_w & HIT CHECK cpu\_w\_cache = ~dirty & mem\_w if ~HIT Write i = dirty Buffer Read\_i = ~dirty if ~arbiter\_resp write\_i =1 Write to arbiter\_resp