

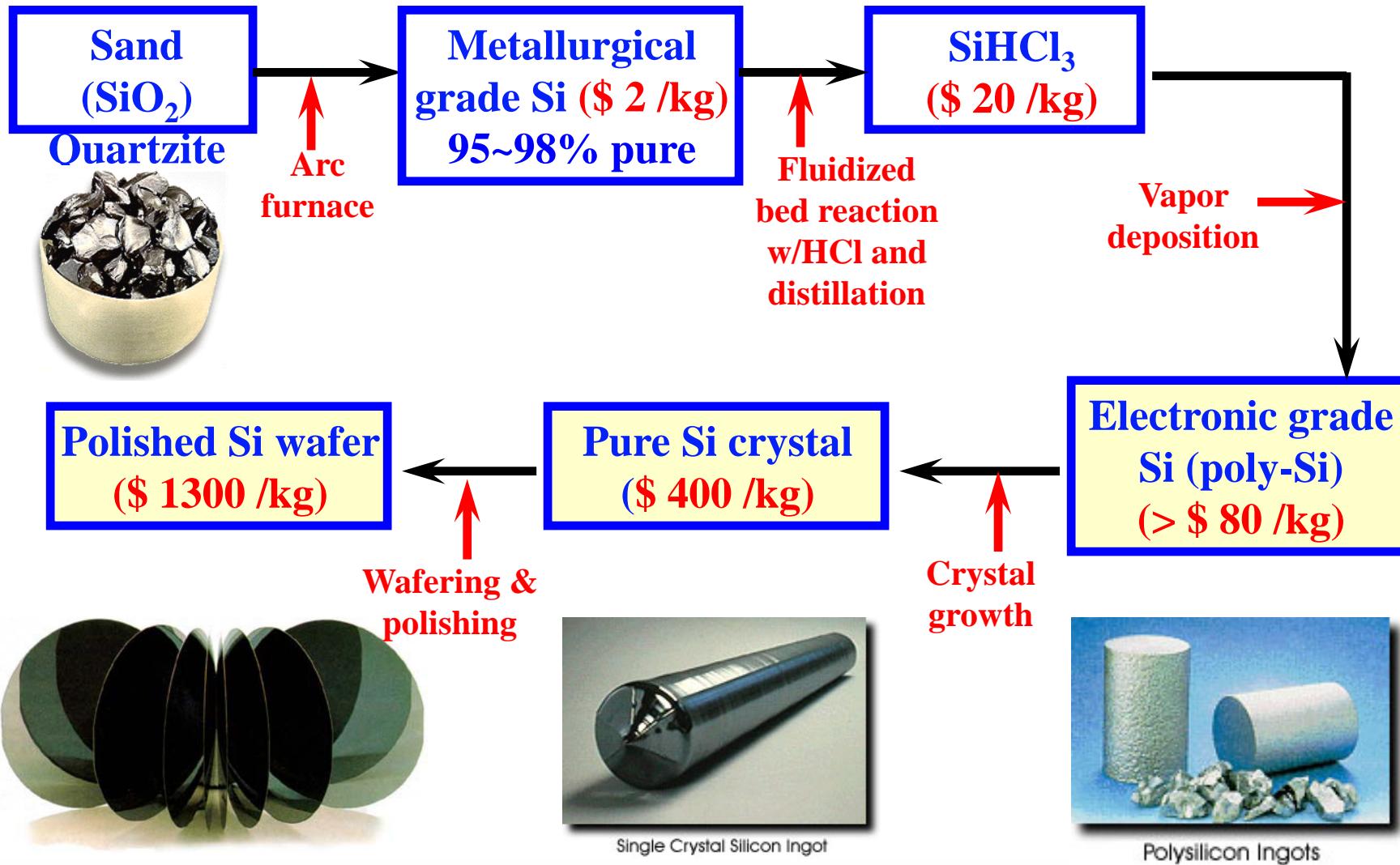
Digital Integrated Circuits

A Design Perspective

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

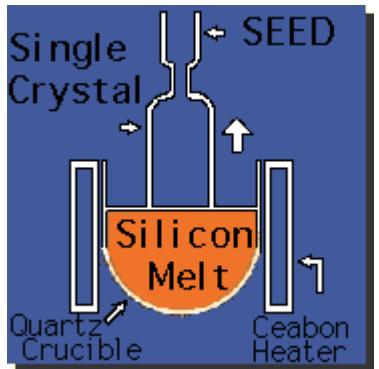
Manufacturing Process

Sand to silicon wafer



Source: <http://www.fullman.com/semiconductors/semiconductors.html>

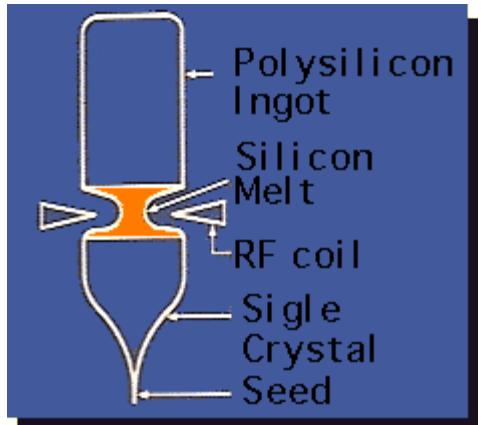
Czochralski (CZ) and float-zone (FZ) techniques



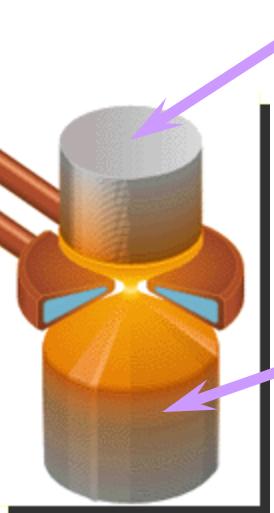
CZ



Poly-Si



FZ

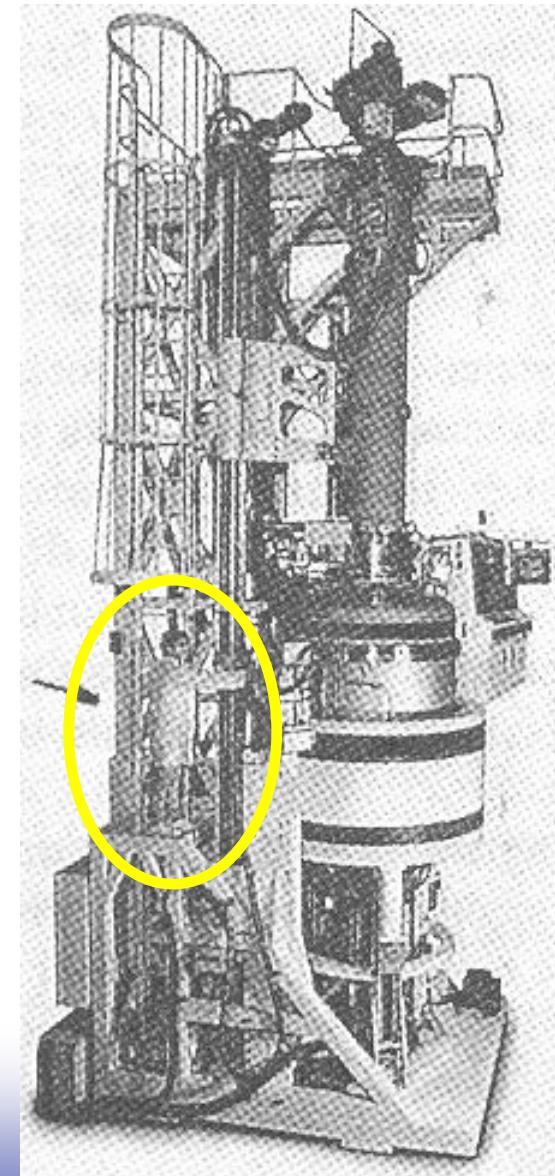
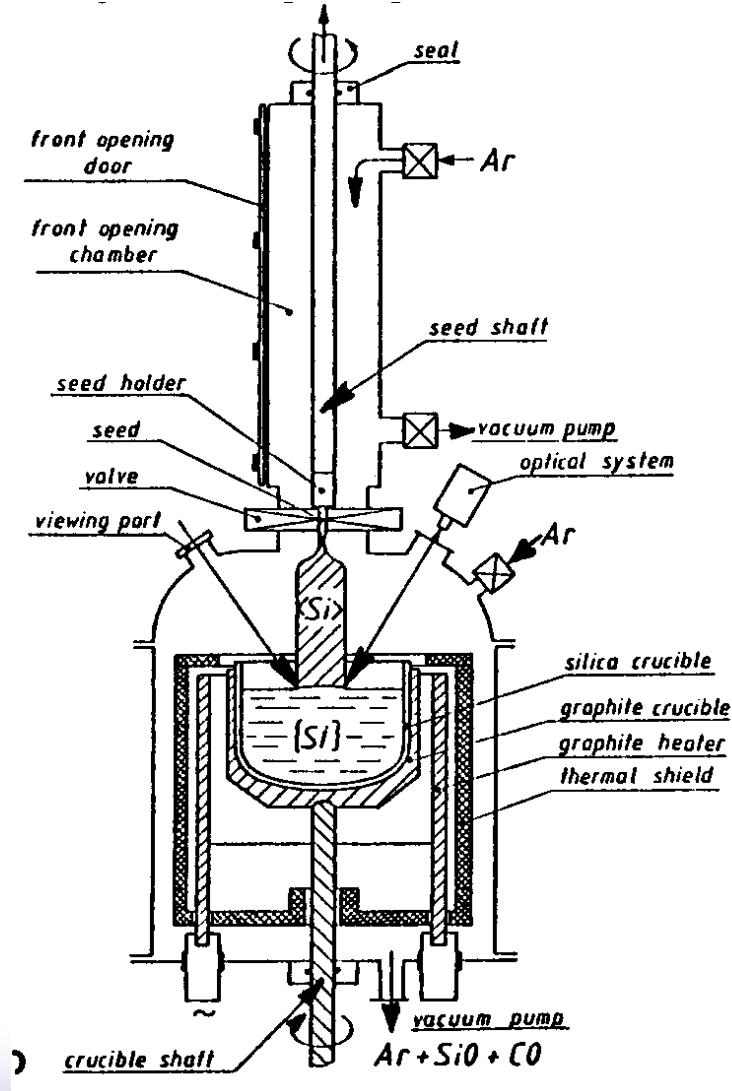


Single crystal Si

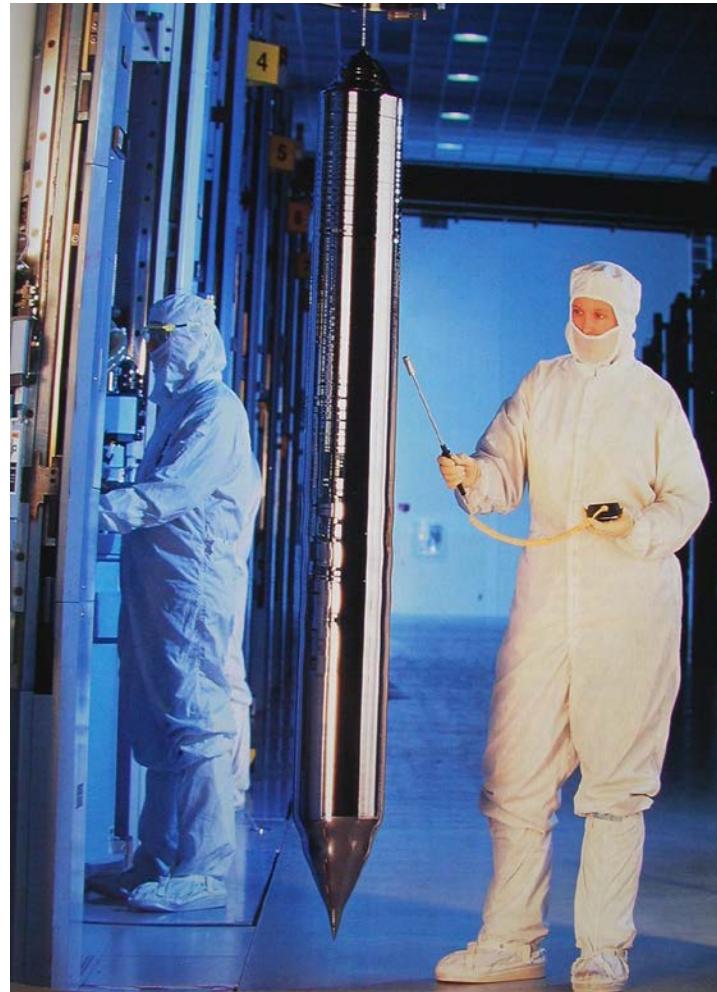
Poly-Si

Sources: <http://www.fullman.com/semiconductors/semiconductors.html>
<http://www.msil.ab.psiweb.com/english/msilhist0-e.html>

300 mm diameter wafer CZ puller



Growing the Silicon Ingot

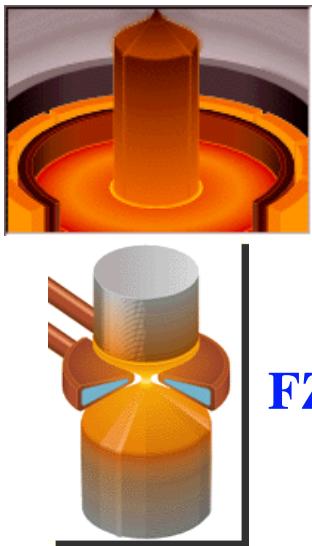


From Smithsonian, 2000

5

Manufacturing

Ingot to wafer

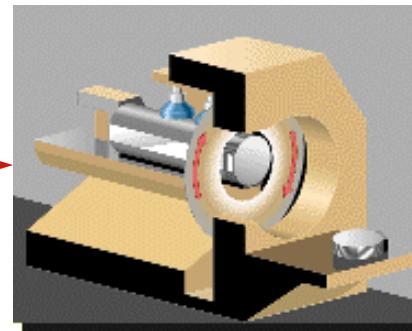


CZ →

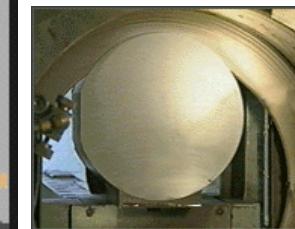


FZ →

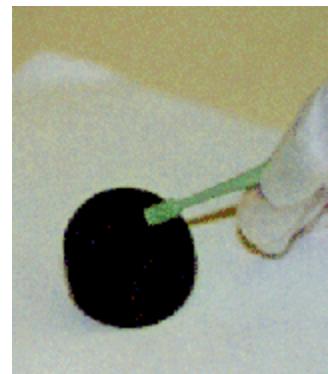
Ingot



Slicing

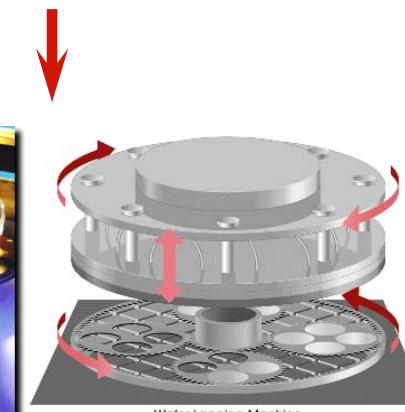


Wafers for IC
manufacturing



Water Polishing
(Strasbaugh Corporation)

Polishing



Wafer Lapping Machine
(Mitsubishi Materials Silicon)

Lapping

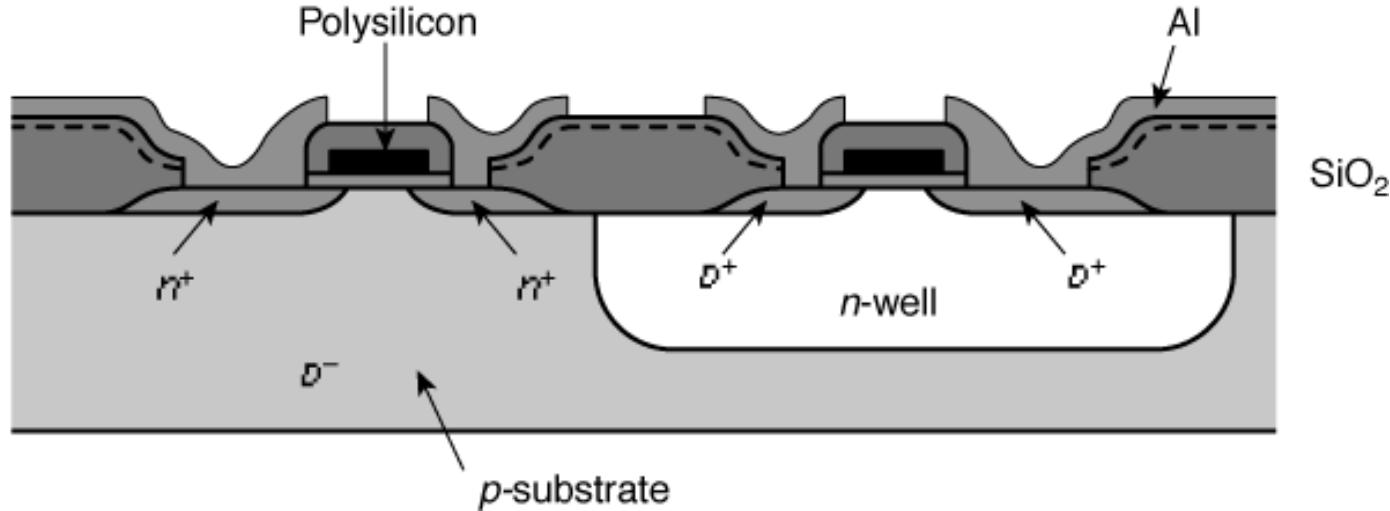
Sources: <http://www.fullman.com/semiconductors/semiconductors.html>
<http://www.msil.ab.psiweb.com/english/msilhist0-e.html>

Planarization: Polishing the Wafers

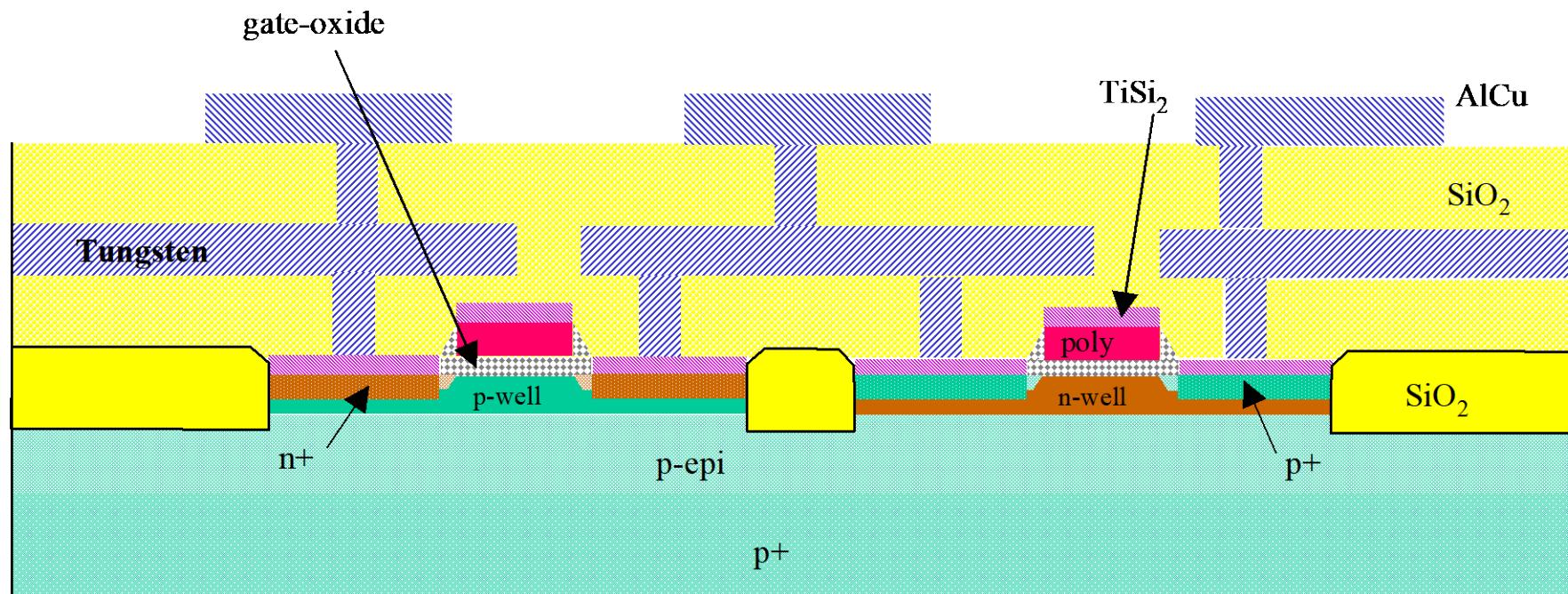


From Smithsonian, 2000

CMOS Process

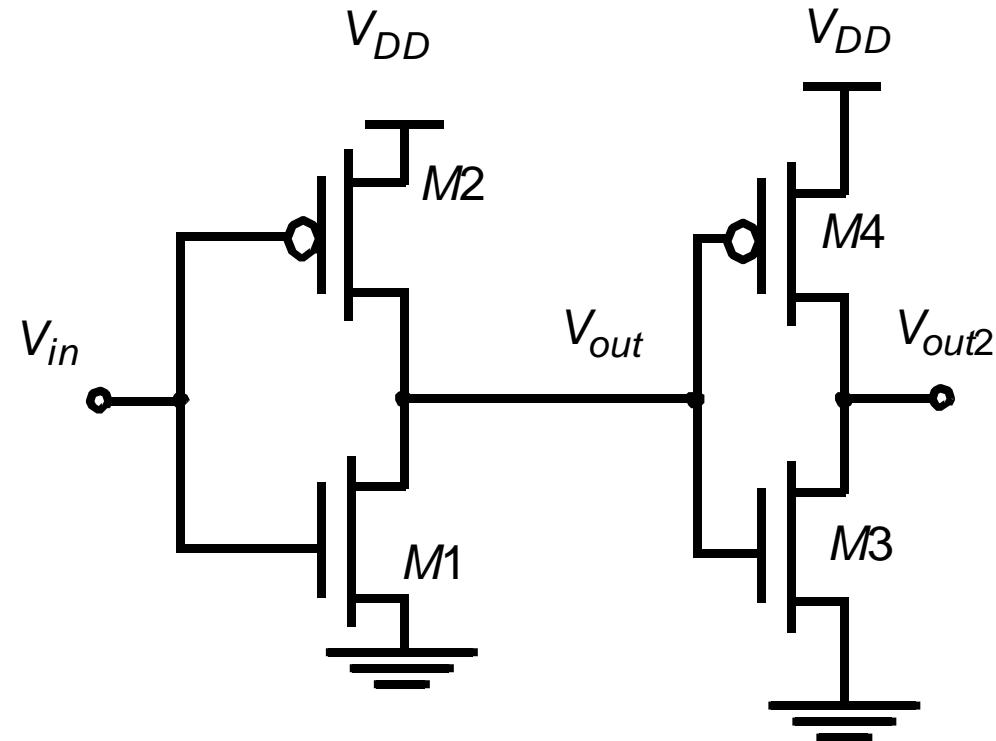


A Modern CMOS Process



Dual-Well Trench-Isolated CMOS Process

Circuit Under Design



Its Layout View

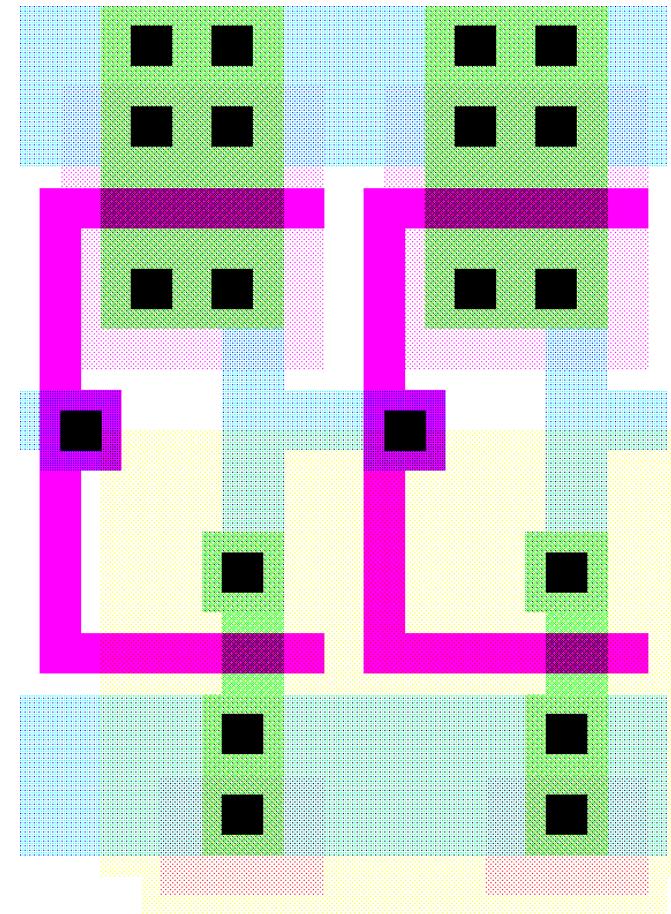
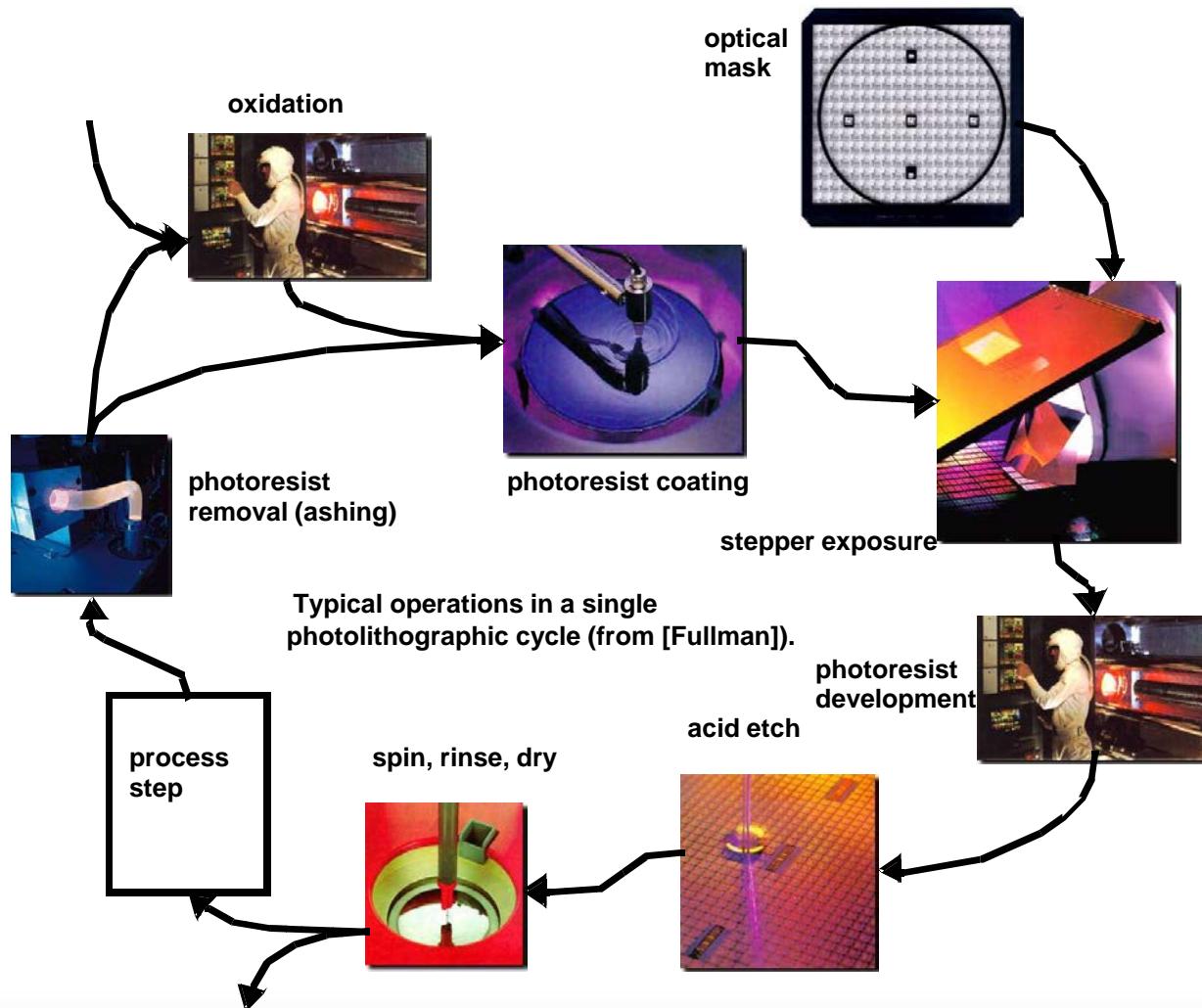
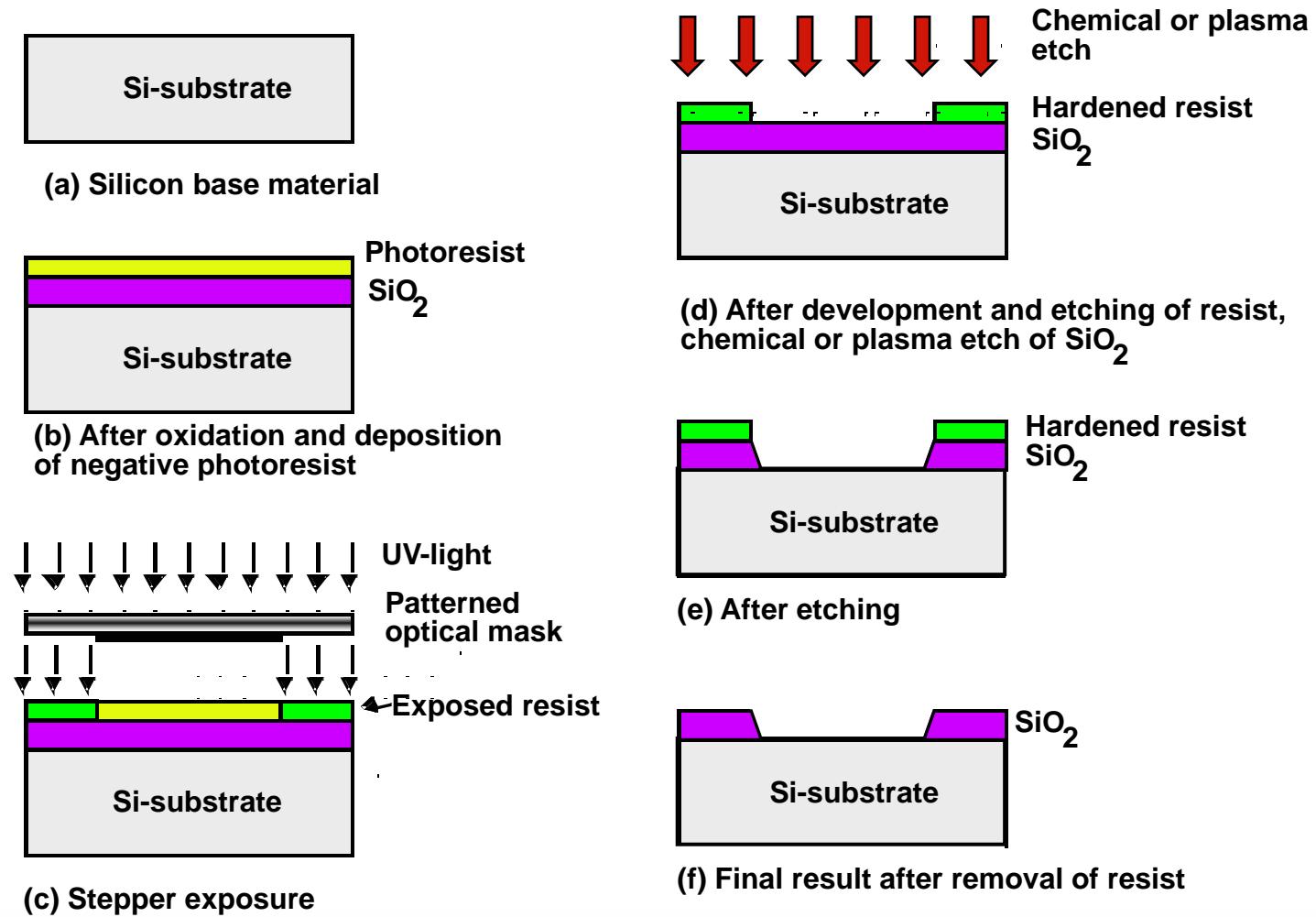


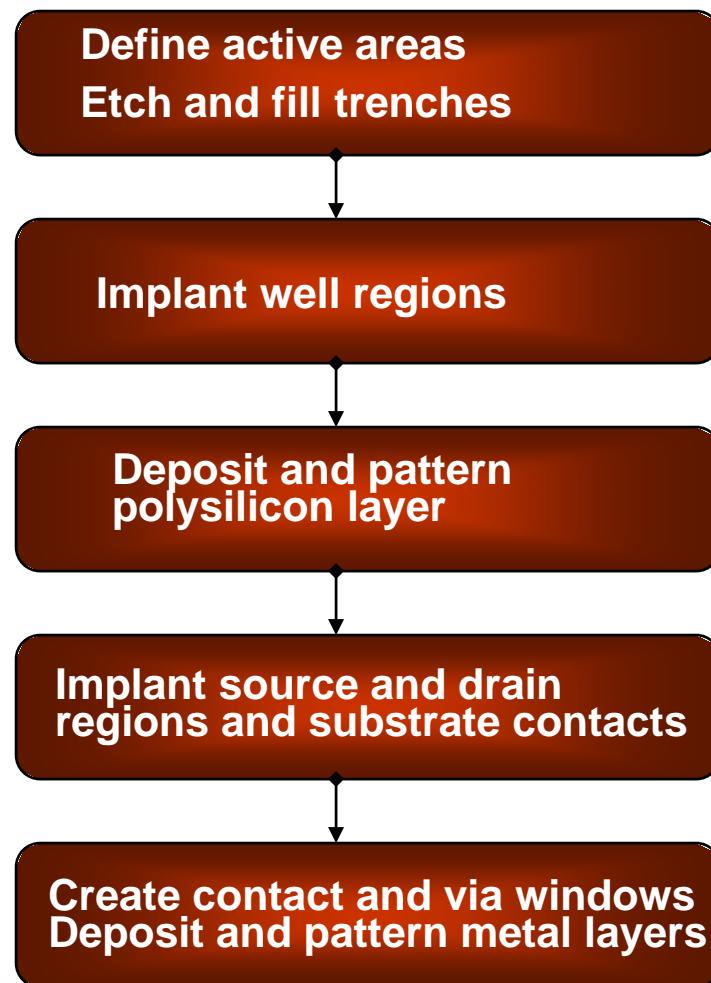
Photo-Lithographic Process



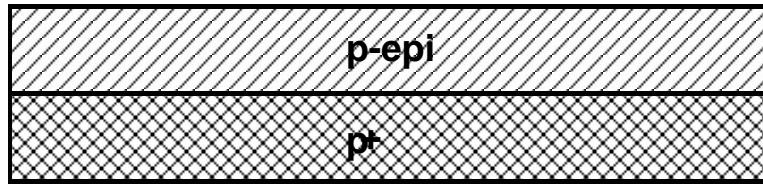
Patterning of SiO_2



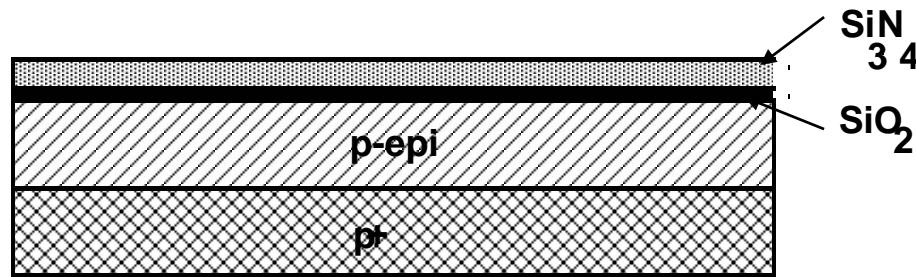
CMOS Process at a Glance



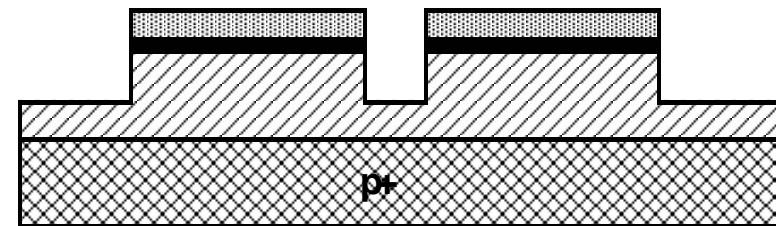
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

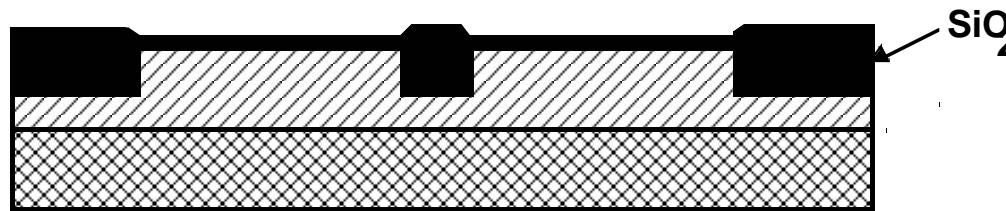


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

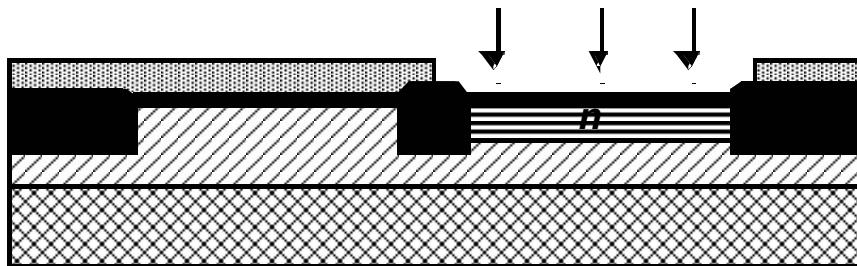


(c) After plasma etch of insulating trenches using the inverse of the active area mask

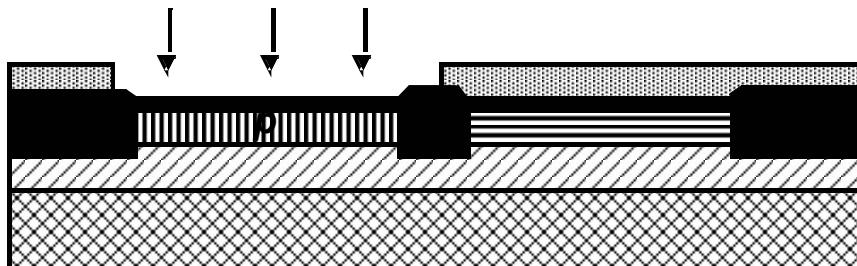
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

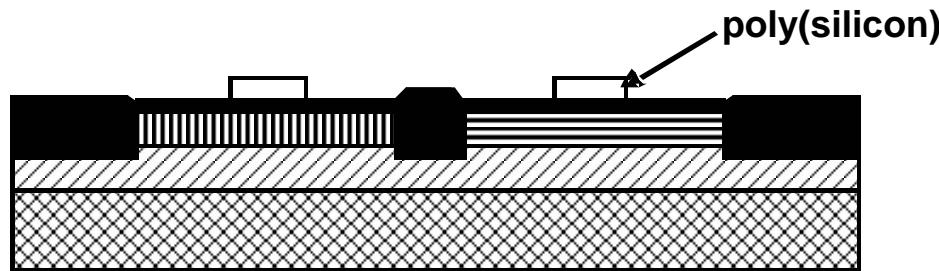


(e) After n-well and $\sqrt{T_p}$ adjust implants

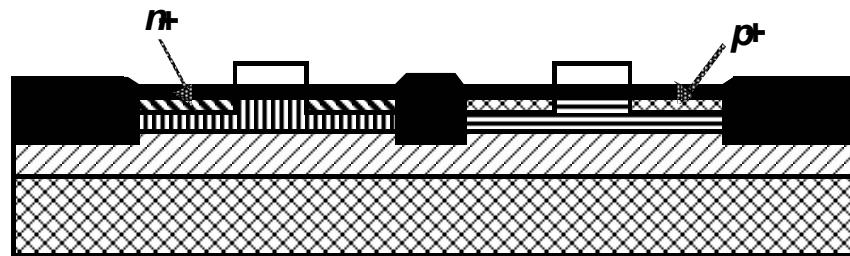


(f) After p-well and $\sqrt{T_n}$ adjust implants

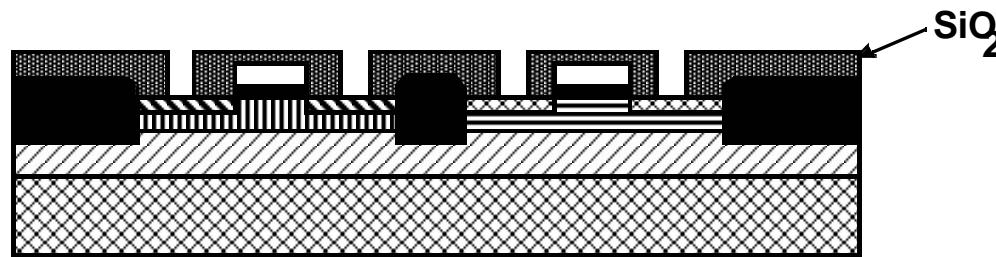
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

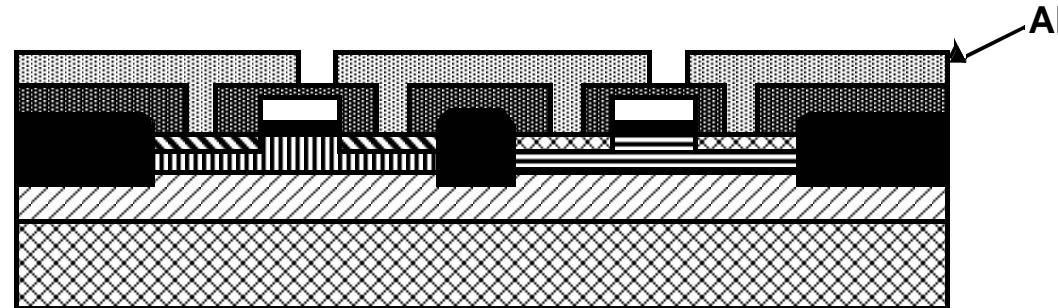


(h) After $n+$ source/drain and $p+$ -source/drain implants. These steps also dope the polysilicon.

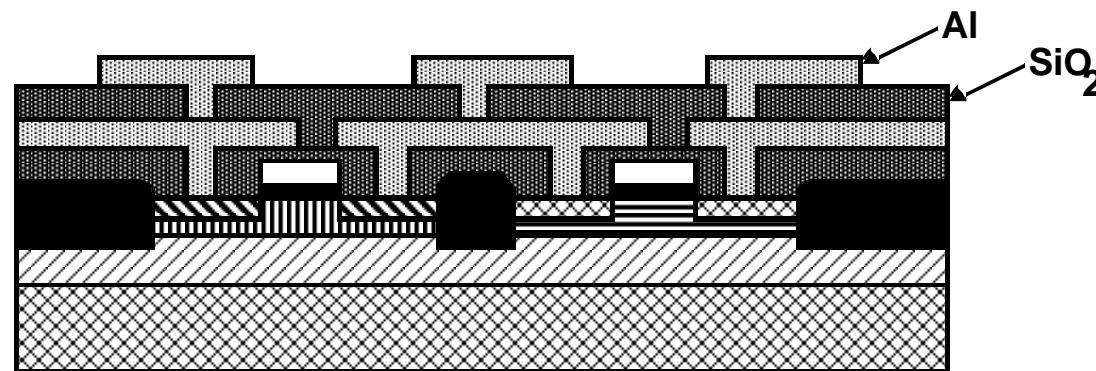


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

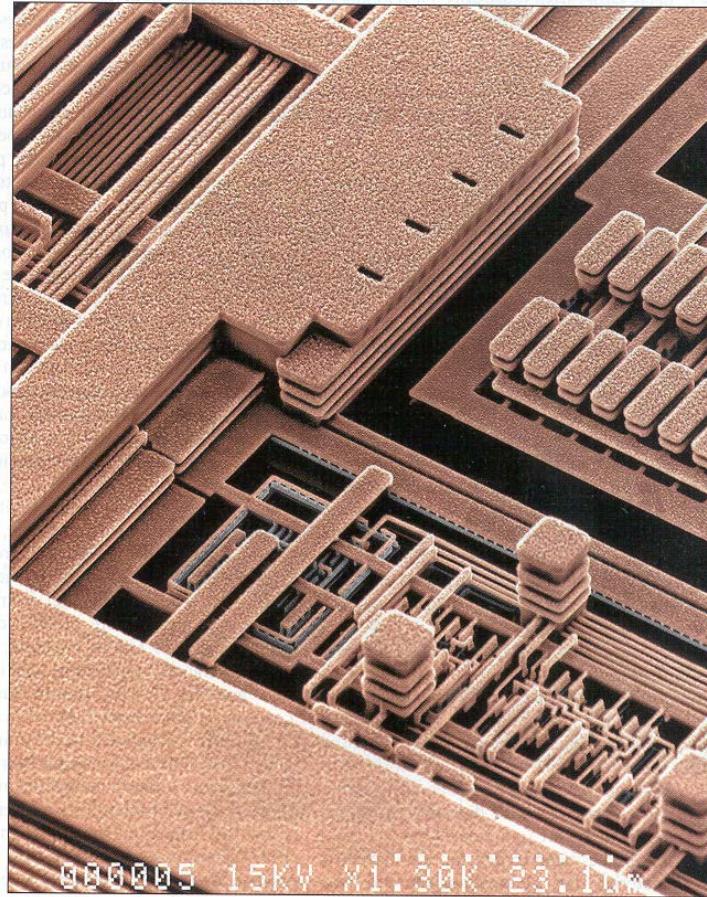
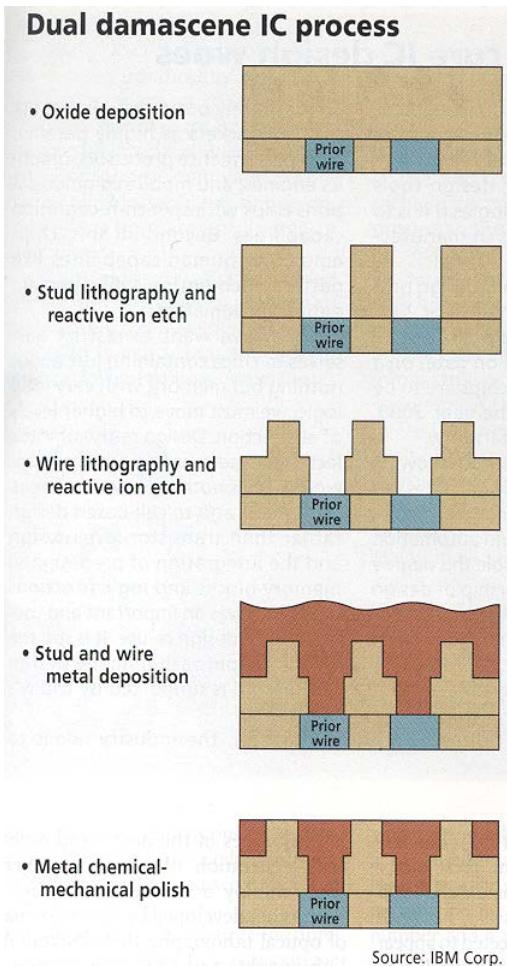


(j) After deposition and patterning of first Al layer.

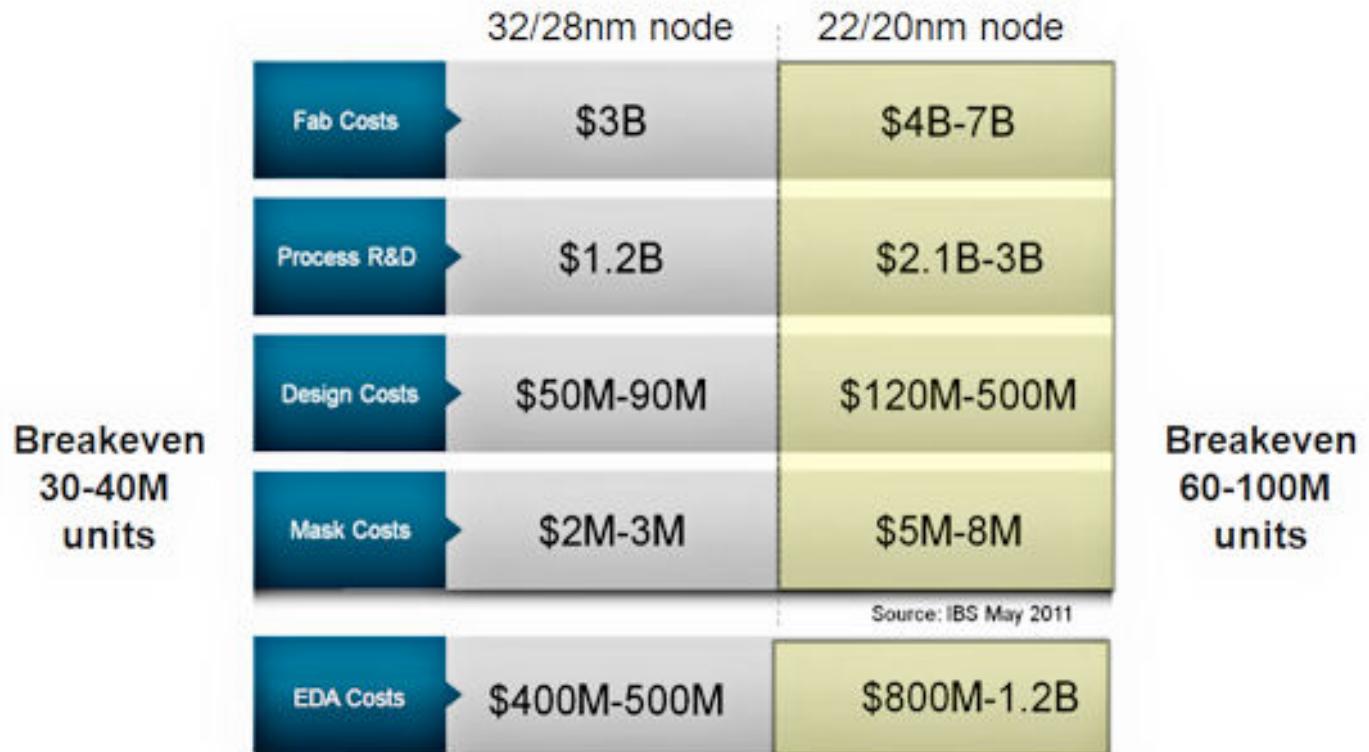


(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

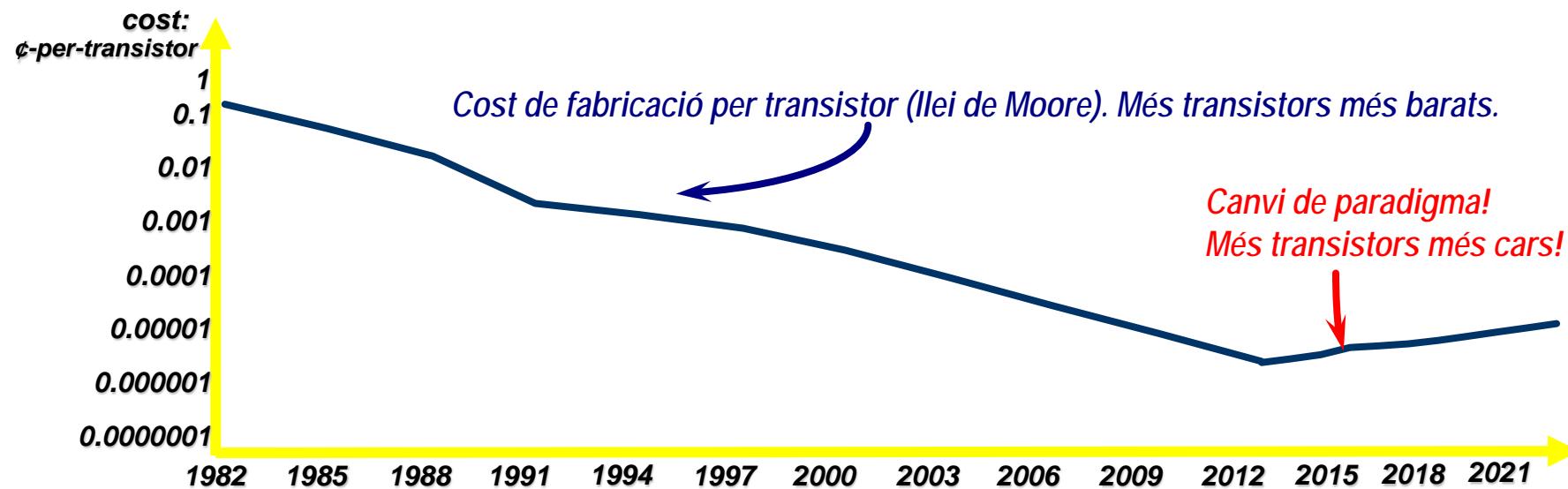
Advanced Metallization



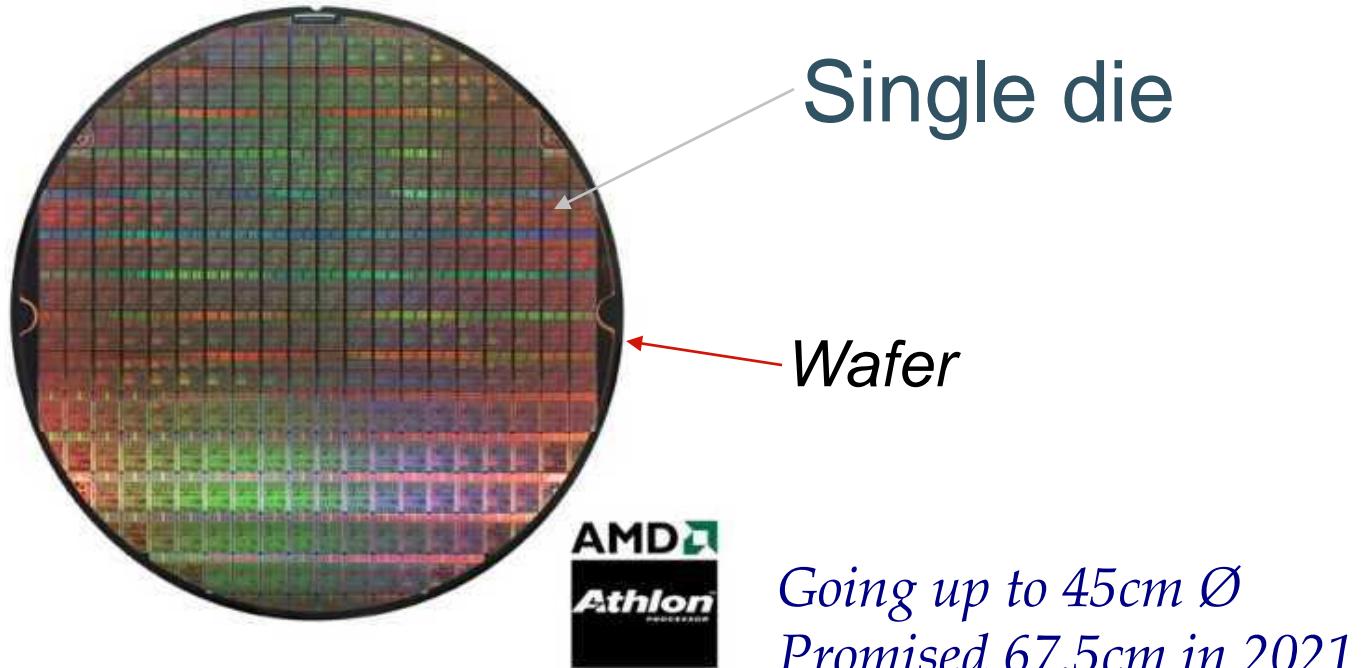
Manufacturing costs



Cost per Transistor



Die Cost

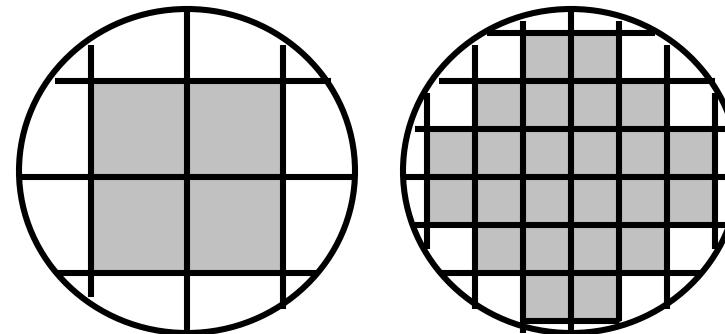


Yield

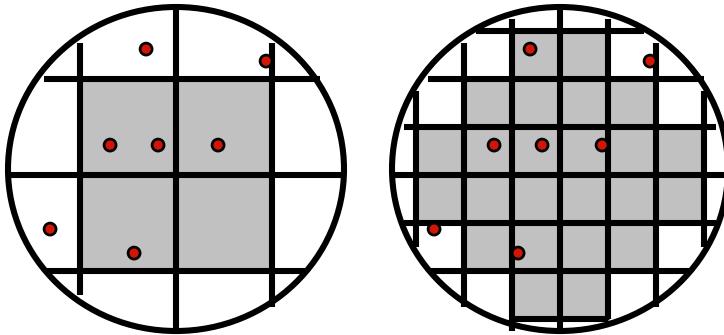
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



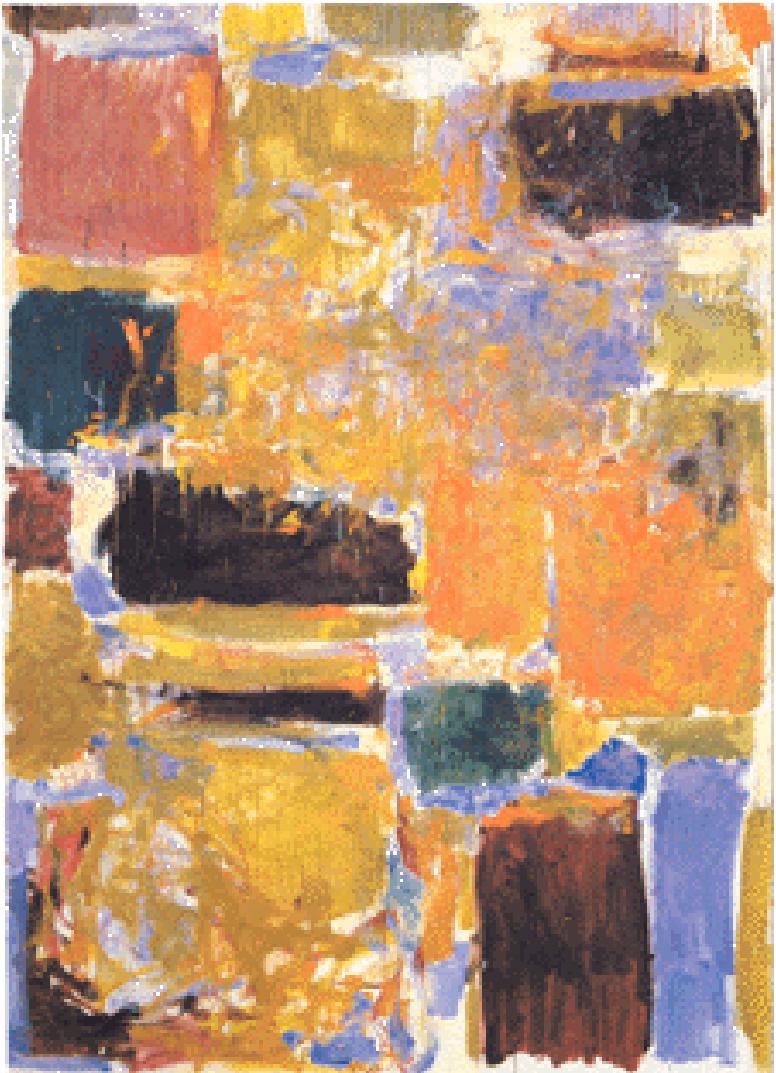
Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

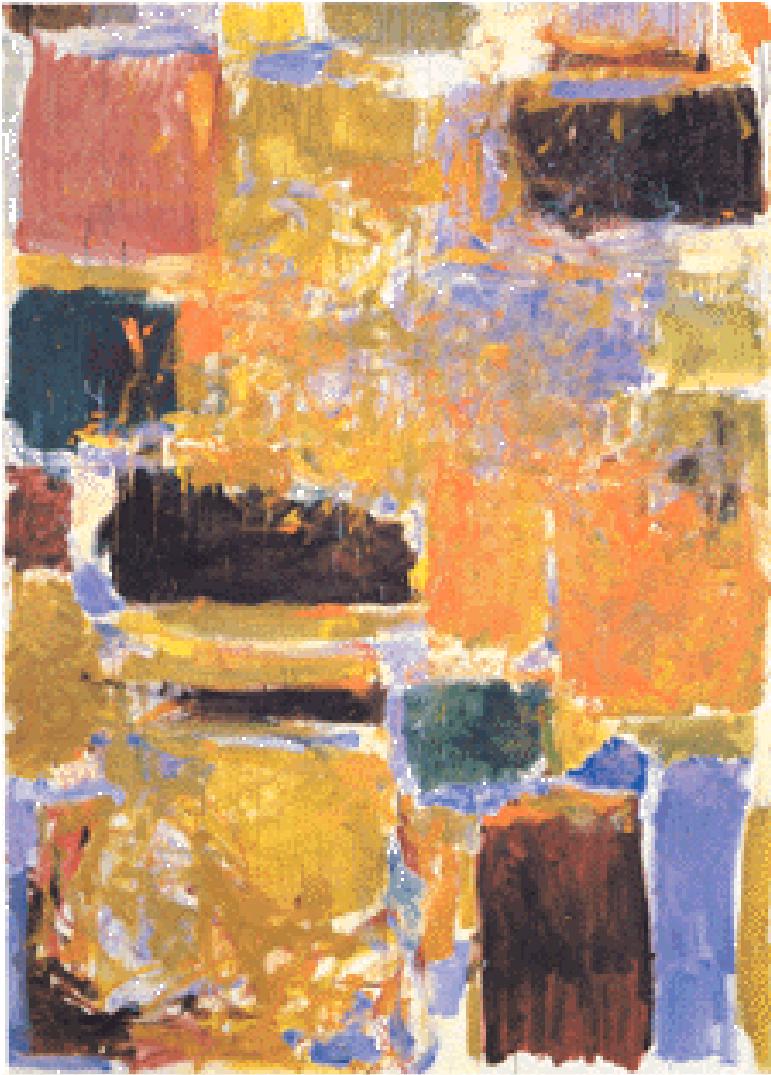


Digital Integrated Circuits

A Design Perspective

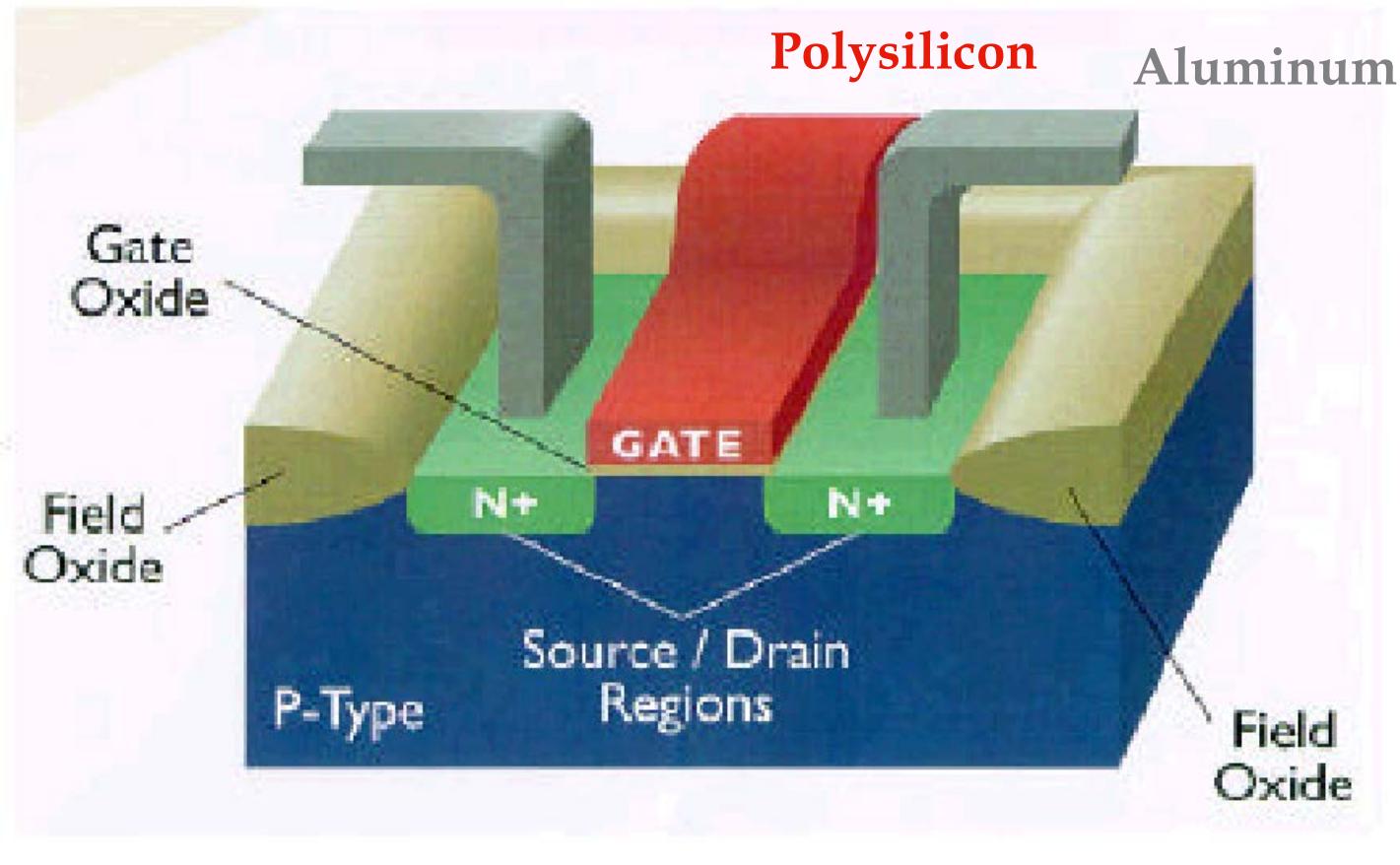
Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

Manufacturing Process



Design Rules

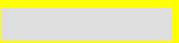
3D Perspective



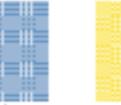
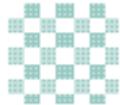
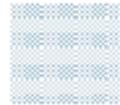
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions (micron rules)

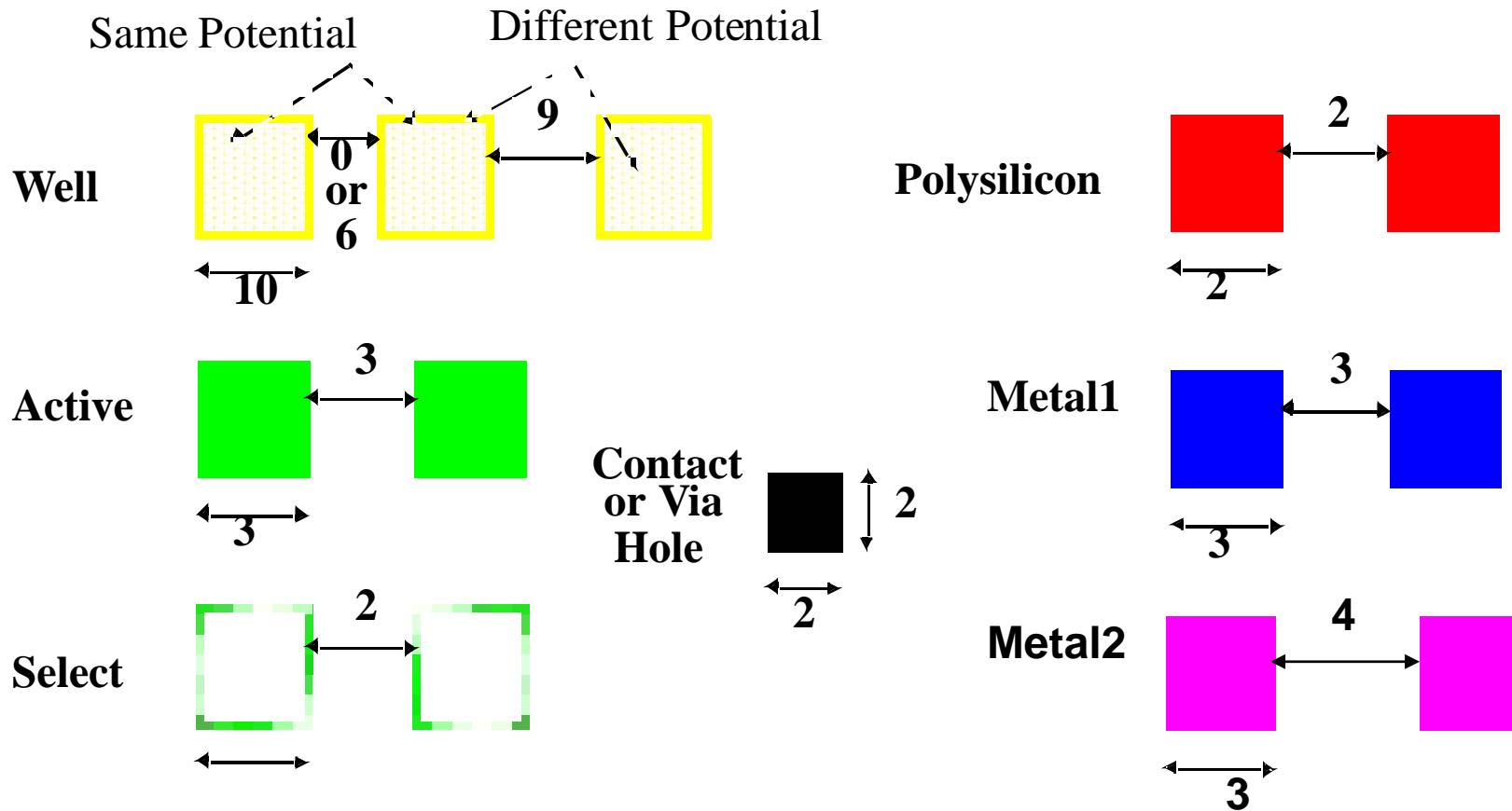
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

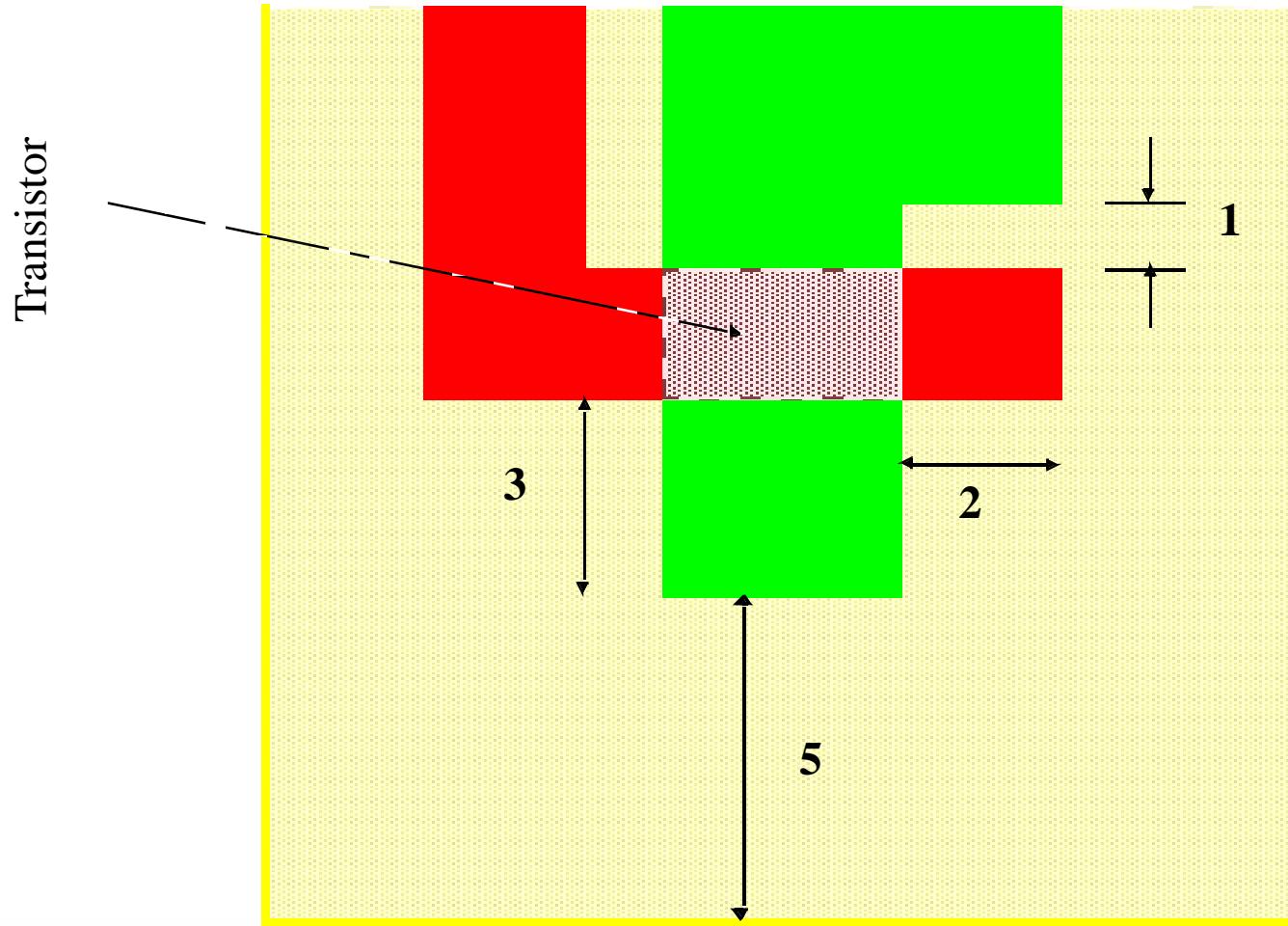
Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal					
well					
polysilicon					
contacts & vias					
active area and FETs					
select					

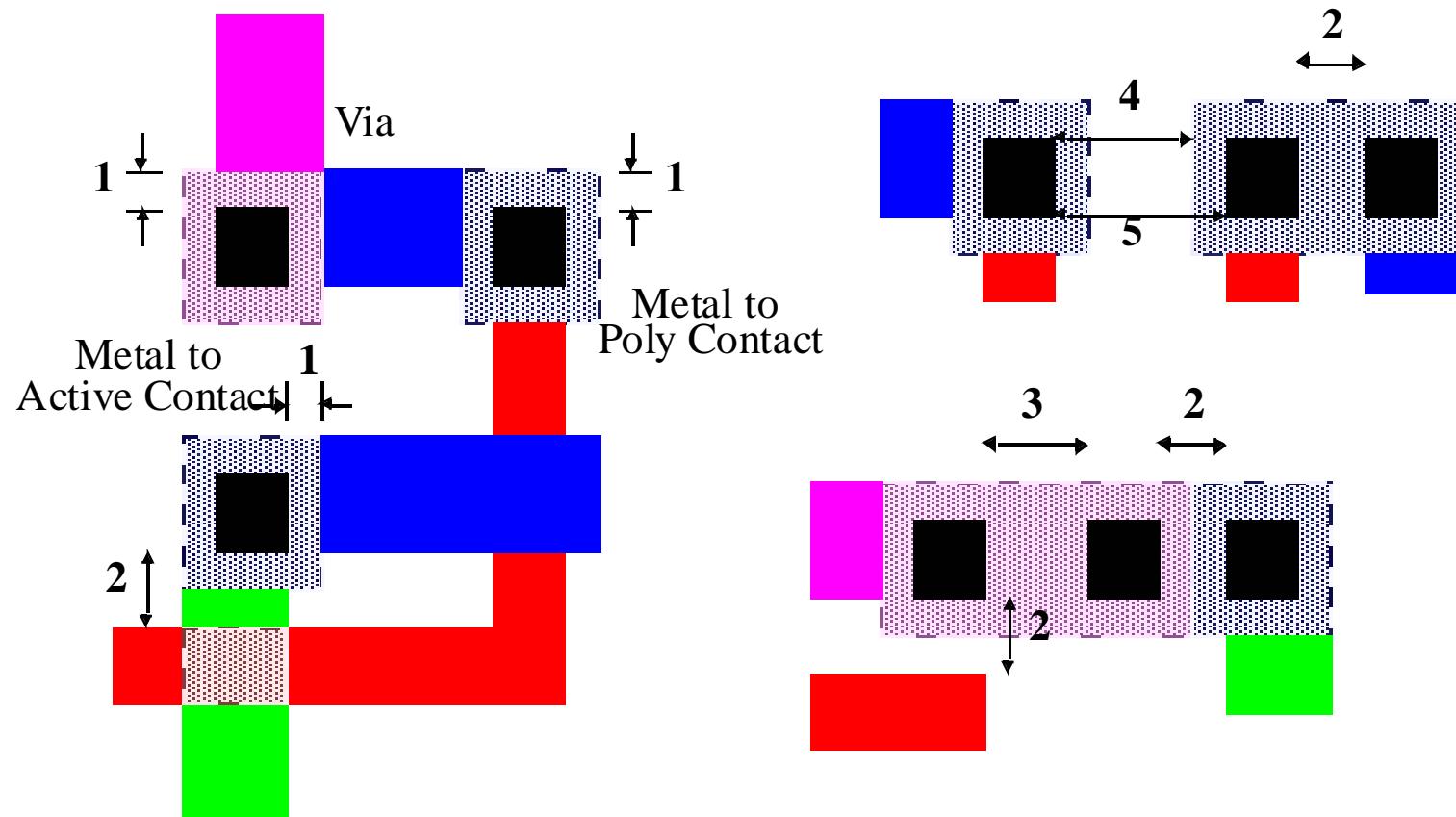
Intra-Layer Design Rules



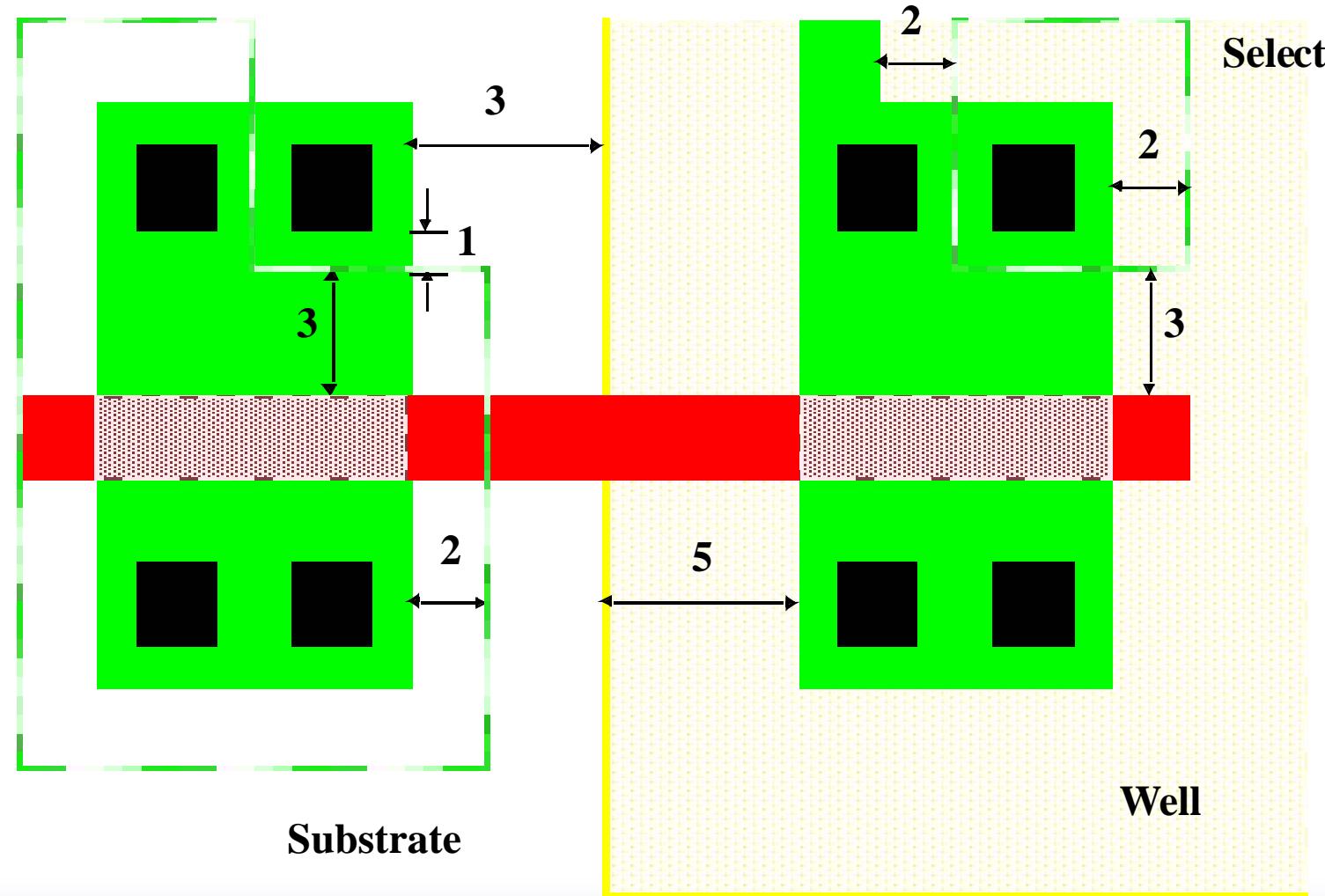
Transistor Layout



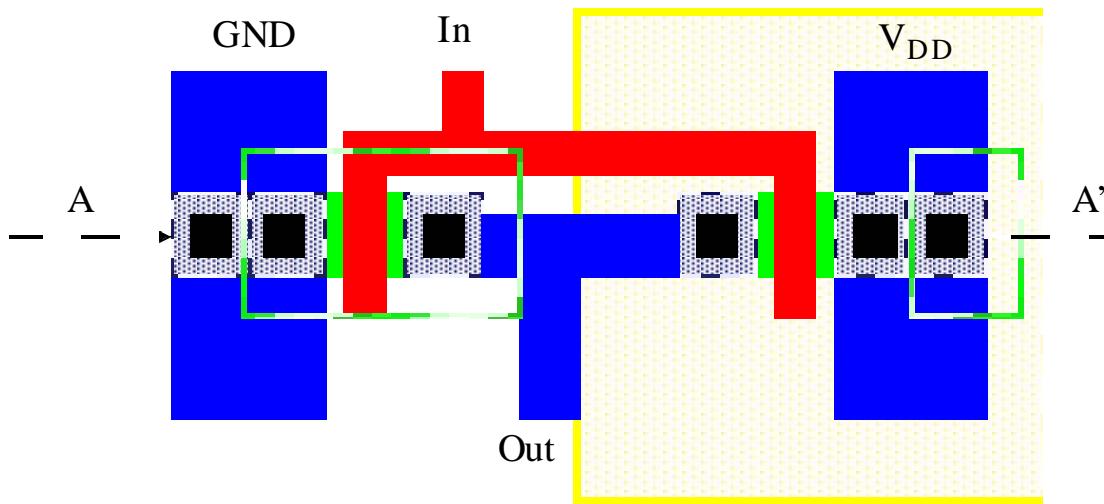
Vias and Contacts



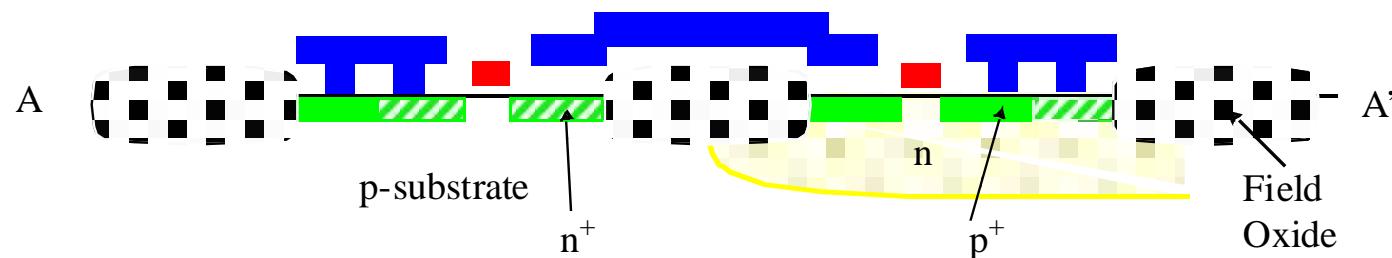
Select Layer



CMOS Inverter Layout

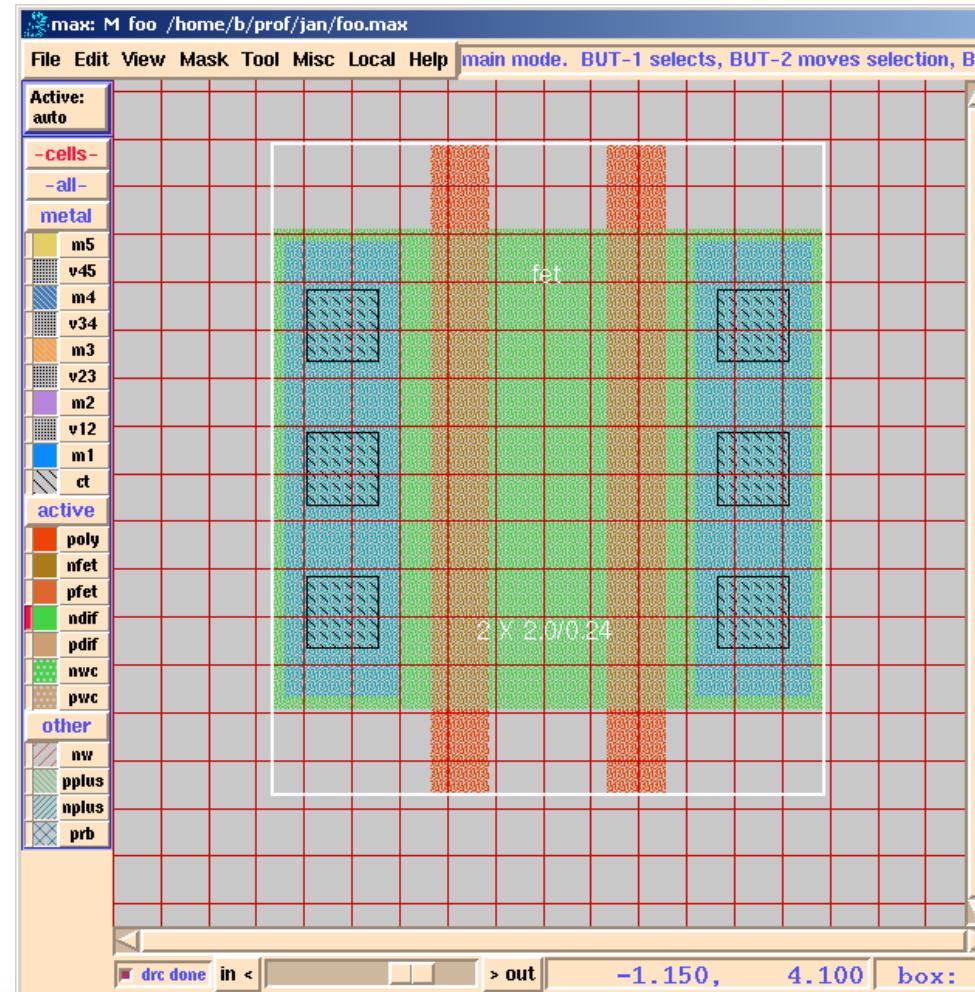


(a) Layout

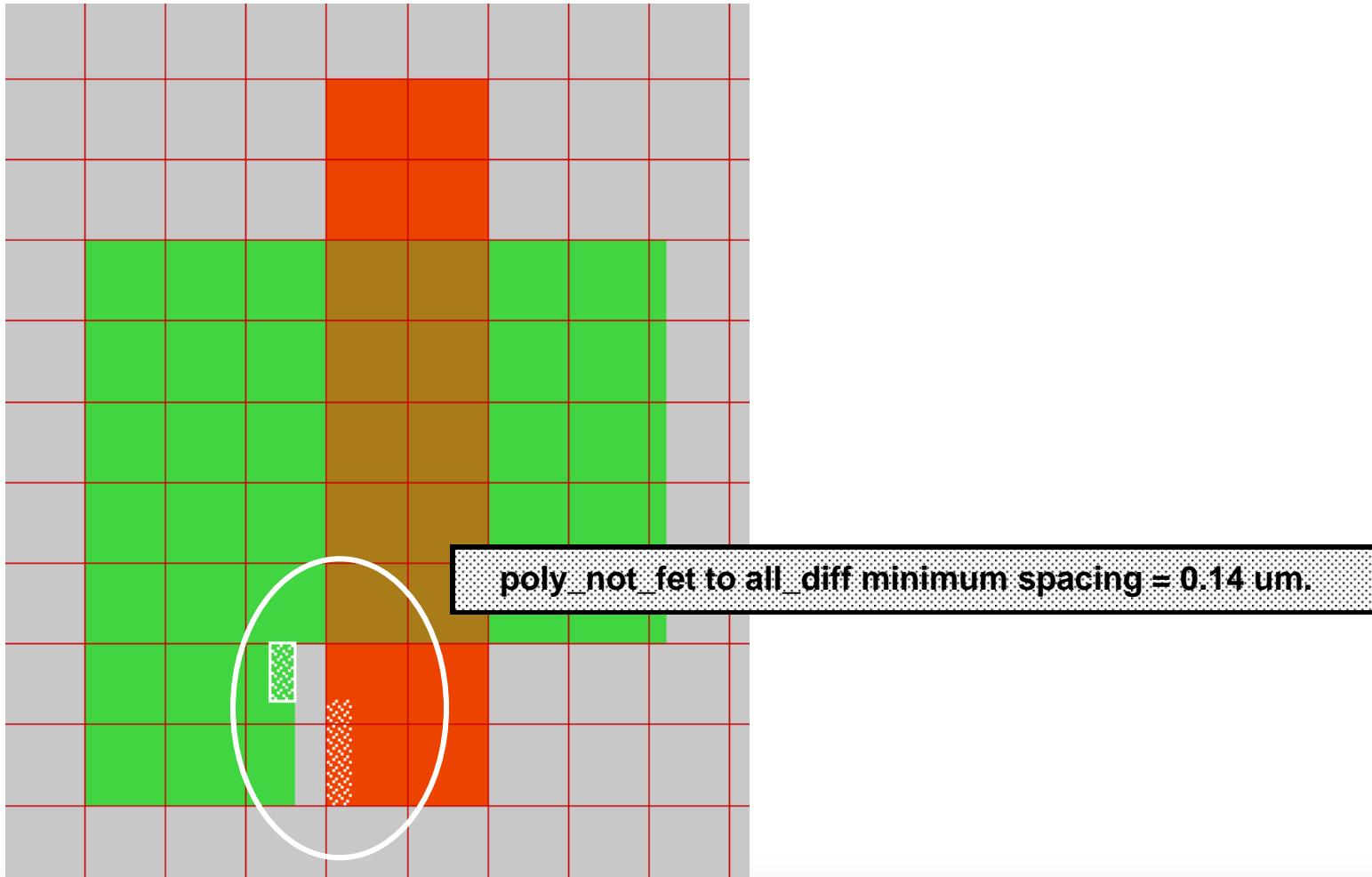


(b) Cross-Section along A-A'

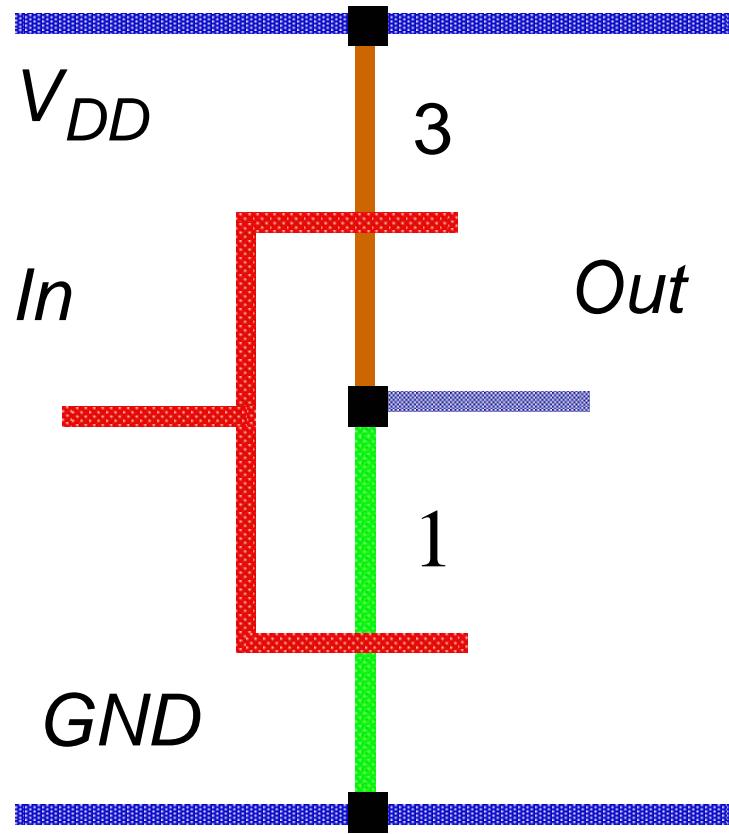
Layout Editor



Design Rule Checker



Sticks Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

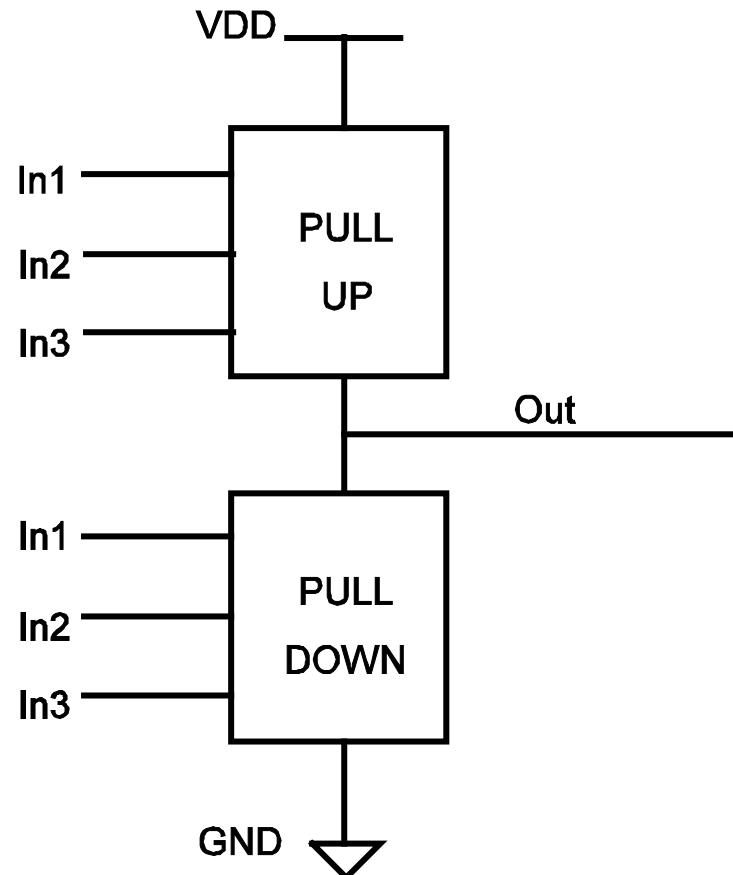
Case study

Standard Cell implementation

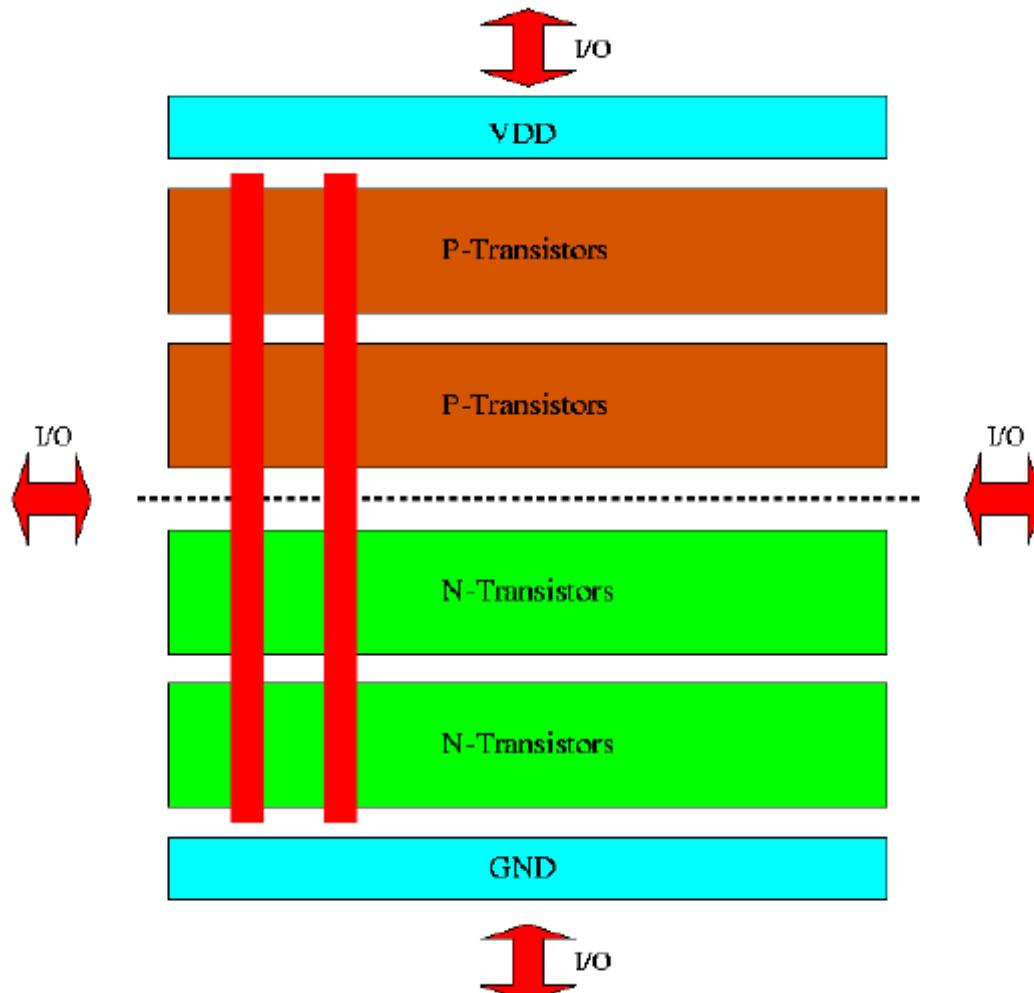
Standard Cell Implementation

- Cells designed in a certain pattern
 - Due to the *standard* pattern they can be used in several circuits
-
- + Design reuse
 - Non-adaptative design

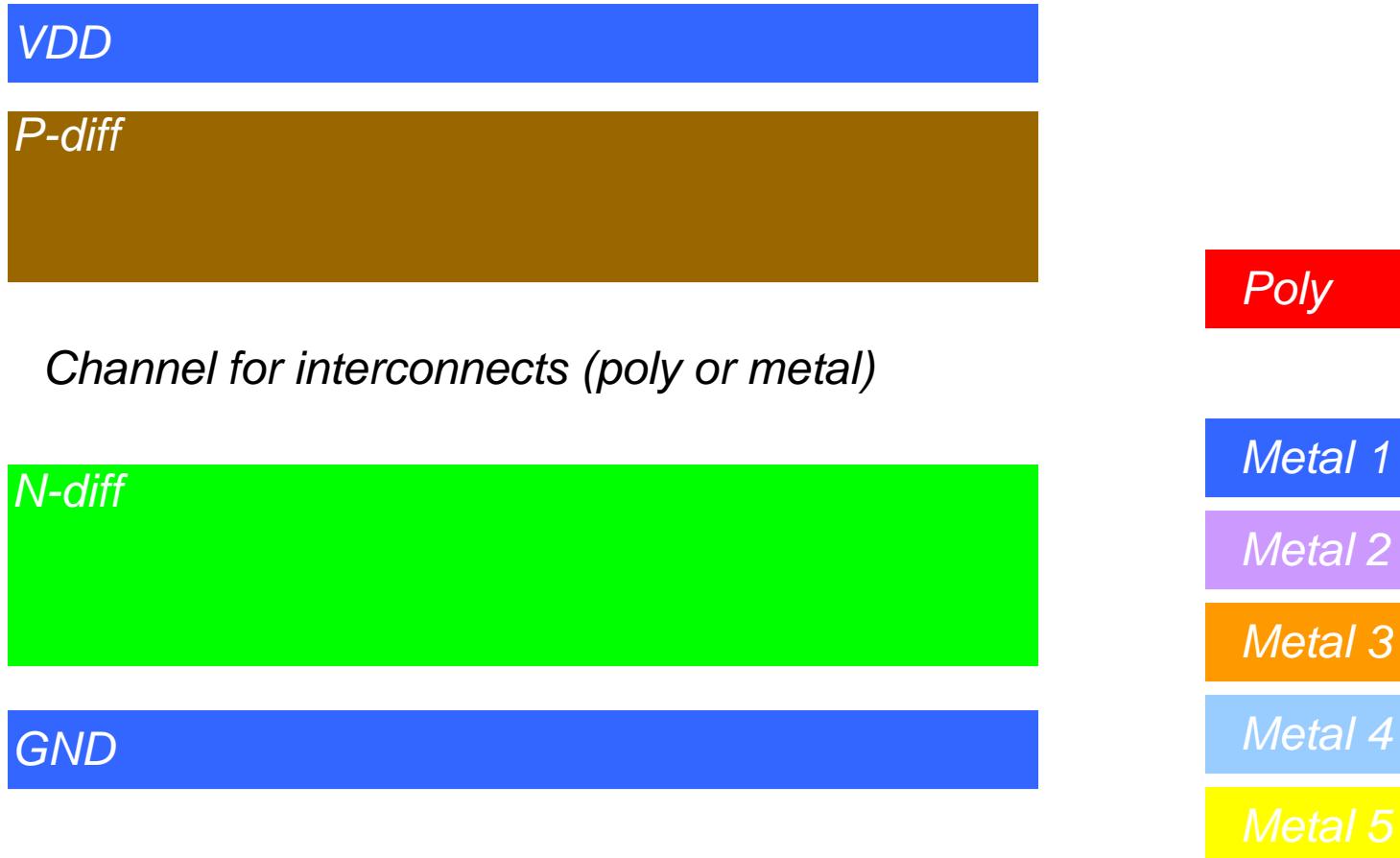
A typical MOS gate



Standard Cell Structure

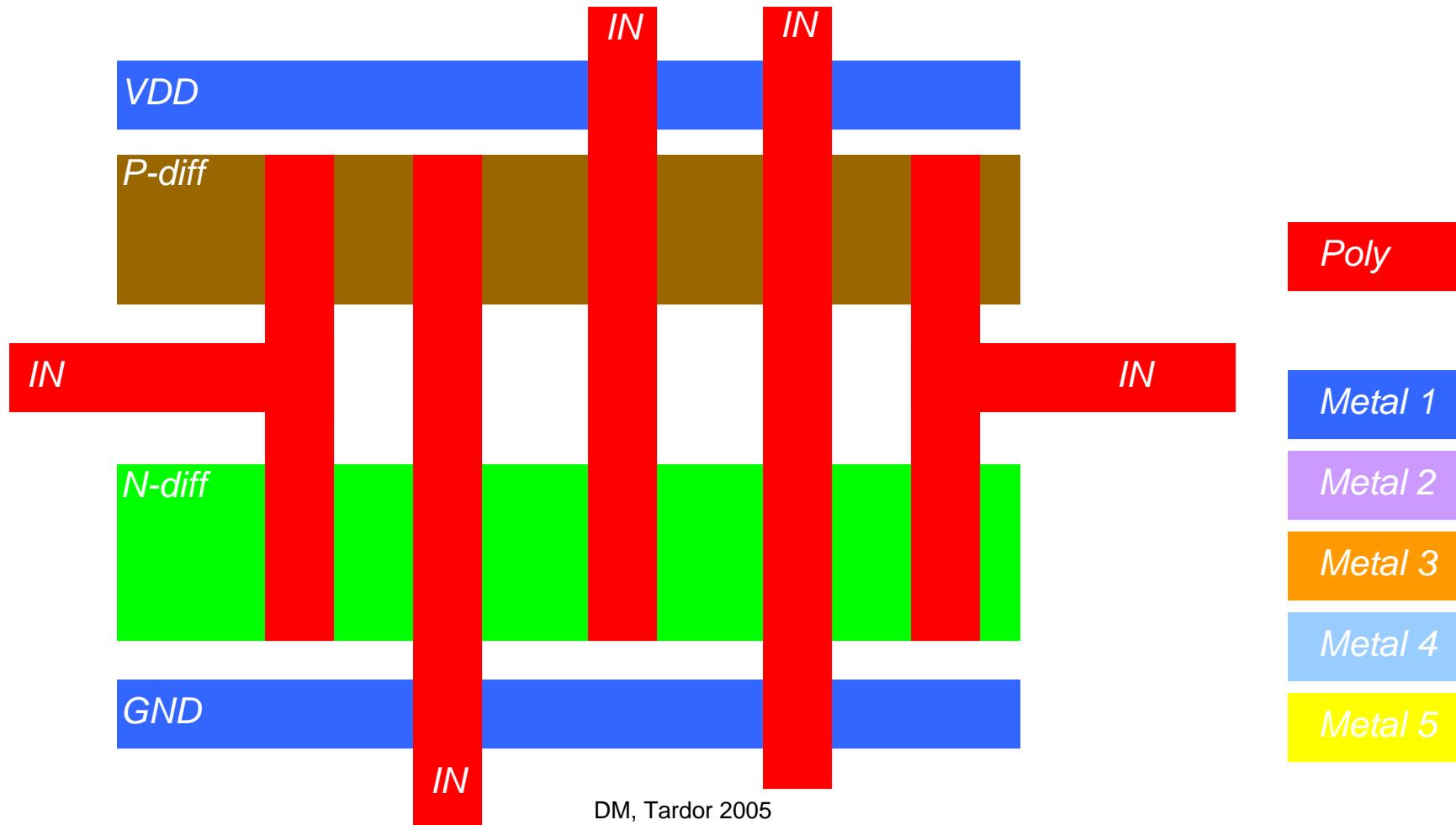


Standard Cell Structure



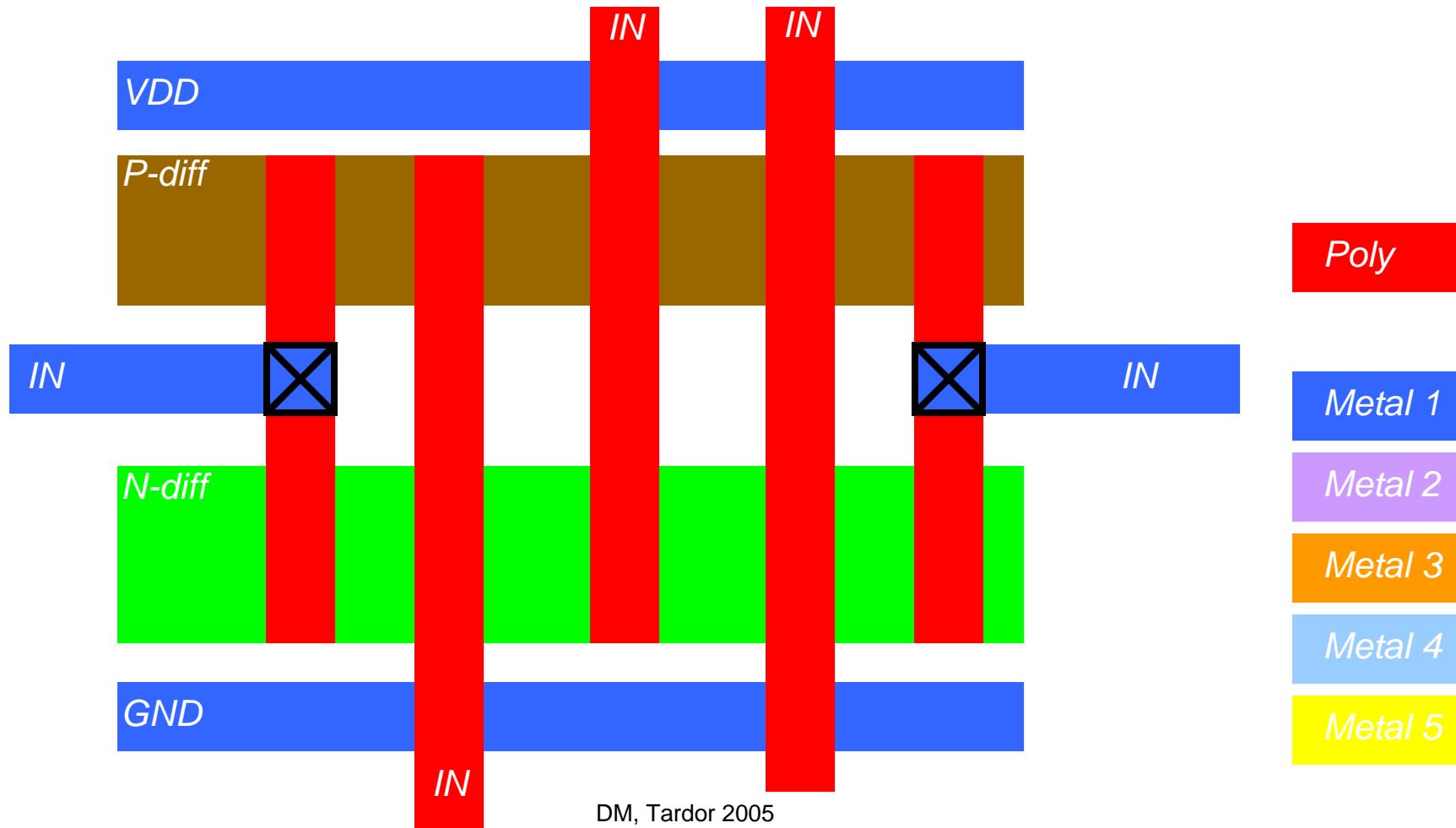
Standard Cell Structure

The inputs of the transistors are connected to the poly layer. Horizontal connections are not recommendable since they increase the manufacturing costs.



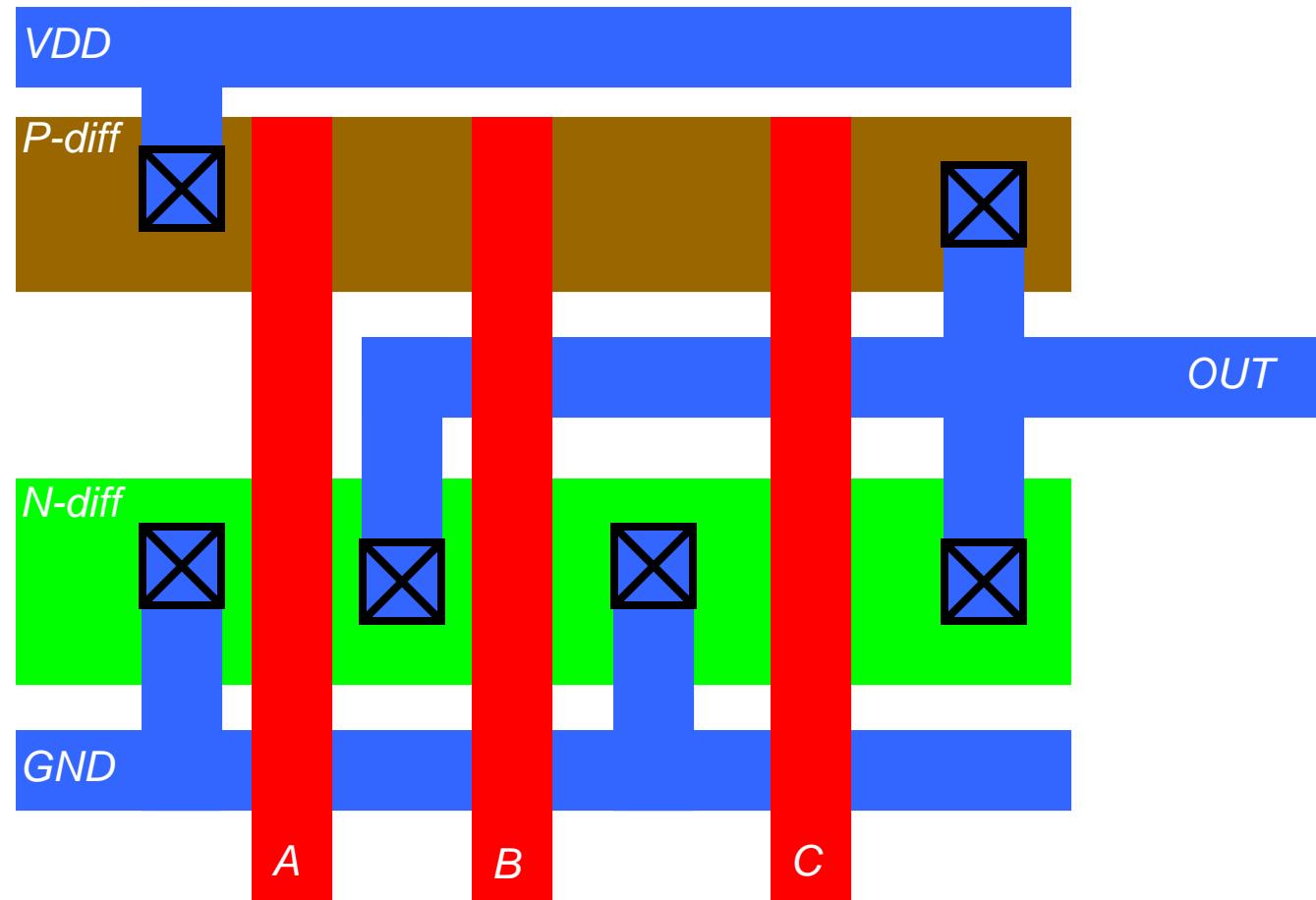
Standard Cell Structure

The inputs of the transistors are connected to poly or to metal –in case they are lateral inputs.



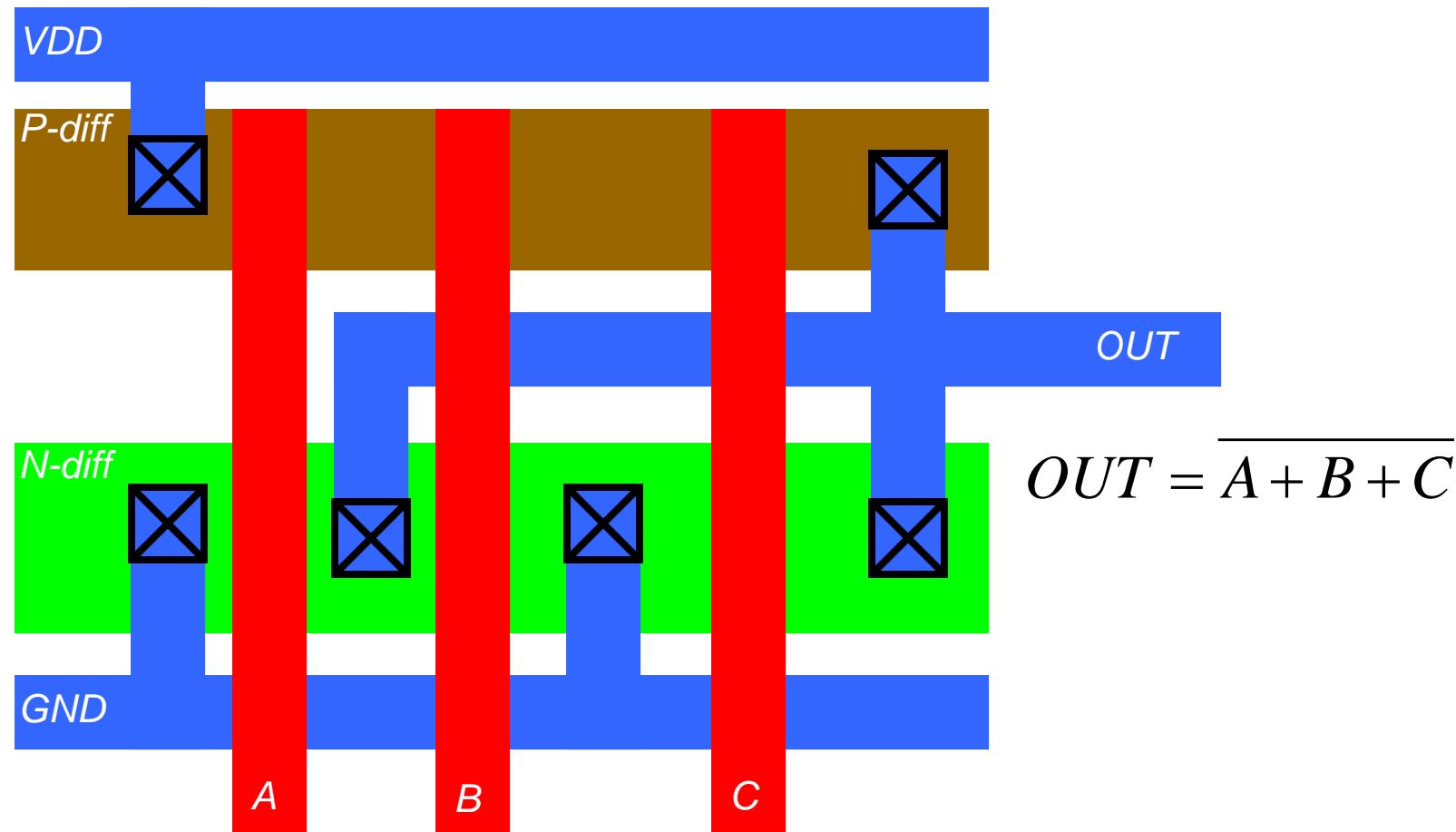
Standard Cell Structure

Transistors are placed in a serial way. If we want them in parallel we will have to add metal connections.



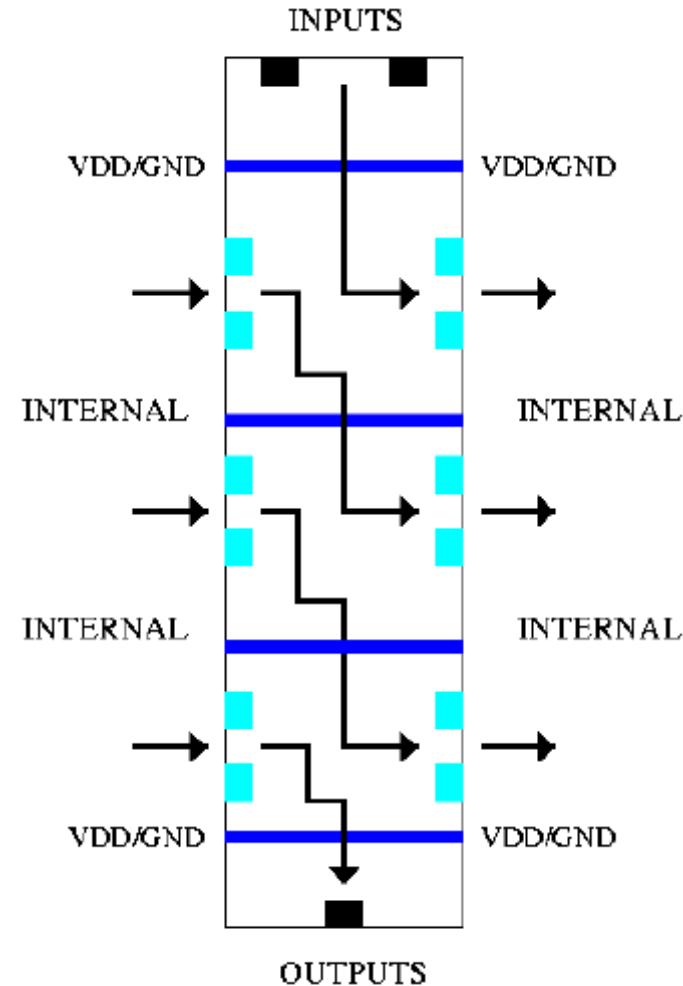
Standard Cell Structure

Transistors are placed in a serial way. If we want them in parallel we will have to add metal connections.



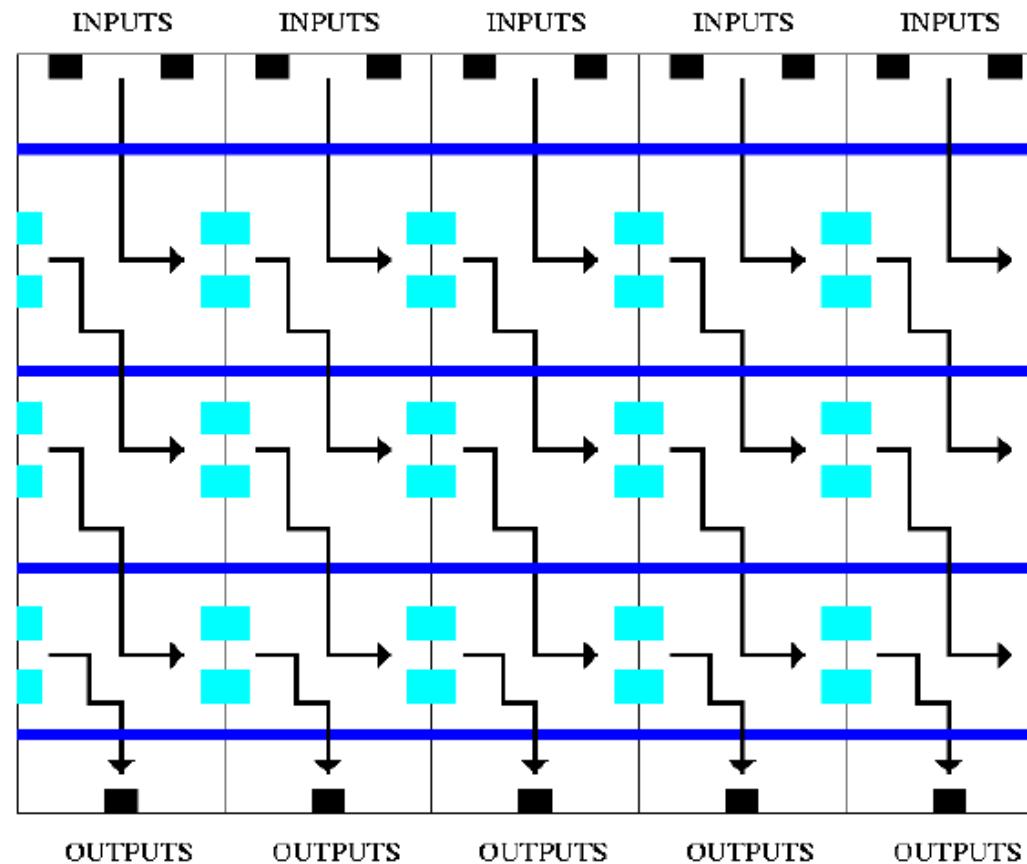
Bit slice design

- We can design a block that implements all the operations for one bit (e.g. in a multi-bit design, as in an adder)
- We have to take into account all input, output and internal connections.
- Putting each cell together generates a regular and dense structure.
- Usual way of designing a processor's datapath (registers + FU + shifters).



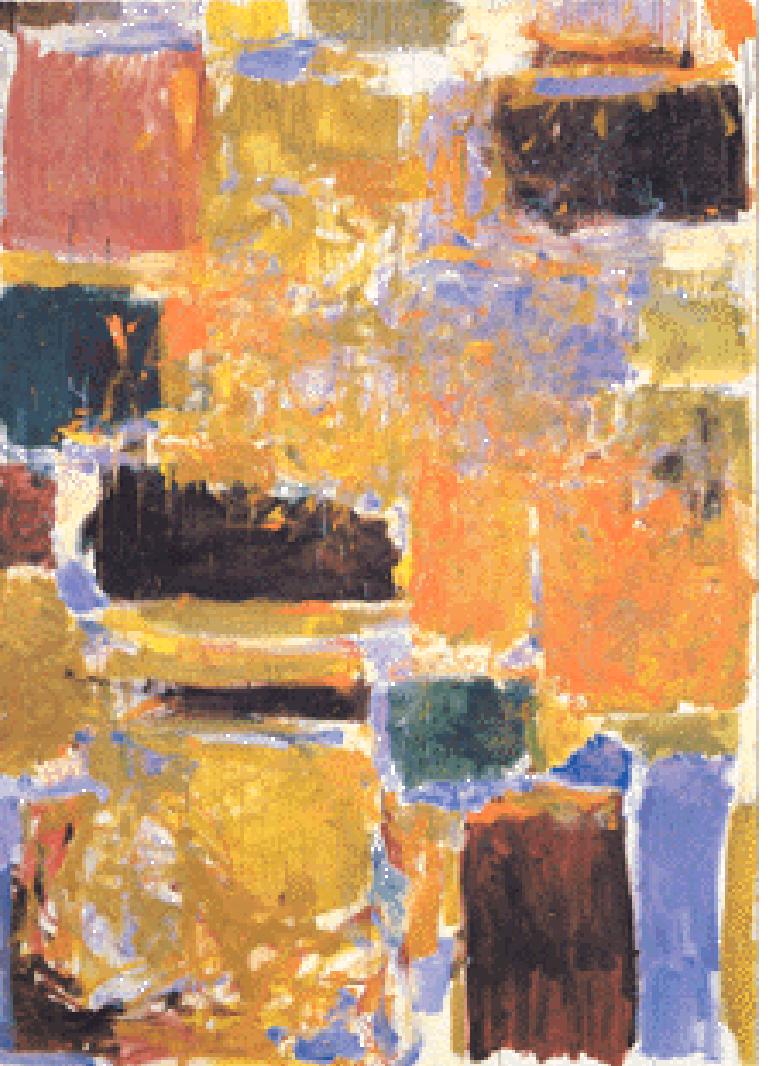
Bit slice design

- Block design from standard 1-bit cells



Conclusions

- Manufacturing ICs is a complex, imperfect and costly process
- Design Rules translate manufacturing/physical limitations to designers
- Design reuse is the norm (i.e. libraries of gates/components/IP)
- Standard cell design is the most common building block.



Design Rules

Problems

- Draw the schematic and the layout of the following gates:
 - $F = \overline{A+B}$
 - $F = \overline{A \cdot B}$
 - $F = \overline{A + B \cdot C}$
 - $F = \overline{A \cdot (B+C)}$