

# LABORATORY 2 : Full-Adder Design

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VLSI .Course 20-21. Fall quadrimester

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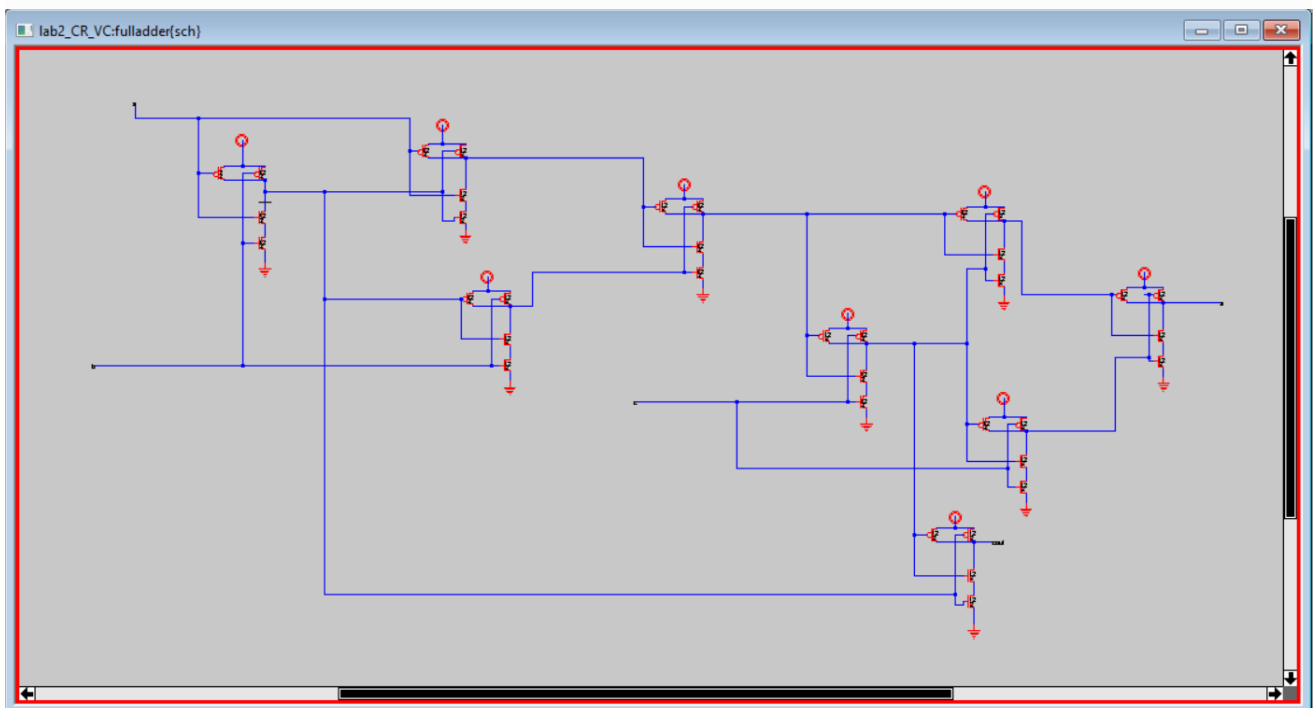
# LAB2: Full-Adder Design

## 1. Hours

We dedicate more or less 4 days. We have problems with Electric and that has delayed us

## 2. Full-Adder Schematic

We make the schematic with 9 NANDS but, we tried with 9 NANDS components and we was problems with NCC (differents number of components). So we have tried with transistors PMOS and CMOS, but we have more problems with NCC and we don't have time. Then this is the result:



We exports 3 inputs (a,b,c) and 2 outputs (cout, s)

## 2.1 Simulation Schematic

In the simulation, all works fine, any warning



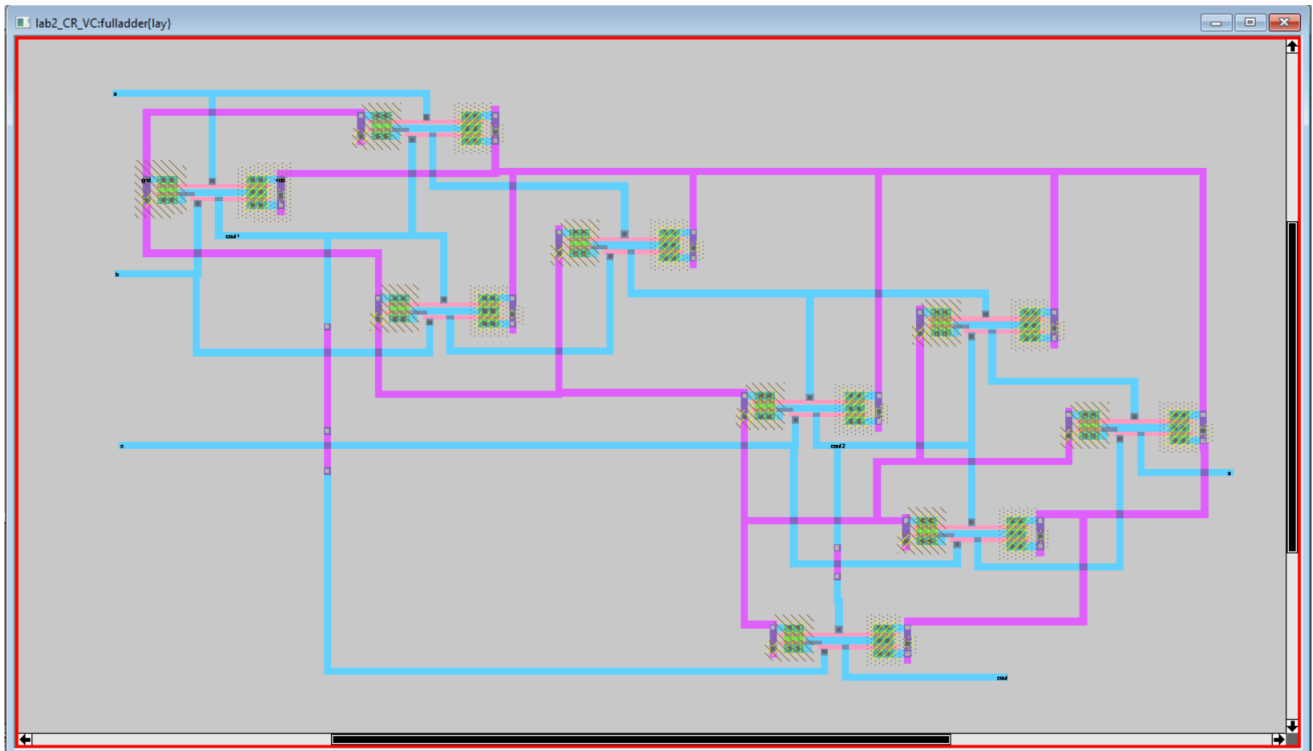
## 3. Fulladder.cmd

```
1 | fulladder.cmd
2 | Written 1/24/02 David_Harris@hmc.edu
3 |
4 | Simulate a full adder for Lab 2.
5 | Note: this file does not check all input combinations.
6 |
7 | 000
8 | a b c
9 | s 2
10 | assert s 0
11 | assert cout 0
12 |
13 | 001
14 | h a
15 | s 2
16 | assert s 1
17 | assert cout 0
18 |
19 | 010
20 | l a
21 | h b
22 | s 2
23 | assert s 1
24 | assert cout 0
25 |
26 | 011
27 | h a
28 | s 2
29 | assert s 0
30 | assert cout 1
31 |
32 |
33 | 100
34 | l b a
35 | h c
```

```
36 | s 2
37 | assert s 1
38 | assert cout 0
39 |
40 |
41 | | 101
42 | h a
43 | s 2
44 | assert s 0
45 | assert cout 1
46 |
47 |
48 | | 110
49 | l a
50 | h b
51 | s 2
52 | assert s 0
53 | assert cout 1
54 |
55 |
56 | | 111
57 | h a
58 | s 2
59 | assert s 1
60 | assert cout 1
```

## 4. Full-Adder Layout

The first option are 9 NANDS as component, (Edit- New Facet Instance), but the simulation didn't work ,so we make a NAND (lab1) and duplicate 8 more. Now the simulation works. We exports 3 inputs (a,b,c) and 2 outputs (cout, s)



## 5. Simulation Layout

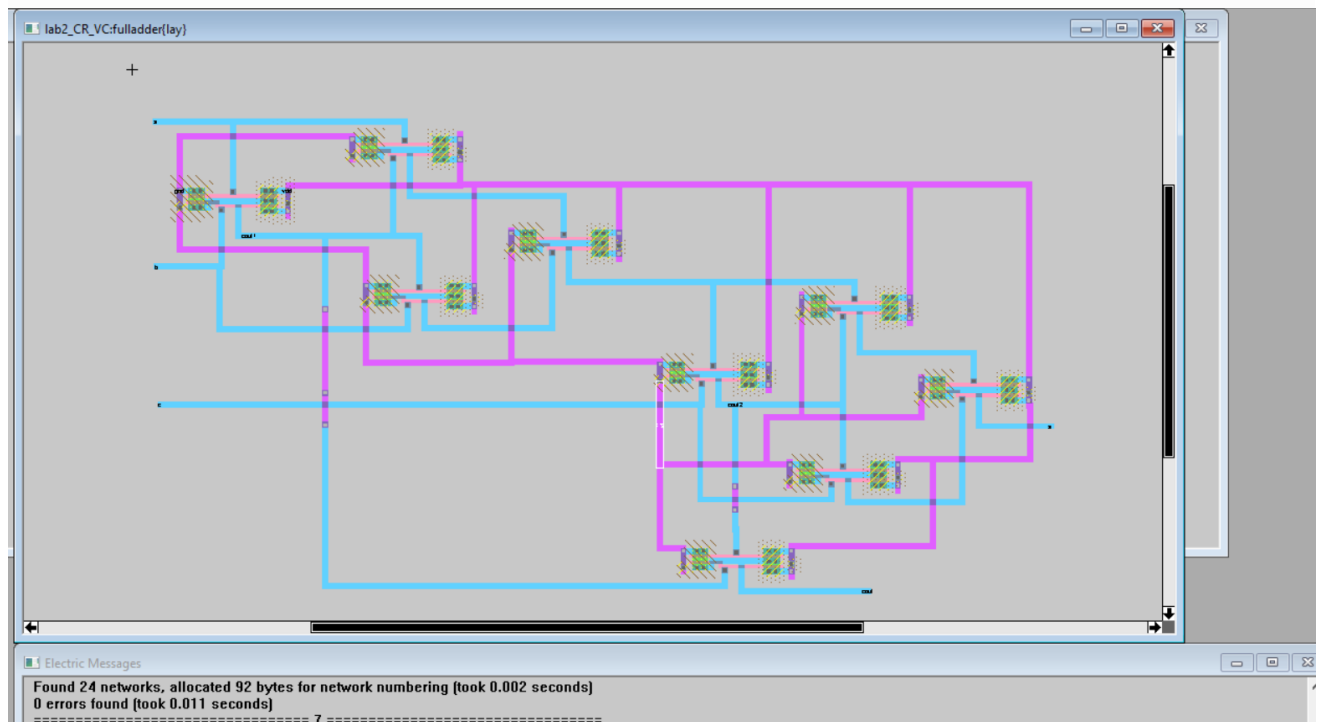
Simulation works, any warning



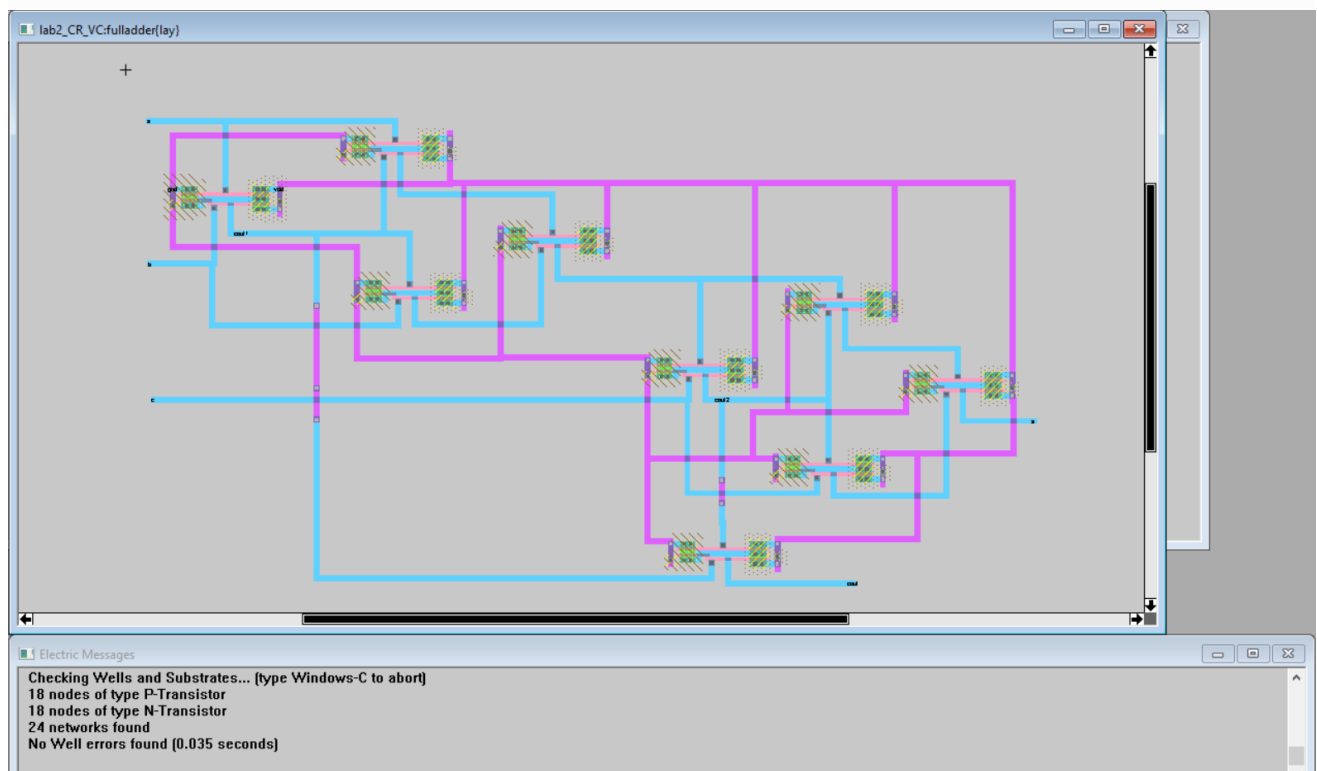
## 6. Verification Status Layout

DRC and ERC pass! The same in the schematic. But like we said, we have had problems with the NCC.

### 6.1 DRC



### 6.2 ERC



## 6.3 NCC

I don't know because we have errors 4 and 5, because we have the same exports names in the two facets, schematic and layout. And the other we don't know how to solve it. And we don't have more time.



```
===== 13 =====
Comparing facet fulladder{sch} with facet fulladder{lay}
- Checking facets recursively; Ignoring Power and Ground nets
- Parallel components not merged; Series transistors not merged
- Checking export names and component sizes
- No facet overrides
Extracting networks from fulladder{sch}...
Extracting networks from fulladder{lay}...
Both facets have 36 components
Both facets have 21 nets
***** Found 5 Export and Structural differences! (0.014 seconds)
To review errors, type:
> Show the next error
< Show the previous error
===== 14 =====
NCC error 5 of 5: Export names 'fulladder{sch}:c' and 'fulladder{lay}:a' do not match
===== 15 =====
NCC error 4 of 5: Export names 'fulladder{sch}:a' and 'fulladder{lay}:c' do not match
===== 16 =====
NCC error 3 of 5: Unassociated networks: from facet fulladder{sch}: b (4 connections), net100 (2 connections), net85 (2 connections), net70 (2 connections), net61 (2 connections), net113 (2 connections), net39 (5 connections), net90 (5 connections), net42 (5 connections), net64 (7 connections); from facet fulladder{lay}: b (4 connections), net15 (2 connections), net14 (2 connections), net12 (2 connections), net11 (2 connections), net1 (2 connections), net4 (5 connections), net6 (5 connections), net7 (5 connections), net10 (7 connections)
===== 17 =====
NCC error 2 of 5: Unassociated nodes
===== 18 =====
NCC error 1 of 5: Unassociated nodes
```