LABORATORY 2 : Full-Adder Design

VLSI .Course 20-21. Fall quadrimester

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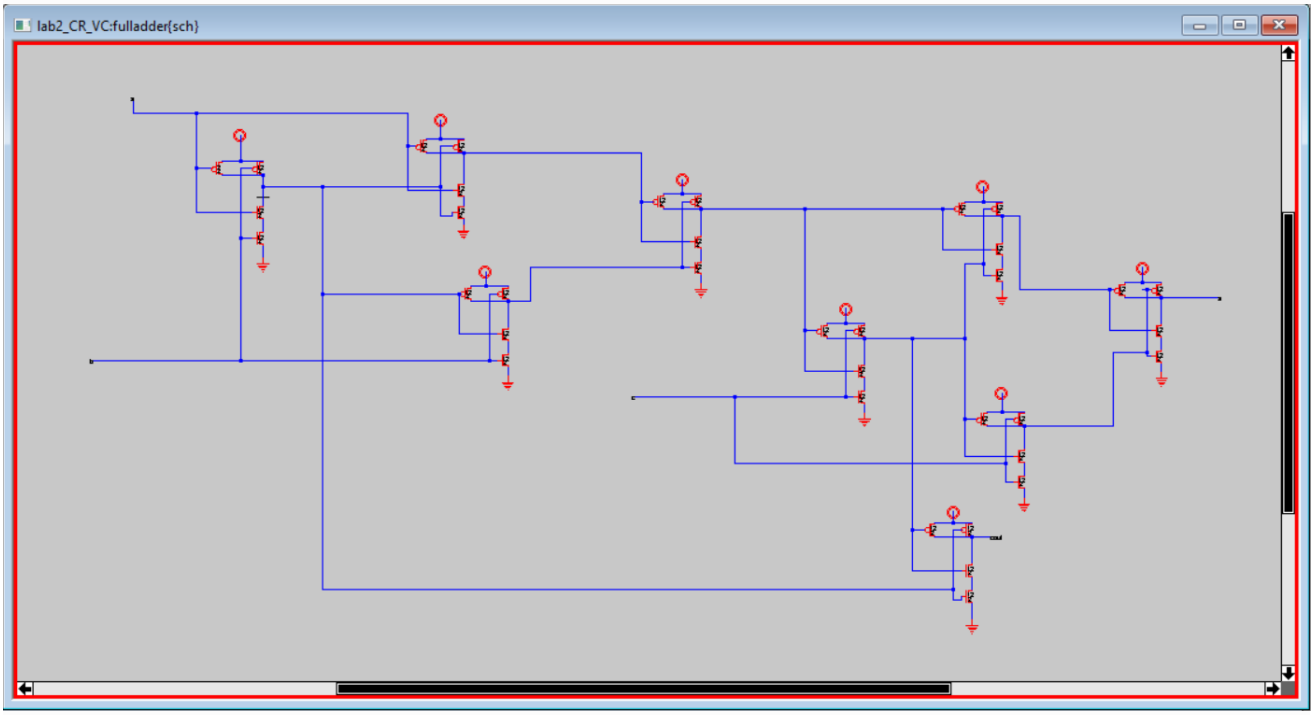
LAB2: Full-Adder Design

1. Hours

We dedicate more or less 4 days. We have problems with Electric and that has delayed us

2. Full-Adder Schematic

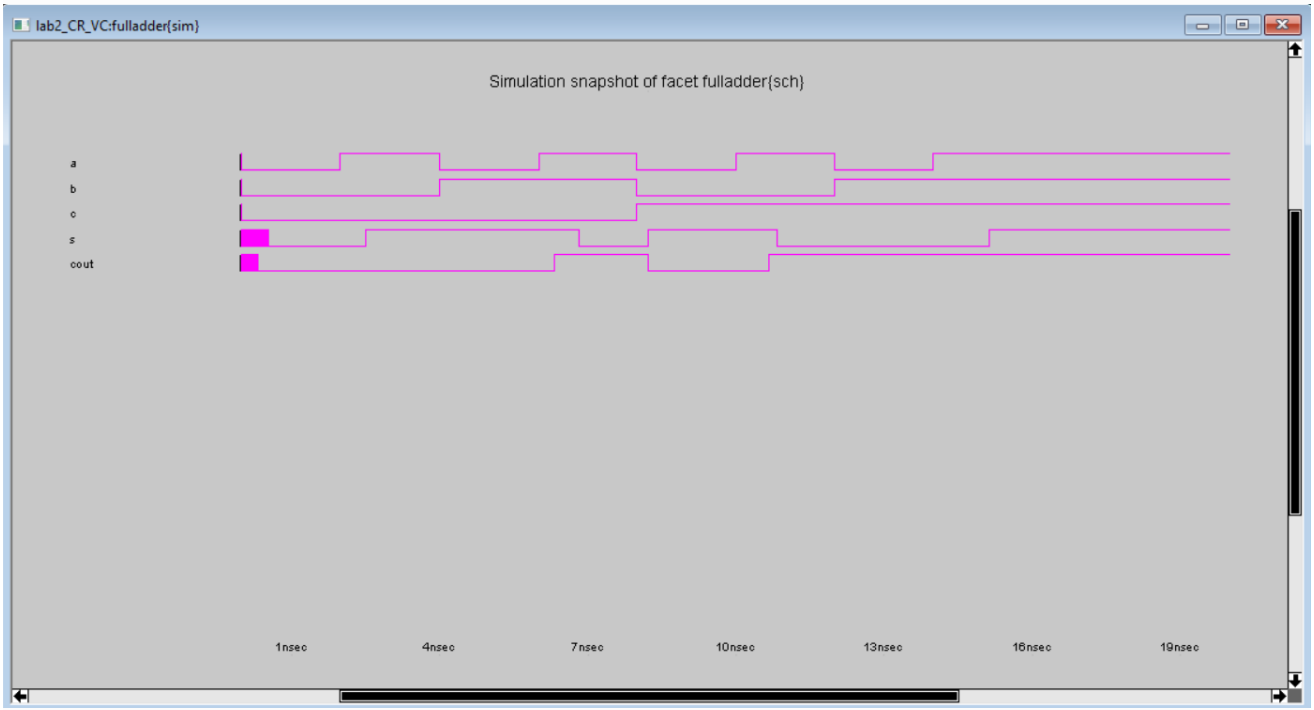
We make the schematic with 9 NANDS but, we tried with 9 NANDS components and we was problems with NCC (differents number of components). So we have tried with transistors PMOS and CMOS, but we have more problems with NCC and we don't have time. Then this is the result:



We exports 3 inputs (a,b,c) and 2 outputs (cout, s)

2.1 Simulation Schematic

In the simulation, all works fine, any warning



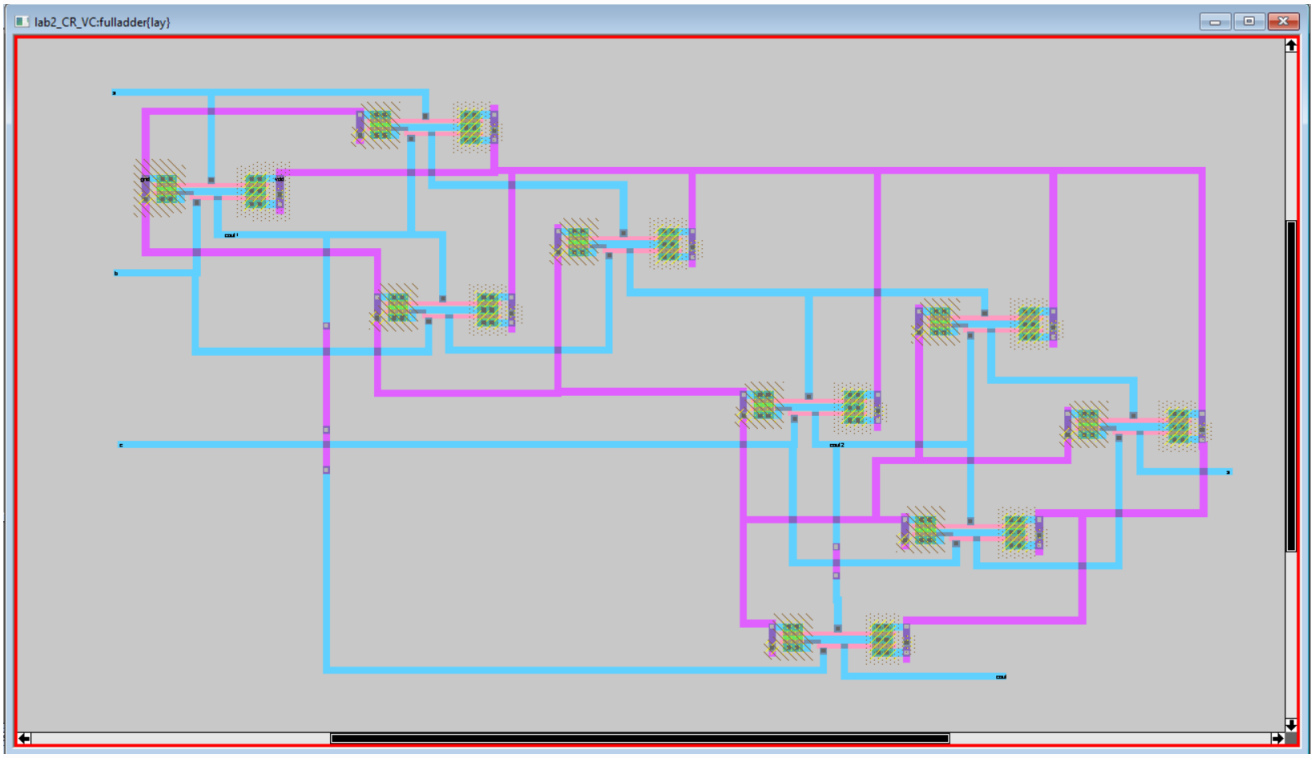
3. Fulladder.cmd

```
| fulladder.cmd
| Written 1/24/02 David_Harris@hmc.edu
|
| Simulate a full adder for Lab 2.
|  Note: this file does not check all input combinations.

| 000
l a b c
s 2
assert s 0
assert cout 0

| 001
h a
s 2
assert s 1
assert cout 0

| 010
l a
h b
s 2
assert s 1
assert cout 0

| 011
h a
s 2
assert s 0
assert cout 1


| 100
l b a
h c
```

```
s 2
assert s 1
assert cout 0


| 101
h a
s 2
assert s 0
assert cout 1


| 110
l a
h b
s 2
assert s 0
assert cout 1


| 111
h a
s 2
assert s 1
assert cout 1
```

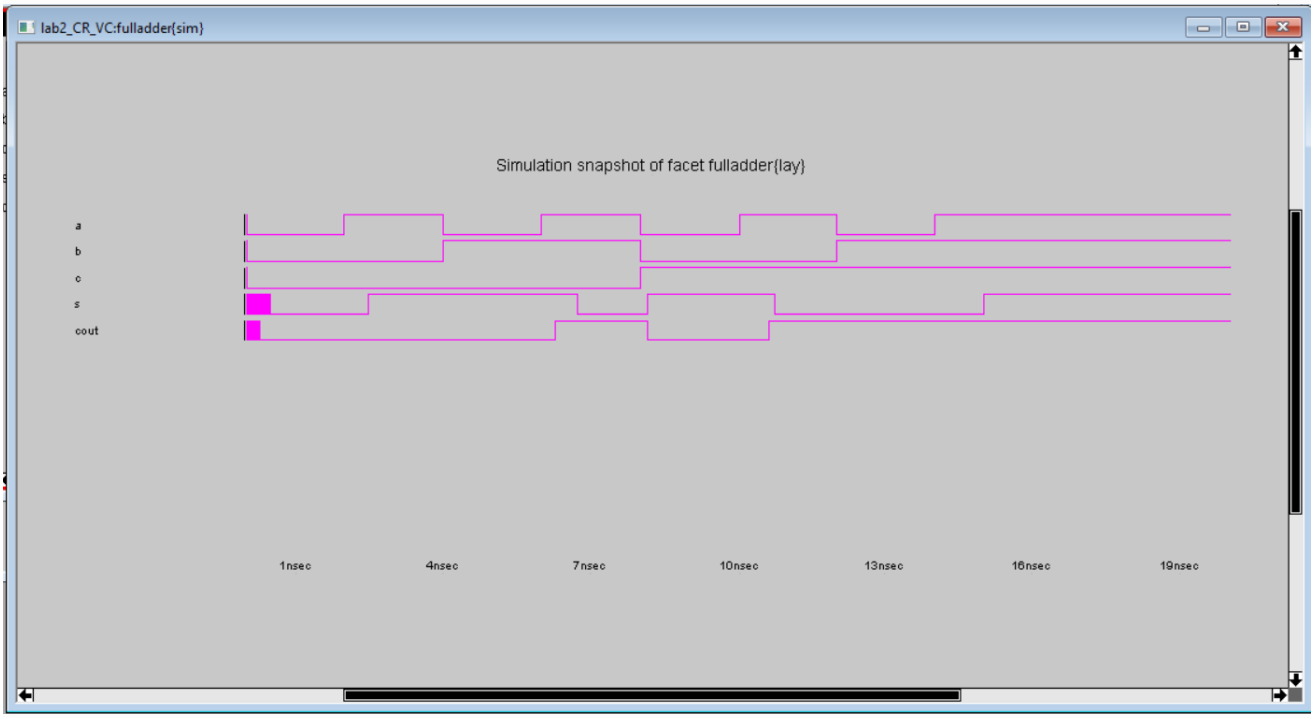
4. Full-Adder Layout

The first option are 9 NANDS as component, (Edit- New Facet Instance), but the simulation didn't work ,so we make a NAND (lab1) and duplicate 8 more. Now the simulation works. We exports 3 inputs (a,b,c) and 2 outputs (cout, s)



5. Simulation Layout

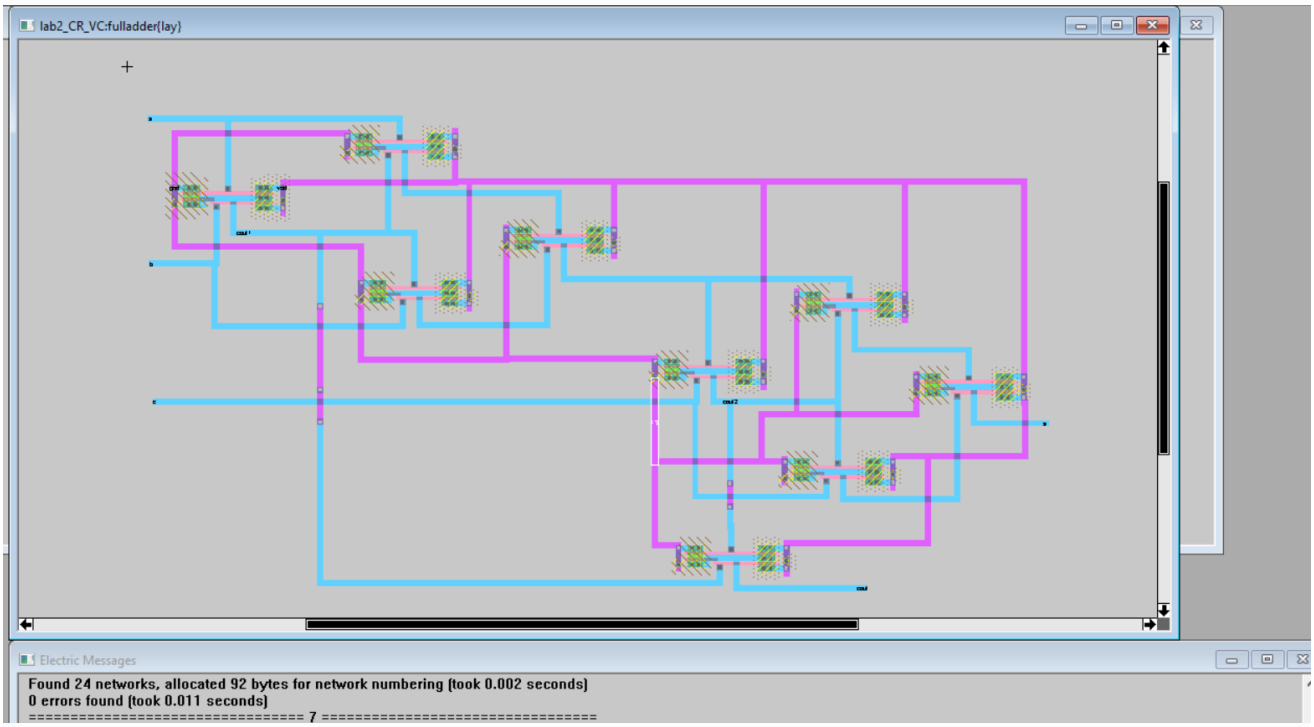
Simulation works, any warning



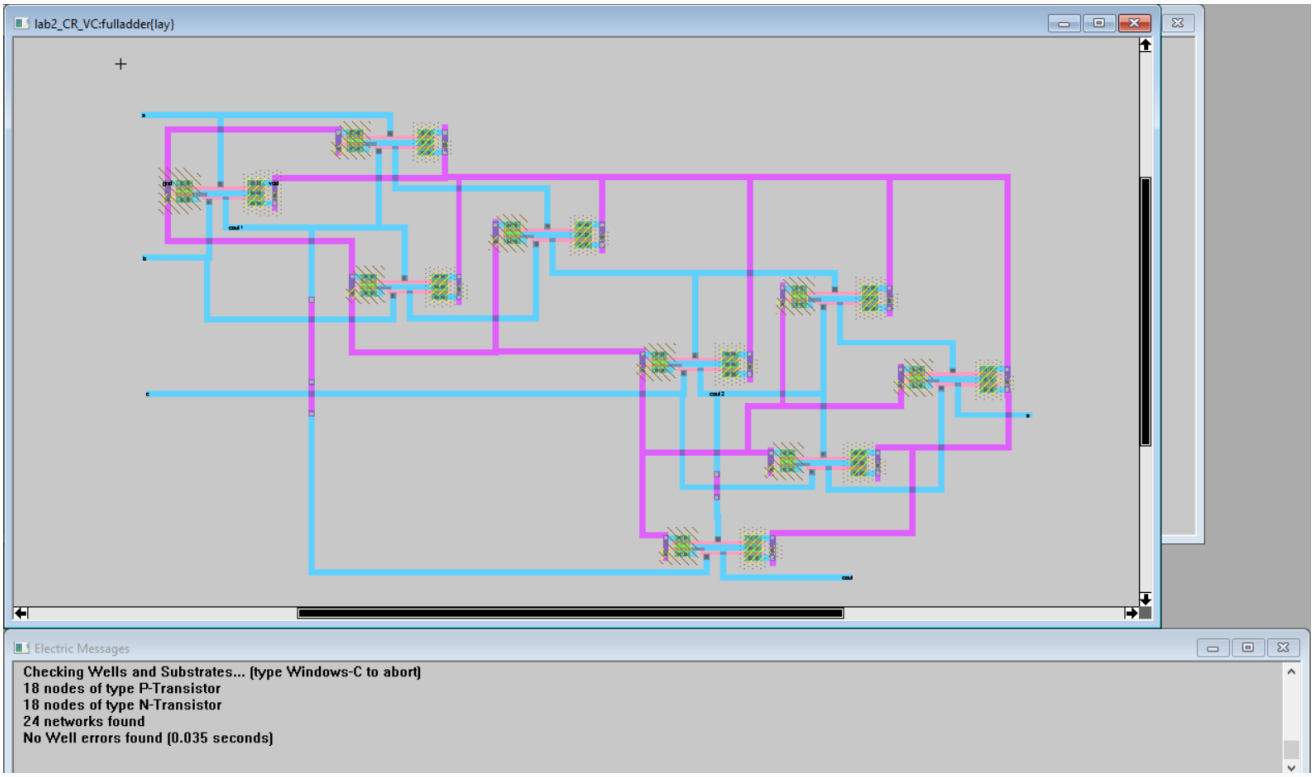
6. Verification Status Layout

DRC and ERC pass! The same in the schematic. But like we said, we have had problems with the NCC.

6.1 DRC



6.2 ERC



6.3 NCC

I don't know because we have errors 4 and 5, because we have the same exports names in the two facets, schematic and layout. And the other we don't know how to solve it. And we don't have more time.