

VIVADO



X-Tech

Presented by Xilinx and Avnet

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XILINX® 7 SERIES FEATURE OVERVIEW

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AGENDA

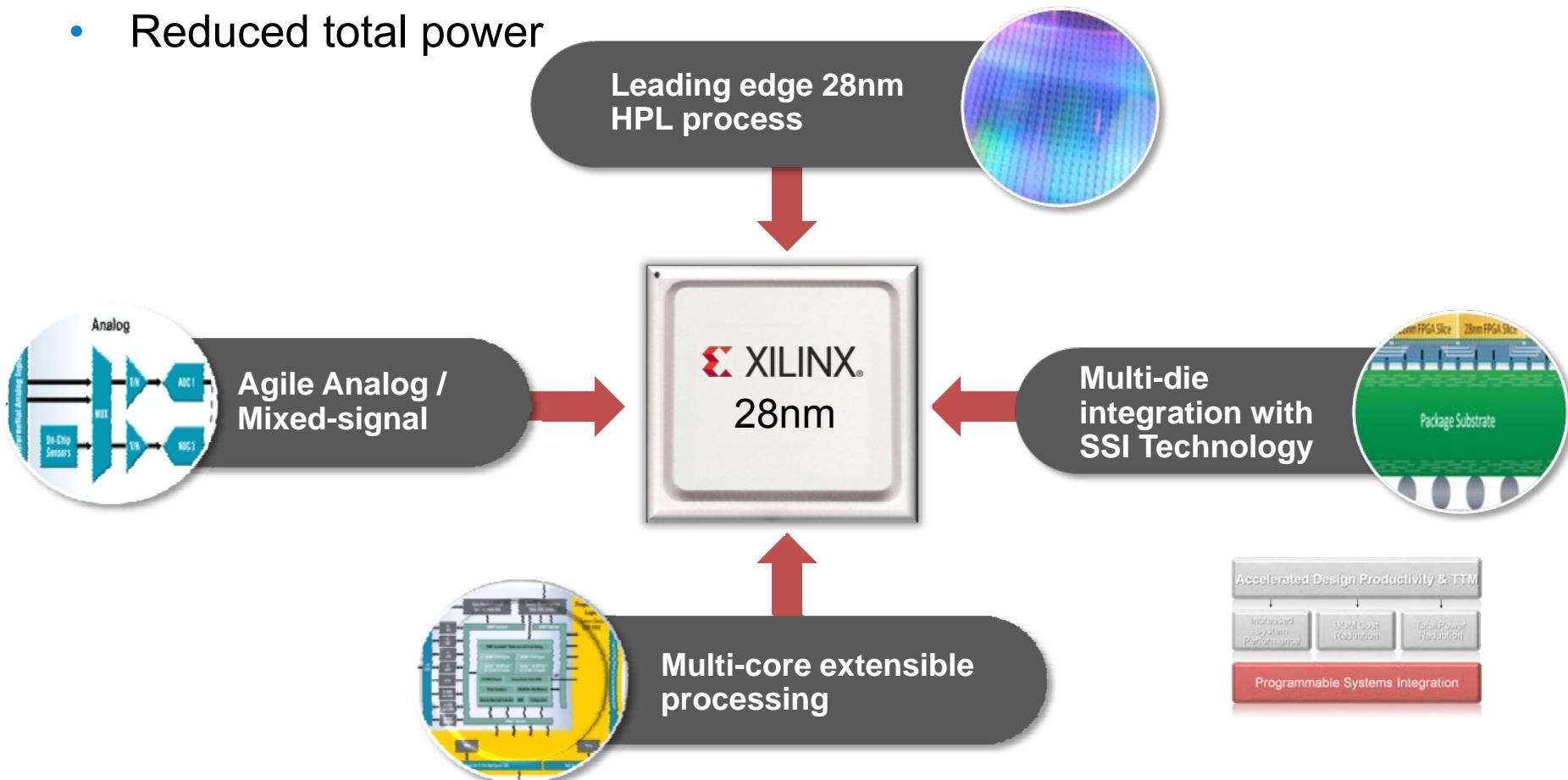
- 7 Series Introduction
- Power Reduction
- Performance
 - > CLB and Embedded Memory
 - > Clocking
 - > I/O
 - > High Speed Memory Interfacing
 - > High Speed Serial Transceivers
 - > PCI Express® Interface
 - > DSP
- Productivity
 - > Agile Mixed Signal (AMS) / XADC
- 7 Series Leadership Summary

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FOUR UNIQUE SYSTEMS INTEGRATION TECHNOLOGIES

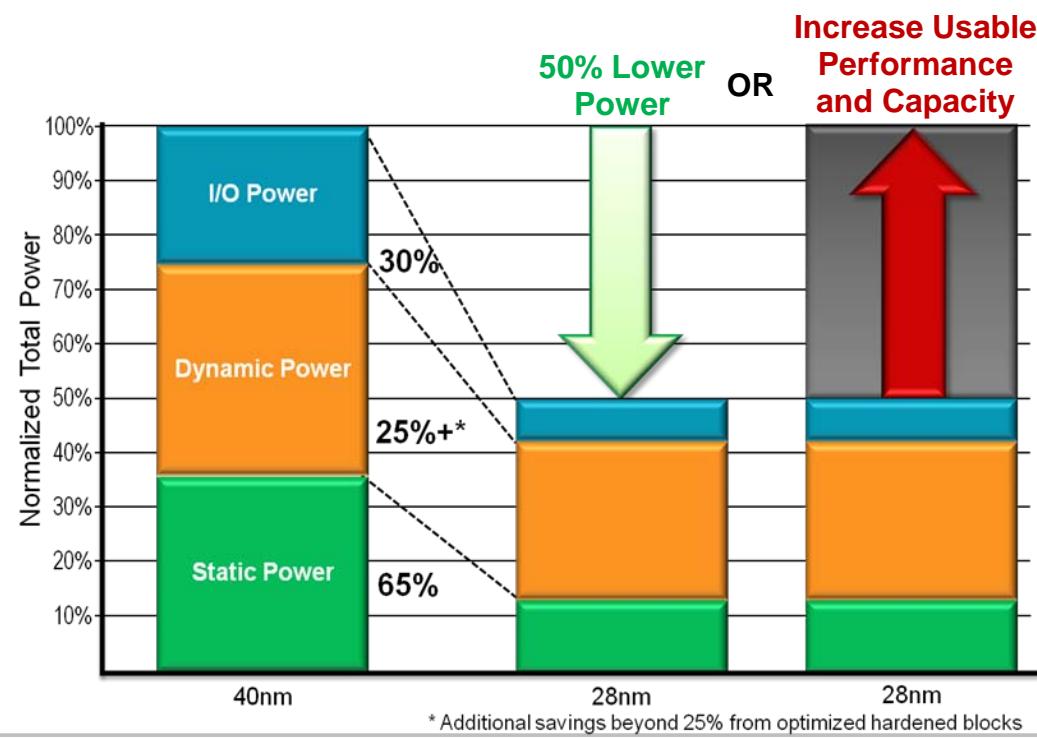
- Increased system-level performance
- Reduced BOM cost
- Reduced total power



7 SERIES LOWER POWER DIFFERENTIATION

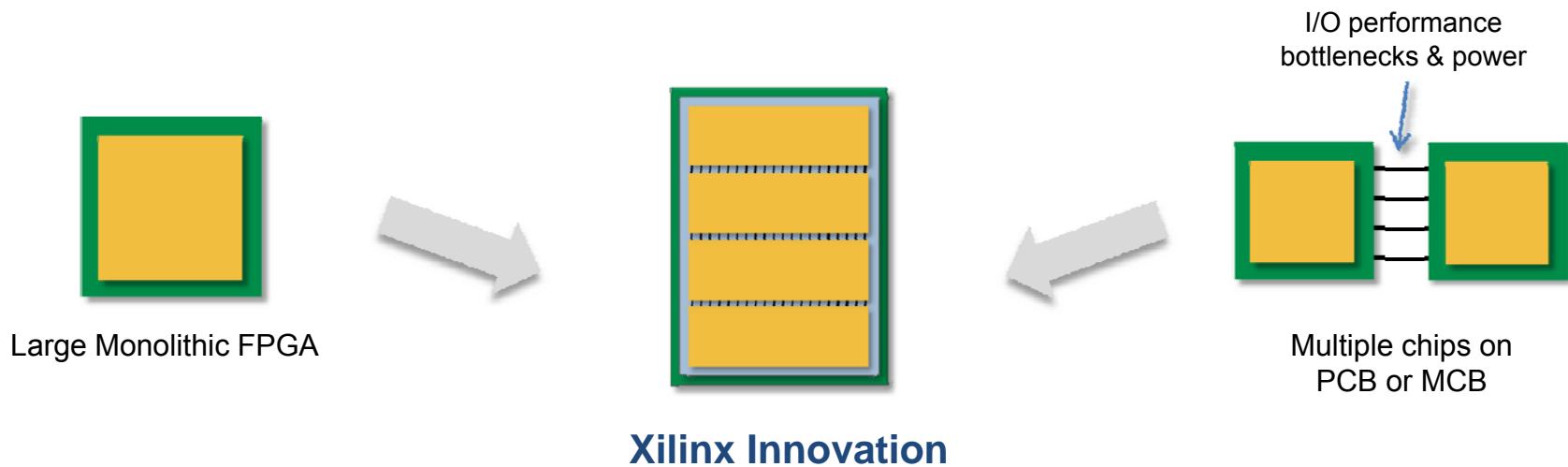
THE POWER CHALLENGE

- 50% Lower Total Power
 - > 65% lower static power enabled by low-power process
 - > 25%+ lower dynamic power via architectural evolution
 - > 30% lower I/O power with enhanced capability
- System Design Flexibility
 - > 50% lower power budget
 - OR**
 - > Take advantage of additional usable performance and capacity at the previous power budget



INTRODUCING STACKED SILICON INTERCONNECT TECHNOLOGY

HIGH BANDWIDTH, LOW LATENCY, LOW POWER



- ✓ Massive number of low latency, die-to-die connections
- ✓ Earlier in time
- ✓ No wasted I/O power
- ✓ Over five years of R&D

Delivers the Best of Both Worlds: High and Usable Capacity

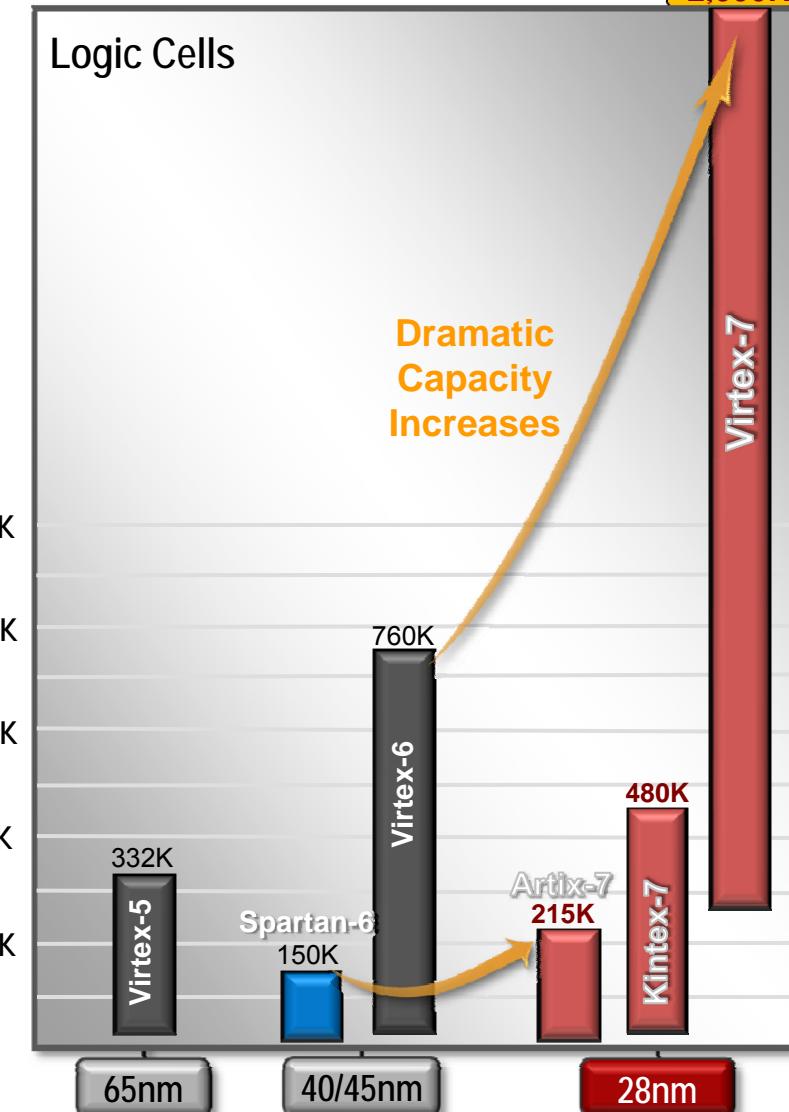
GROUND BREAKING CAPACITY GAINS AT 28NM

WORLD'S FIRST 2 MILLION LOGIC CELL FPGA

- Over 2x capacity increases over Spartan-6 and Virtex-6 FPGAs

Family	Capacity Range
ARTIX. ⁷	16K – 215K LCs
KINTEX. ⁷	70K – 480K LCs
VIRTEX. ⁷	330K – 2M LCs

- 16K – 2M LCs; the widest capacity range offered in a single unified product family
- Larger densities enable higher performance
 - > More calculations/clock cycle by utilizing parallelism inherent in FPGAs



BREAKTHROUGH POWER, PERFORMANCE & PRODUCTIVITY

ARTIX⁷

KINTEX⁷

VIRTEX⁷

Maximum Capability	Lowest Power and Cost	Industry's Best Price-Performance	Industry's Highest System Performance
Logic Cell Range	16K – 215K	70K – 480K	330K – 2,000K
Block RAM	13 Mb	34 Mb	68 Mb
DSP Slices	740	1,920	3,600
Peak DSP Perf. (symmetrical FIR)	929 GMACS	2,845 GMACs	5,335 GMACS
Transceivers	16	32	96
Transceiver Performance	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s, 13.1 Gb/s, 28.05 Gb/s
Memory Performance	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
PCIe Interface	Gen2x4	Gen2x8	Gen3x8
I/O Pins	500	500	1,200
I/O Voltages	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V

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SCALABLE OPTIMIZED ARCHITECTURE ADVANTAGE

- Common elements enable easy IP reuse for quick design portability across all 7 series families
 - > Design scalability from low-cost to high-performance
 - > Expanded eco-system support
 - > Quickest Time To Market (TTM)



Logic Fabric
LUT-6 CLB



On-Chip Memory
36Kbit/18Kbit Block RAM



DSP Engines
DSP48E1 Slices



Hi-performance Serial I/O Connectivity
Transceiver Technology



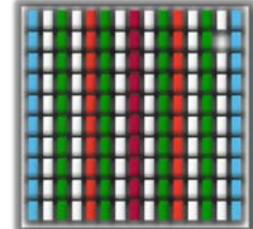
Precise, Low Jitter Clocking
MMCMs



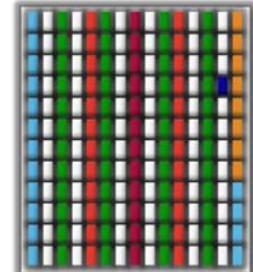
Enhanced Connectivity
PCIe® Interface Blocks



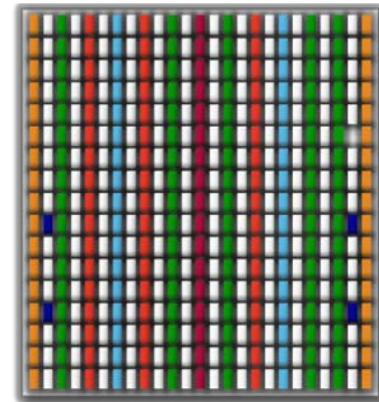
Hi-perf. Parallel I/O Connectivity
SelectIO™ Technology



Artix™-7 FPGA



Kintex™-7 FPGA



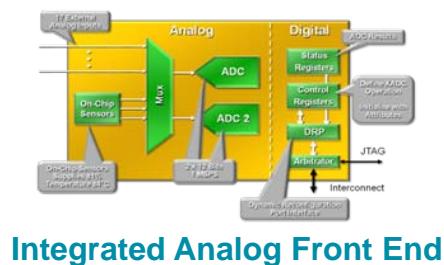
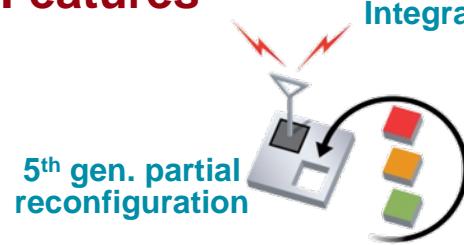
Virtex®-7 FPGA

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7 SERIES POWER EFFICIENCY FOCUS FROM EVERY ANGLE

Additional Power Saving Features

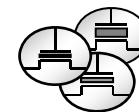


Fine grain clock and logic gating

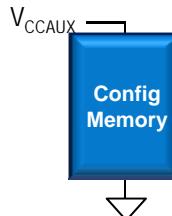
Lower device core voltage



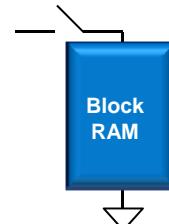
High performance,
low power process



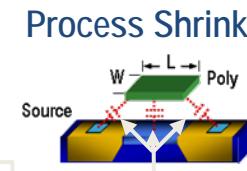
Reducing
Static Power



Reduced from
2.5V to 1.8V

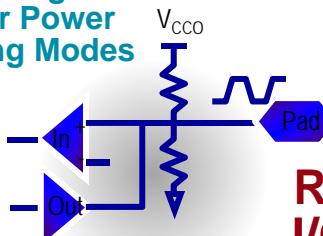


Unused Block RAM
Power Savings



IO Design &
User Power
Saving Modes

Optimized Hard
Blocks



Reducing
I/O Power

STATIC POWER REDUCTION TECHNIQUES

Process

- Xilinx requested a Process with 50% less leakage than std. 28nm HP process
 - > TSMC delivered with 28nm Low Power High-K Metal Gate process with individual blocks power drop by 40 – 80% (HPL)

Design

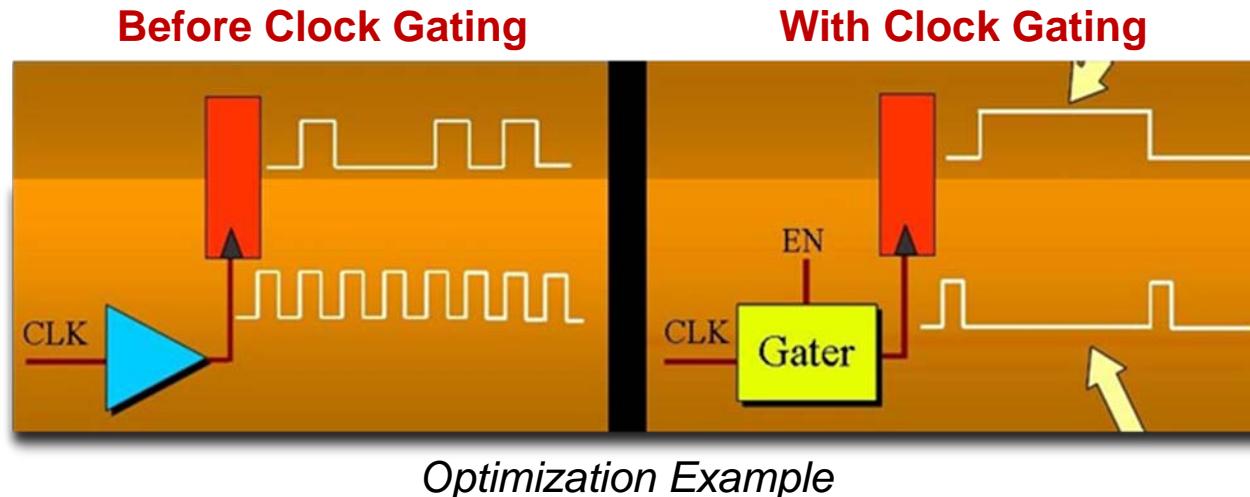
- Judicious transistor choice per block – improved over Virtex®-6 FPGAs
 - > Adjust threshold voltage and gate length/width to optimize performance/leakage
- Voltage scaling option (-2L) for instant 30% reduction
- Reduced V_{CCAUX} to 1.8V from 2.5V
 - > Used for Configuration memory, PLL, IDELAY

Architecture

- Power Gate unused blocks
- Partial Reconfiguration technology for 30%+ static power reduction
 - > Improved ease-of-use for mainstream designs
 - > Support for all 7 series FPGAs

SIGNIFICANT DYNAMIC POWER REDUCTION WITH INTELLIGENT CLOCK GATING

- Fine-grain Clock Gating eliminates unnecessary clock activity while maintaining functionality and performance
 - > Power = $\alpha \times f_{clk} \times C_L \times V^2$
 - > Clock and Logic Gating reduces switching activity α
- Up to 25% Dynamic power reduction
 - > Synthesis independent logic reorganization

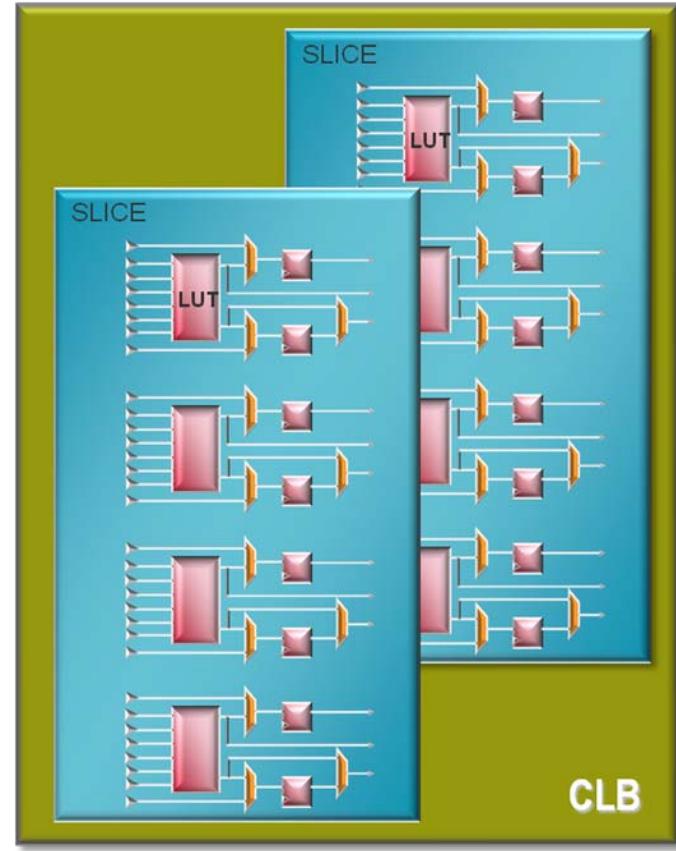


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CONFIGURABLE LOGIC BLOCK

- Architecture consistent with Virtex-6 and Spartan-6 FPGAs
 - > Two side-by-side slices per CLB
 - > Four 6-input Look Up Tables (LUTs) per slice
 - > Two flip-flops per LUT
 - > MUX7 and MUX8 for creating larger logic structures
- Ease of design migration
 - > Designs can migrate easily from Spartan-6 and Virtex-6 to 7 series FPGAs
 - > Designs can migrate between 7 series families as user's requirements change



Highly capable logic structure with easy migration enhancing Productivity

DISTRIBUTED RAM

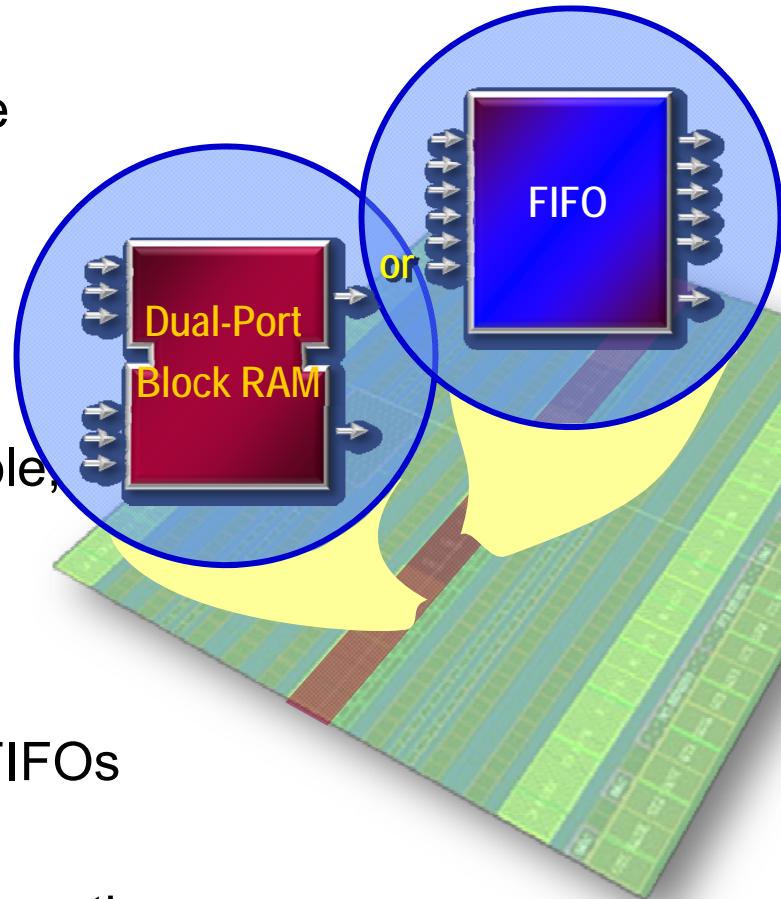
- Distributed LUT memory
 - > Each LUT can be 64-bit memory
 - > Inherently single-port, but can be made dual-port, multi-port
- Ideal for small and fast memories
 - > Coefficient storage
 - > Small data buffers
 - > Small state machines
 - > Small FIFOs
 - > Shift registers ...
- Adjacent LUTs can be cascaded
 - > Up to 256x1-bit single port memory or 64x1bit quad port memory in a single slice

Capability of single SLICE_M			
Single Port	Dual Port	Simple Dual Port	Quad Port
32x2	32x2D	32x6SDP	32x2Q
32x4	32x4D	64x3SDP	64x1Q
32x6	64x1D		
32x8	64x2D		
64x1	128x1D		
64x2			
64x3			
64x4			
128x1			
128x2			
256x1			

Fine-grained distributed memory is intimately coupled to the logic

36KBIT BLOCK RAM

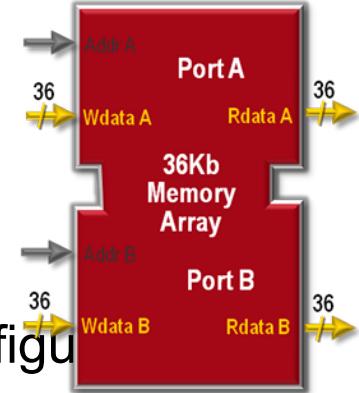
- 36K/18K Block RAM
 - > All 7 series FPGA families use same Block RAM as Virtex-6 FPGAs
- Two independent ports address common data
 - > Individual address, clock, write enable, clock enable
 - > Independent widths for each port
- Integrated control for fast and efficient FIFOs
- Integrated 64 / 72-bit Hamming error correction



Each RAM block can be configured as Block RAM or FIFO

FLEXIBLE BLOCK RAM CONFIGURATIONS

- All 7 series 36K/18K Block RAM consistent with Virtex-6 FPGAs for Easy Migration
 - > 32Kx1 to 512x72 in one 36K Block RAM
 - > 16Kx1 to 512x36 in one 18K Block RAM
 - > Single-port, Simple Dual-port and True Dual-port config
 - > Integrated cascade logic creates 64Kx1 from two 32Kx1 Block RAM
 - > Byte-write enable



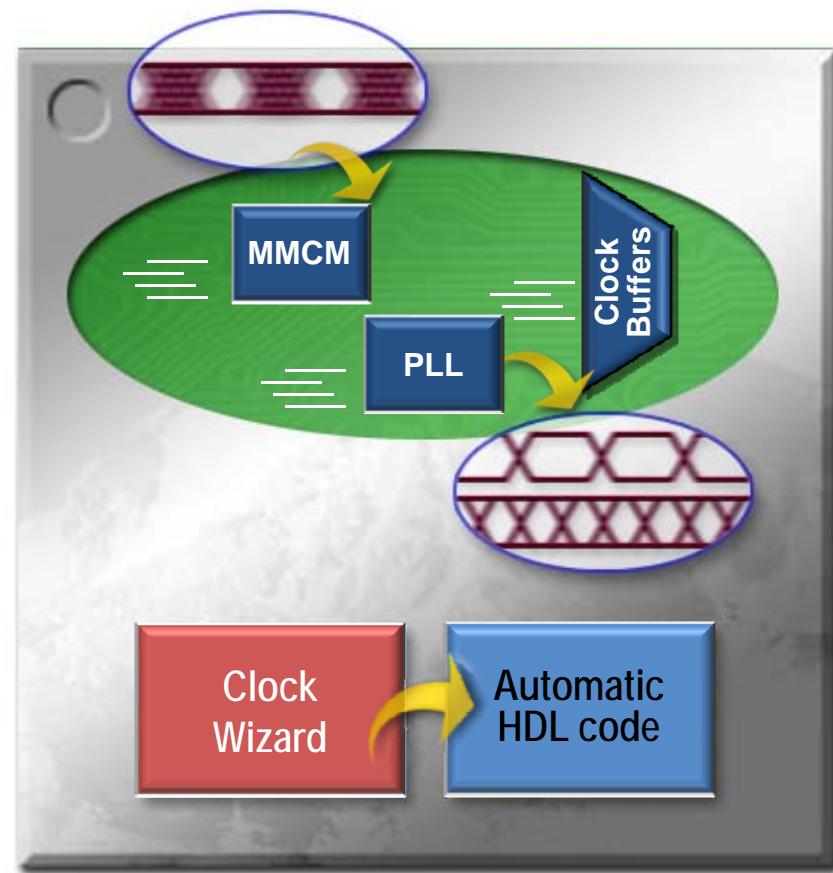
Wide Variety of Configurations for Flexibility			
	Each 18K	Each 36K	Comments
True Dual-port	16Kx1, 8Kx2, 4Kx4, 2Kx9, 1Kx18	32Kx1, 16Kx2, 8Kx4, 4Kx9, 2Kx18, 1Kx36	▪ Two fully independent read and write operations
Simple Dual-port	16Kx1, 8Kx2, 4Kx4, 2Kx9, 1Kx18, 512x36	16Kx2, 8Kx4, 4Kx9, 2Kx18, 1Kx36, 512x72	▪ 1 read & 1 write port ▪ Read AND write in 1 cycle
Single-port	16Kx1, 8Kx2, 4Kx4, 2Kx9, 1Kx18, 512x36	16Kx2, 8Kx4, 4Kx9, 2Kx18, 1Kx36, 512x72	▪ 1 read & 1 write port ▪ Read OR write in 1 cycle

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7 SERIES ADDRESSES HIGH PERFORMANCE CLOCKING CHALLENGES

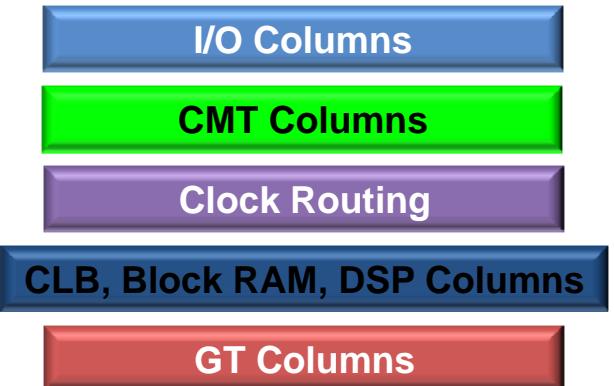
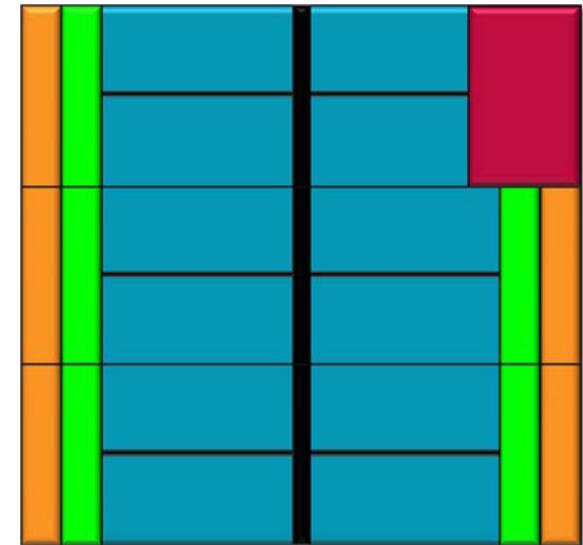
- Based on established Virtex-6 FPGA clocking structure
 - > Same Scalable Optimized Architecture in all 7 series
- Low-skew clock distribution
 - > Combination of paths for driving clock signals to and from different locations
- Clock buffers
 - > High fanout buffers for connecting clock signals to the various routing resources
- Clock regions
 - > Device divided into clock regions with dedicated resources
- Clock Management Tile (CMT)
 - > One MMCM and one PLL per CMT
 - > Up to 24 CMTs per device
- Easy-to-use software
 - > Fast and simple access to the circuitry



Powerful Clocking Solutions

7 SERIES FPGA LAYOUT

- Similar Floorplan to Virtex-6 FPGAs
 - Provides easy migration to 7 series FPGAs
- CMT columns moved from center of device to adjacent to I/O columns
 - No more inner vs. outer column performance difference
 - Support for higher performance interfaces
- Only one I/O column per half device
 - Uniform skew from center of device
- GT columns replace I/O and CMT in smaller devices
 - > GT columns not always present

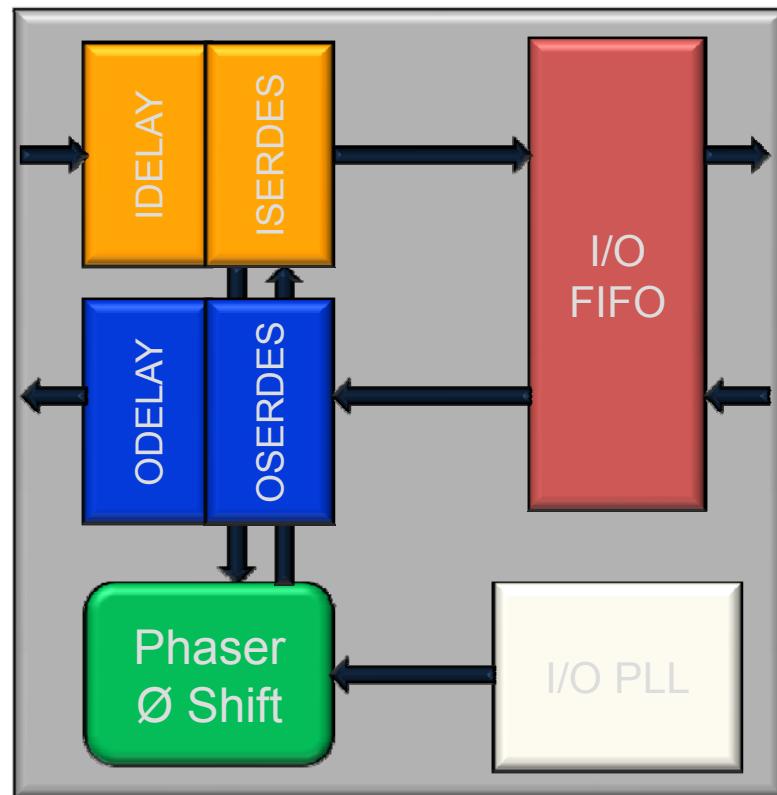


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7 SERIES ADDRESSES THE I/O CHALLENGES

- Two distinct I/O types that extend Virtex-6 FPGA I/O
 - > High performance and high range I/O
 - > Application targeted mix of I/O types across 7 series families
 - > More power controllable features
- Extension of logic layer functionality
 - > Wider input/output SERDES
 - > Addition of independent ODELAY
- New hardware blocks to address highest I/O performance
 - > Phaser, I/O FIFO and I/O PLL
 - > Grouping of these new I/O blocks



7 SERIES I/O BANKS

	Spartan-6 FPGA	Virtex-6 FPGA	7 Series FPGA
I/O Bank Size	30 ~ 83 I/O per	40 I/O Per	50 I/O Per
Clock Capable I/O per Bank	8 Clocks per bank	4 Diff or 8 SE	4 Diff or 8 SE
DQS Specific I/O Per Bank	NA	Shared with CCIO	4 Diff Pairs

Special Designation	I/O Type	I/O Number
select_io	Single Ended	VRP
select_io		SE
select_io		P
select_io		N
select_io		P
select_io		N
select_io		45
select_io		DQSCC-P
select_io		P
select_io		DQSCC-N
select_io		N
select_io		P
select_io	Group D 12 IOs	N
select_io		41
select_io		P
select_io		40
select_io		N
select_io		39
select_io		P
select_io		38
select_io		N
select_io		37
select_io		P
select_io		36
select_io	Group C 12 IOs	N
select_io		35
select_io		P
select_io		34
select_io		N
select_io		33
select_io		DQSCC-P
select_io		P
select_io		DQSCC-N
select_io		N
select_io		P
select_io		30
select_io	Group B 12 IOs	N
select_io		29
select_io		CCIO-P
select_io		P
select_io		CCIO-N
select_io		N
select_io		27
select_io		CCIO-P
select_io		P
select_io		26
select_io		CCIO-N
select_io		N
select_io	Group A 12 IOs	25
select_io		CCIO-P
select_io		P
select_io		CCIO-N
select_io		N
select_io		23
select_io		CCIO-P
select_io		P
select_io		CCIO-N
select_io		N
select_io		22
select_io		DQSCC-P
select_io	Single Ended	P
select_io		20
select_io		DQSCC-N
select_io		N
select_io		19
select_io		P
select_io		18
select_io		N
select_io		17
select_io		P
select_io		16
select_io		N
select_io		15
select_io		P
select_io		14
select_io		N
select_io		13
select_io		P
select_io		12
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select_io		10
select_io		N
select_io		9
select_io		DQSCC-P
select_io		P
select_io		DQSCC-N
select_io		N
select_io		7
select_io		P
select_io		6
select_io		N
select_io		5
select_io		P
select_io		4
select_io		N
select_io		3
select_io		P
select_io		2
select_io		N
select_io		1
select_io		VRN
select_io		SE
select_io		0

50 I/O Banks with 4x12 pin for high performance memory interface construction

7 SERIES I/O VOLTAGE SUPPORT

- Why are there 2 different I/O types in the 7 Series
 - > 3.3V I/O banks: Used for legacy and broadest application interface support
 - ◆ For High Volume Artix-7, Kintex-7, and low I/O count portion of Virtex-7 FPGAs
 - ◆ Consumer, Broadcast, ISM, Wireless, Wired, A&D applications
 - > 1.8V I/O banks: Used for the highest performance DDR and LVDS interfaces
 - > For High End Kintex-7 and Virtex-7 FPGA applications
 - ◆ Higher End Broadcast, Wired, Wireless, A&D

	I/O Voltage Range	Spartan-6 FPGAs	Virtex-6 FPGAs	Artix-7 FPGAs	Kintex-7 FPGAs	Virtex-7 T Devices	Virtex-7 XT Devices
3.3V I/O Bank HR (High Range)	$V_{CCO} \leq 3.3V$	✓	Up to 2.5V	✓	✓	✓ ¹	
1.8V I/O Bank HP (High Performance)	$V_{CCO} \leq 1.8V$					✓ ²	✓

¹ Up to 100 3.3V I/O in the Virtex-7 count parts

² Up to 150 1.8V I/O in the Kintex-7 parts

Two I/O Bank types provide best match between applications and product family

I/O VOLTAGE SUPPORT AND STANDARDS IN 3.3V I/O HIGH RANGE BANKS

I/O Standard	3.3V	2.5V	1.8V	1.5V	1.2V
LVCMOS	LVCMOS33 (up to 8mA)	LVCMOS25 (up to 8mA)	LVCMOS18 (up to 24mA)	LVCMOS15 (up to 24mA)	LVCMOS12* (up to 12mA)
LVDS	TMDS	LVDS Mini LVDS PPDS RSDS* (pt-to-pt)			
PCI	PCI				
SSTL			SSTL18_I SSTL18_II DIFF_SSTL18_I DIFF_SSTL18_II	SSTL15 DIFF_SSTL15	
HSTL			HSTL_I_18	HSTL_I HSTL_II DIFF_HSTL_I	

*NO DCI support in 3.3V I/O banks
LVDS inputs must have a common mode <= 1.8V

Widest I/O Standard Support for High Volume and Some High End Applications

I/O VOLTAGE SUPPORT AND STANDARDS IN 1.8V I/O HIGH PERFORMANCE BANKS

I/O Standard	1.8V	1.5V	1.35V	1.2V
LVCMOS	LVCMS18	LVCMS15		LVCMS12 (Up to 8mA)
LVDS	LVDS***			
SSTL	SSTL18_I* SSTL18_II** DIFF_SSTL18_I* DIFF_SSTL18_II**	SSTL15** DIFF_SSTL15**	SSTL135** DIFF_SSTL135**	
HSTL	HSTL_I_18* HSTL_II_18** DIFF_HSTL_I_18* DIFF_HSTL_II**	HSTL_I* HSTL_II** DIFF_HSTL_I* DIFF_HSTL_II**		HSTL_I_12
LVDCI/HSLVDCI	LVDCI_18 HSLVDCI_18 LVDCI_DV2_18	LVDCI_15 HSLVDCI_15 LVDCI_DV2_15		

- * Supports DCI in addition to what is listed
- ** Supports DCI and T_DC1 in addition to what is listed
- *** LVDS inputs must have a common mode <= 1.8V

Highest performance I/O for High End and Some High Volume Applications

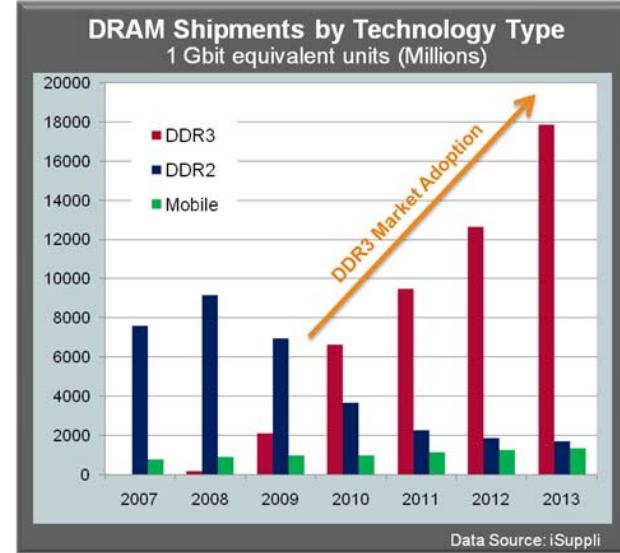
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DRAM TREND TO DDR3 FOR 2011-2013

85% Main Market

- DDR2/3 (1.5V and 1.8V)
 - > Volume leader driven by PC market adoption in 2010 resulting in lowest cost memory architecture
 - > 1866/1866Mb/s for high performance applications
 - > DDR4 expected introduction ~2013/2014



5% Low Power

- LPDDR (1.8V mobile), LPDDR2 (1.2V handsets)
 - > Driven by power standards for standby with partial refresh

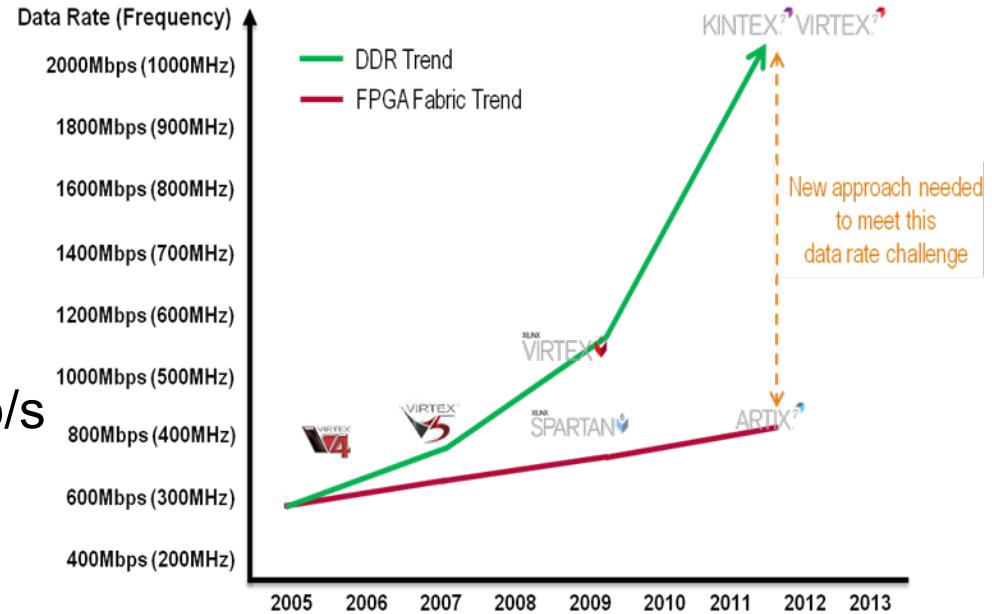
5% Networking

- QDRII/+, RLDRAM II / 3
 - > Driven by the need for low latency and fast random access cycle

CUSTOMERS NEED HIGHER PERFORMANCE INTERFACES

- Memory Interfaces
 - > DDR3 1866Mb/s
 - > QDRII+ 550MHz
 - > RLDRAM II 533MHz

- LVDS Interfaces
 - > Flat panel video link 1050Mb/s
 - > SFI-4.1 710Mb/s
 - > SPI-4.2 800+ Mb/s
 - > Specialty ASIC IF 1600+ Mb/s

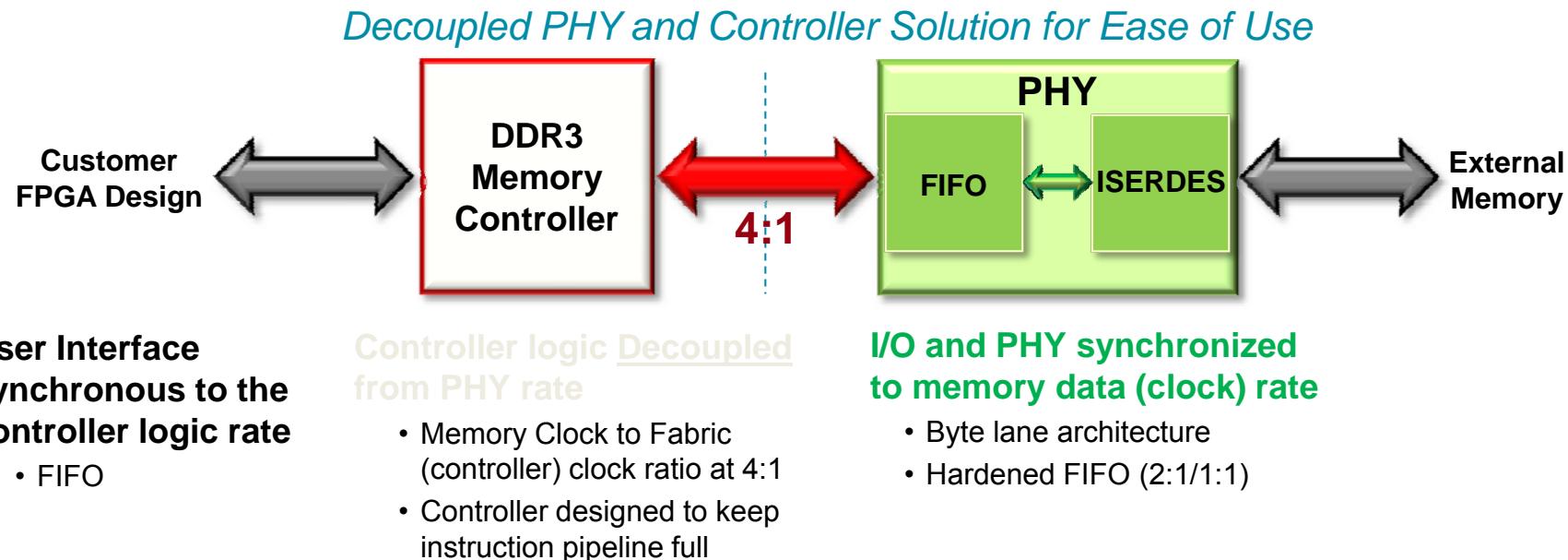


- High speed source synchronous data transmission

Data Rates increasing quicker than fabric performance

DEDICATED FIFO FOR PHY TO CONTROL DECOUPLING

- 7 Series Controller and PHY Architecture
 - > I/O that can keep up with the memory data rates
 - > Hardened PHY elements to keep up with the I/O rates
 - > $\frac{1}{4}$ rate soft controller in Fabric (decouple I/O rate from fabric speed)



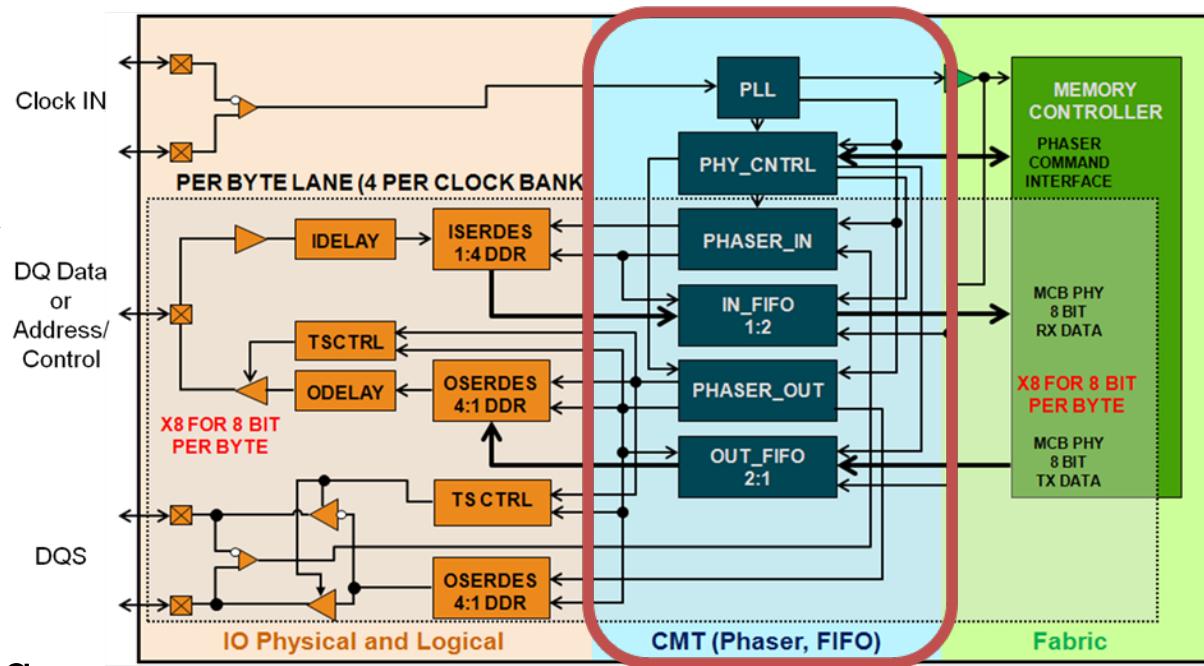
NEW I/O CLOCKING STRUCTURE IMPROVES CLOCK ADJUSTMENT

- Enhanced features of CMT
 - > Add additional MMCM columns and move next to I/O column
 - > Add new “Phaser” to CMT
- Created new “Phaser”
 - > **IO PLL** - Add reduced-functionality MMCM-lite (a basic PLL)
 - > **Phaser In** - VT stable circuit used for read data capture clocking for DDR3
 - > **Phaser Out** - VT stable circuit generating clocking for DDR3 data writes
- Created new “IO FIFO”
 - > Bridge variable phase PHY to fixed phase fabric
 - > Lower frequency on fabric side for design ease



NEW 7 SERIES CMT

- CMT per I/O bank now includes:
 - > 1 PLL block
 - > 1 PHY_CONTROL block
 - > 4 PHASER_IN blocks
 - > 4 PHASER_OUT blocks
 - > 4 IN_FIFO blocks
 - > 4 OUT_FIFO blocks
 - > 1 MMCM block
- Dedicated I/O clock routing
 - > Between the I/O logical and the Phaser blocks
 - > Shortest path, lowest noise and minimum skew



CMT and I/O tightly coupled for higher performance

PHASER BLOCK DETAILS

- PLL or IO PLL: Covered in clocking module
 - > Simple version of MMCM
 - > Generates output frequencies up to 1,866 Mb/s
- PHY_CONTROL
 - > Command interface between the Phaser blocks and IOSERDES and/or Fabric
 - > DLL to create bias for PVT independent delays to other Phaser sub blocks
- PHASER_IN: Clock inputs from ISERDES
 - > DQS phase detection
 - > Shift the sampling clock into the middle of data eye
 - > Clock division to accommodate ISERDES de-serialization ratio
- PHASER_OUT: Clock outputs to OSERDES
 - > Alignment DQS/Data byte group to CK per byte “flyby”
 - > Precise 90 degree phase shift of the sampling clock
 - > Clock division to accommodate OSERDES serialization ratio
 - > One PHASER_IN and One PHASER_OUT take care of a group of 12 I/Os

Each Bank is capable of supporting 4 different DQS groups

MEMORY ARCHITECTURES AND DATA RATES

Memory Architectures Supported	Spartan-6 FPGAs	Virtex-6 FPGAs	7 Series FPGAs
DDR2	Yes	Yes	Yes
DDR3	Yes	Yes	Yes
QDR-II+	No	Yes	Yes
RLDRAM II	No	Yes	Yes
RLDRAM 3	No	No	Yes
LPDDR	Yes	No	No
LPDDR2	No	No	Yes

Data Rates/Clock Frequency	Spartan-6 FPGAs	Virtex-6 FPGAs	Artix-7 FPGAs (3.3V I/O)	Kintex-7 FPGAs (1.8V I/O)	Virtex-7 FPGAs (1.8V I/O)
DDR3 (Data Rates)	800 Mb/s	1,066 Mb/s	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
QDR II+ (Clock Freq.)	N.A.	400 MHz	N.A.	550 MHz	550 MHz
RLDRAM II (Clock Freq.)	N.A.	500 MHz	N.A.	553 MHz *	533 MHz

* Under evaluation

Note: QDR II+ and RDRAM II maximum frequencies are limited by memory device specification

HIGH SPEED MEMORY INTERFACING SUMMARY

Higher Performance

- Improved Physical layer (PHY) architecture
 - > Dedicated byte lanes to improve timings for higher data rates
 - > New I/O clocking structure for better clock adjustment over voltage and temp. (Phaser)
 - > Dedicated FIFO for PHY to controller decoupling
- New high performance Phaser and IO FIFO blocks
 - > Phaser has ideal Hard blocks up to DDR3 1,866 Mb/s interfaces
 - > Addition of I/O FIFO decouples the physical timing from core timing
- Tightly coupled CMT to I/O structure
 - > Will meet demanding performance needs for high speed DDR3 interfaces

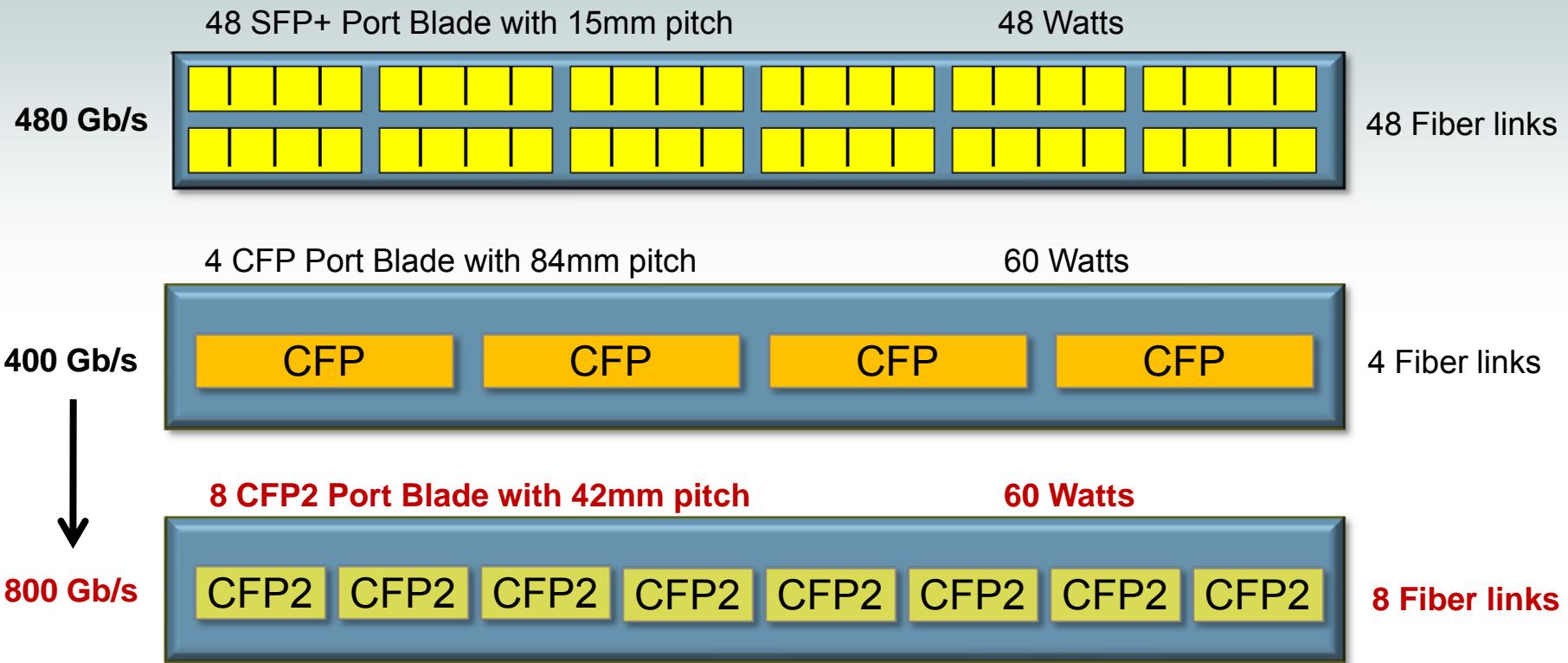
Higher Productivity

- Setup of Phaser, IO FIFOs and high speed clock routing controlled by MIG
 - > Increased User Flexibility and Ease of Use
- Broad Memory Architecture support
 - > DDR3, DDR2, LPDDR2, QDR-II+, RLDRAM II/ 3
- AXI4 support for IP Plug and Play
 - > Scalable Optimized Architecture across Artix-7, Kintex-7 and Virtex-7 FPGAs for easier IP development

AGENDA

- 7 Series Introduction
- Power Reduction
- Performance
 - > CLB and Embedded Memory
 - > Clocking
 - > I/O
 - > High Speed Memory Interfacing
 - > **High Speed Serial Transceivers**
 - > PCI Express® Interface
 - > DSP
- Productivity
 - > Agile Mixed Signal (AMS) / XADC
- 7 Series Leadership Summary

TACKLING THE POWER AND BANDWIDTH DILEMMA



Power Density is the Primary Limiting Factor

7 SERIES TRANSCEIVER OVERVIEW

- GTP (6.6 Gb/s): Artix-7 FPGAs
 - > Main stream connectivity in ultra low-cost packages
- GTX (12.5 Gb/s): Kintex-7 and Virtex-7 FPGAs
 - > Cost effective 12.5 Gb/s in low density FPGAs
 - ◆ FPGA solutions can be less expensive than off-the-shelf 10 Gb/s PHY
 - > Supports PCI Express Gen1, 2 and 3, CPRI9.8G
 - > Support for high performance backplanes
 - > Low power mode for optimizing chip-to-chip communications
 - > Backwards compatibility with 6.6G and below Virtex-6 GTX designs
- GTH (13.1 Gb/s): Virtex-7 FPGAs
 - > Supports 25% overhead required for EFEC in wired OTU applications
 - > 10GBASE-KR support for high performance backplanes
 - > Higher rate backplanes & next generation optical networking to 12.5 Gb/s+
- GTZ (28.05 Gb/s): Virtex-7 HT FPGAs
 - > Enables bandwidth for 100 - 400G applications supporting major high-speed serial and optical protocols
 - > Lowest jitter and highest signal quality



7 SERIES TRANSCEIVER PROTOCOL SUPPORT¹

Market	Protocol	Artix-7 GTP	Kintex-7/Virtex-7 GTX	Virtex-7 GTH
General	PCI Express	Gen1, 2	Gen1, 2, 3	Gen1, 2, 3
Wired	Ethernet	1GE, 2.5GE, XAUI, RXAUI	1GE, 2.5GE, XAUI, RXAUI, 10GBase-R, 10G-KR*, 40GE, 100GE	1GE, 2.5GE, XAUI, RXAUI, 10GBase-R, 10G-KR (enhanced), 40GE, 100GE
	SONET/OTU	OC-3/12/48	OC-3/12/48/192, OTU1/2/3/4	OC-3/12/48/192, OTU1/2/3/4
	Interlaken	<= 6.6G	<=6.5G, 10.3125G 12.5G	<=6.5G, 10.3125G, 12.5G
	Custom CEI Backplane	<= 6.6G	<=6.5G, CEI-11-LR*	<= 6.5G, CEI-11LR (enhanced)
	PON	BPON, GPON, GEAPON (up to 1.25 BCDR)	BPON, GPON, GEAPON, 10GEAPON, 10GGPON (up to 2.5G BCDR)	BPON, GPON, GEAPON, 10GEAPON, 10GGPON
Wireless	CPRI/OBSAI	0.614, 1.2, 2.4, 3.0, 4.9, 6.6	0.614, 1.2, 2.4, 3.0, 4.9, 6.14, 9.8, 12	0.614, 1.2, 2.4, 3.0, 4.9, 6.14, 9.8, 12
	Serial Rapid IO	Gen1, 2	Gen1, 2	Gen1, 2
Audio Video ²	SDI	SD/HD/3G-SDI	SD/HD/3G-SDI/10G-SDI	SD/HD/3G/10G-SDI
	DisplayPort	1.6, 2.7, 5.4	1.6, 2.7, 5.4	1.6, 2.7, 5.4
Other	QPI	-----	4.8, 6.4, 8.0, 9.6	4.8, 6.4, 8.0, 9.6
	Fiber Channel	1G, 2G	1G, 2G, 4G, 10G	1G, 2G, 4G, 8G, 10G
	SATA/SAS	1.5G, 3G, 6G	1.5G, 3G, 6G	1.5G, 3G, 6G
	Aurora	Up to 6.6G	Up to 12.5G	Up to 13.1G

1: Consult 7 series transceiver user guide for latest information. 2: V-by-One supported through 3rd party.

VIRTEX-7 HT FPGA BANDWIDTH LEADERSHIP

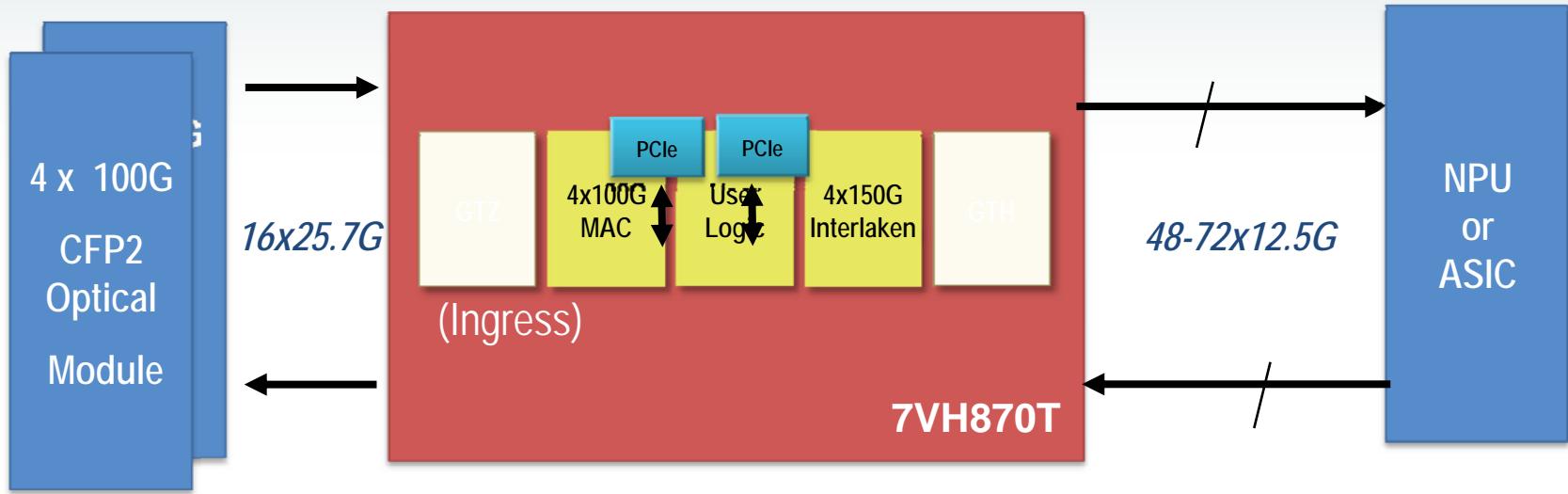
Bandwidth and Feature Leadership

Parameter	Virtex-7 HT FPGA	Competitive Solution	Xilinx Advantage
28G Transceivers	8 - 16	4	4x
13.1G Transceivers	48 - 72	32 (12.5G only)	2.25x
Total Bandwidth	2.78 Terabits	1.02 Terabits	2.7x
Logic Cells (K)	580 - 876	435 - 622	1.4x
On Die Memory (Mb)	34 - 51	47 - 51	1.3x
DSP	1,680 – 2,520	640 - 684	5.8x
Parallel IO	650	597	1.2x
Devices in Family	2	2	1.5x

Virtex-7 HT FPGA competitive advantage comparison

APPLICATION EXAMPLE – 400GE LINE CARD

- Enables manufacturers to be first-to-market with 400GE line cards
- Integrated 400G interface to optical modules
- Interface up to four ASIC or NPUs



Only FPGA that Enables a Single Chip 400G Implementation

28GB/S TRANSCEIVER PERFORMANCE

SEE DEMO ON XILINX.COM

See Industry's Fastest, Lowest
Jitter 28Gb/s FPGA running live!

A man with glasses and a beard, identified as Dr. Howard Johnson, is speaking on stage. To his right is a computer setup with a Dell monitor displaying a signal integrity analysis software interface. The software shows a complex multi-lane signal waveform with various performance metrics and graphs. Below the monitor is a signal generator or analyzer unit with various knobs and buttons. The Xilinx logo is visible on the front panel of the equipment.

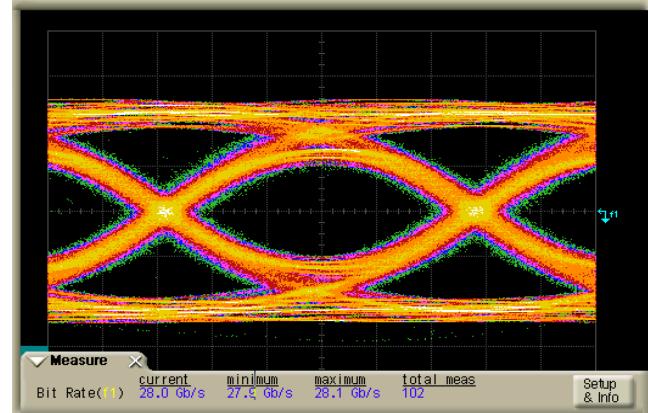
Dr. Howard Johnson, Signal Integrity Expert
Author of "High Speed Digital Design: A Handbook of Black Magic"



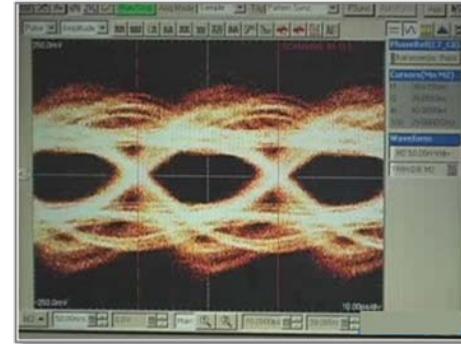
VIRTEX-7 HT VS. LEADING 28G SOLUTION

EYE COMPARISON – REALLY NO COMPARISON

- Xilinx clean 28G with excellent eye opening and jitter performance
 - > Using realistic PRBS31 data pattern



- Competitor is extremely noisy with a significantly smaller eye opening
 - > Using much simpler PRBS7 pattern



Note: Eye size is shown close to relative scale, competition has a **significantly smaller opening!**

Fastest, Lowest Jitter Serial Transceivers that meet the OIF CEI28G specs

7 SERIES TRANSCEIVER DIFFERENTIATION

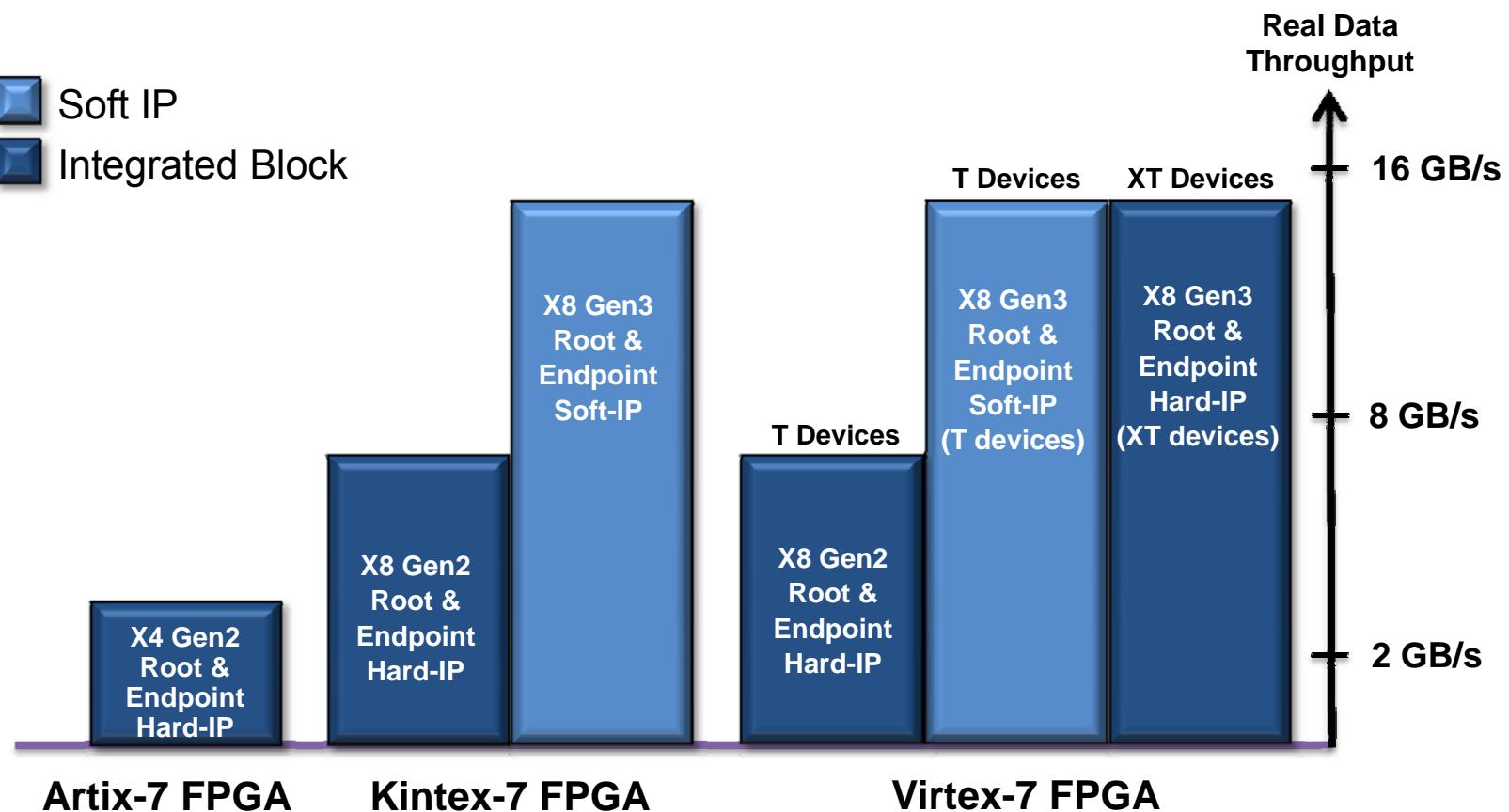
- Common Transceiver architecture across 7 series enabling IP portability
- 10Gb/s for high volume applications
 - > Lower density Kintex-7 and Virtex-7 FPGAs can now be more cost effective than discrete solutions with PHY
- Power efficient support for QPI
 - > Next-generation Intel µP interconnect opens up new markets
 - > Possible to place Xilinx FPGA in processor socket of multi-processor server
- Extra margin for PCI Express
 - > LC tank in Kintex-7 and Virtex-7 FPGAs allow more margin for low cost PCIe compliance
- Comprehensive Transceivers coverage
 - > Artix-7 GTP: High-volume 6.6 Gb/s
 - > Kintex-7 GTX: Lowest cost 12.5 Gb/s
 - > Virtex-7 GTX: Cost effective 12.5 Gb/s
 - > Virtex-7 GTH: Highest performance/count up to 13.1 Gb/s
 - > Virtex-7 GTZ: Support for next generation 28.05 Gb/s applications

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7 SERIES FPGA PCI EXPRESS SOLUTIONS

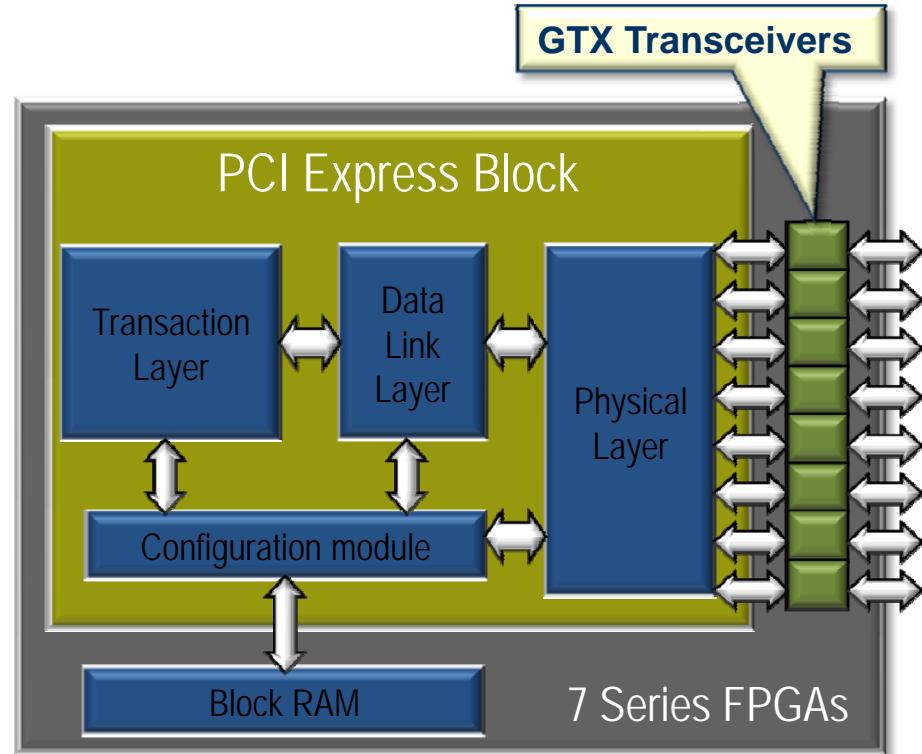
- Soft IP
- Integrated Block



Hard PCI Express block in Every 7 Series Family –
Scalable Optimized Architecture for Scalable Bandwidth

7 SERIES GEN2 INTEGRATED BLOCK

- Features
 - > Compliant to PCIe **revision 2.1** **NEW!**
 - > Endpoint & Root Port
 - > AXI user interface
 - > <100ms FPGA configuration over PCI Express
 - > Easy migration from previous generation
- NEW!** End-to-end CRC
- NEW!** Advanced Error Reporting
- Wrappers
 - > Multi-Function
 - > Single-Root I/O Virtualization
- Configurations
 - > Lane Widths: x1-8
 - > Data Rates: Gen1 & Gen2 (2.5/5.0 Gb/s)
 - > Scales with device, GT and fabric speed

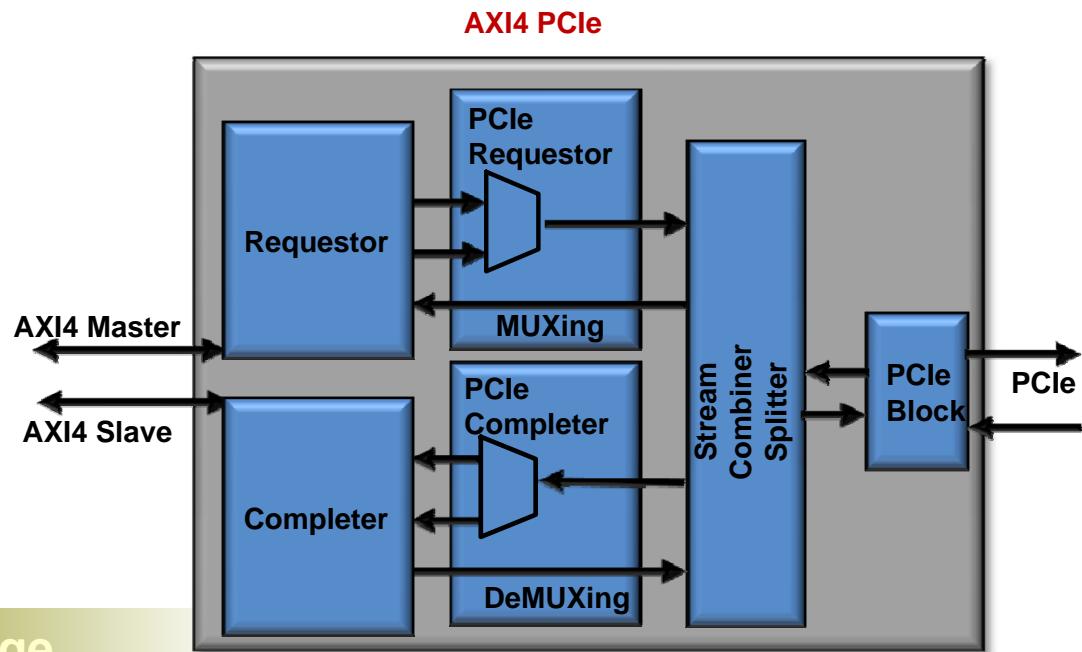
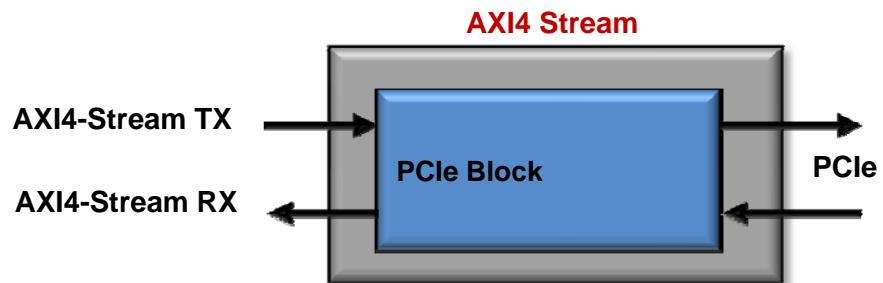


PCI Express Scales with Device, GT and Fabric Speed

7 SERIES PCIE AXI4 INTERFACES

DESIGNED FOR DIFFERENT PERSONAS

- AXI4 Stream
 - > Easy migration from Local Link
 - > Maximum control
 - > Maximum performance
 - > Starting in IDS 13.1
- AXI4 (Memory Mapped)
 - > Memory Mapped Users
 - > Processor/EDK Users
 - > Migration from PLB46
 - > Starting in IDS 13.2



Extensive PCI Express Coverage
for Different User Needs

NEW GEN3 SUPPORT

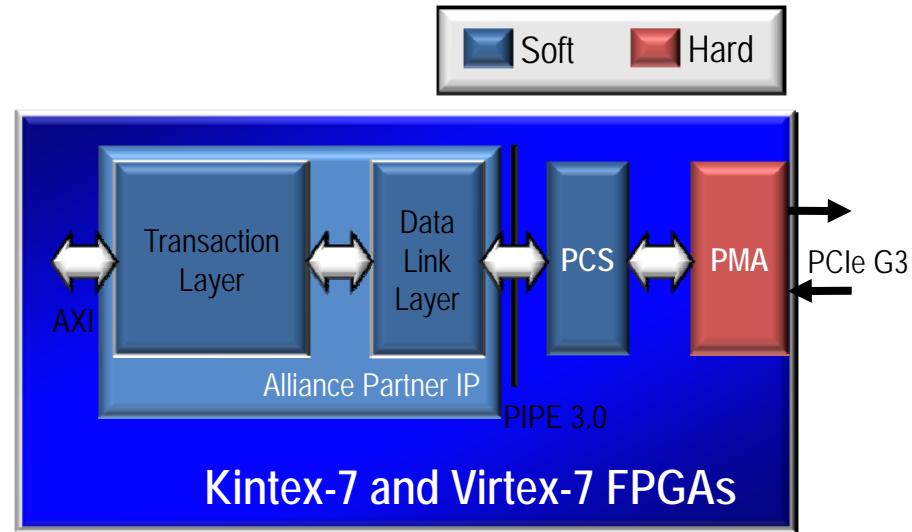
	Encoding	Line Rate Per Lane	Effective Data Rate
Gen1	8b10b	2.5Gb/s	2Gb/s
Gen2	8b10b	5Gb/s	4Gb/s
Gen3	128b130b & Scrambling	8Gb/s	~8Gb/s

- New PHY Layer
 - > 8Gb/s raw line rate per lane
 - > 128b130b encoding/scrambling
 - ◆ 1.5% encoding overhead
 - > Doubles the data throughput
- Protocol Enhancements
 - > 2.1 ECNs
 - > Additional ECNs

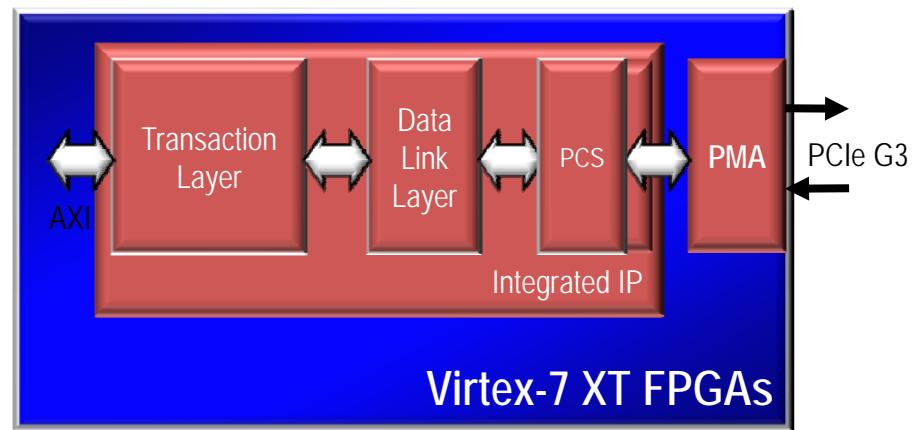
Gen3 interface required to also support Gen1 and Gen2 on same pairs of wires

7 SERIES GEN3 SOLUTIONS

- Kintex-7, Virtex-7T & XT FPGAs
 - > Supported in -2 & -3 speed grades
 - > Xilinx supplied Gen3 PCS/PMA
 - ◆ GTX Transceivers
 - ◆ PIPE 3.0
 - > Alliance Partner soft IP for Gen3
 - ◆ Northwest Logic
 - ◆ PLDA



- Virtex-7XT FPGAs
 - > Integrated block for PCIe Gen3
 - > Up to 8-lanes Gen3



7 SERIES PCI EXPRESS DIFFERENTIATION

- PCIe Gen2 Integrated Block
 - > Build on a proven architecture
 - > Integrated blocks up to Gen2x8 in Kintex-7 and Virtex-7 FPGAs, Gen2x4 in Artix-7 FPGAs
 - > Adding support for new capabilities:
 - ◆ ECRC, AER, SR-IOV, and Multi-Function
- PCIe Gen3
 - > Supported in Kintex-7 and Virtex-7 GTX transceivers
 - > Supported with Alliance Partner soft IP in Kintex-7 and Virtex-7 FPGAs
 - ◆ Northwest Logic and PLDA
 - > Integrated blocks in Virtex-7 XT devices

AGENDA

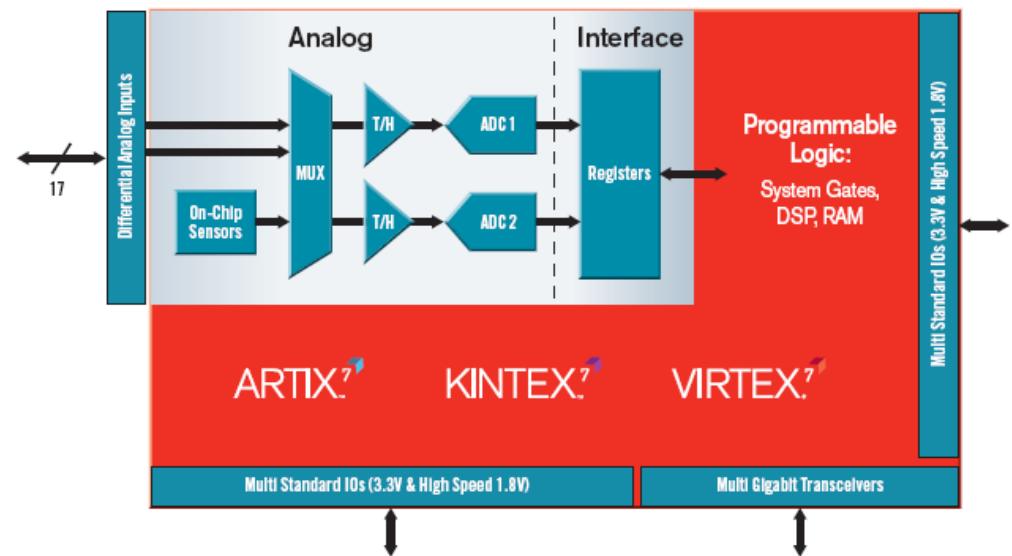
- 7 Series Introduction
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 - > Agile Mixed Signal (AMS) / XADC
- 7 Series Leadership Summary

XILINX AGILE MIXED SIGNAL TECHNOLOGY

CUSTOMIZED ANALOG WITH FPGA FLEXIBILITY

- Customizable Analog → Xilinx Analog to Digital Converter (XADC)
 - > Dual Independent ADCs
 - > Track and hold Capability
 - > 17 Multiplexed Analog inputs
 - > On-Chip Voltage and Temperature Sensors
 - > 16 bit register interface to ...

- Flexible FPGA fabric



LEARN MORE ABOUT AGILE MIXED SIGNAL TECHNOLOGY

- Available in ALL 7 series families and devices Artix-7, Kintex-7, Virtex-7 FPGAs
- Learn More at www.xilinx.com/AMS
 - > “Agile Mixed Signal” white paper (WP392)
 - > XADC User Guide
- Afternoon X-Tech presentation at 3:00pm



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7 SERIES FAMILIES COMPARISON

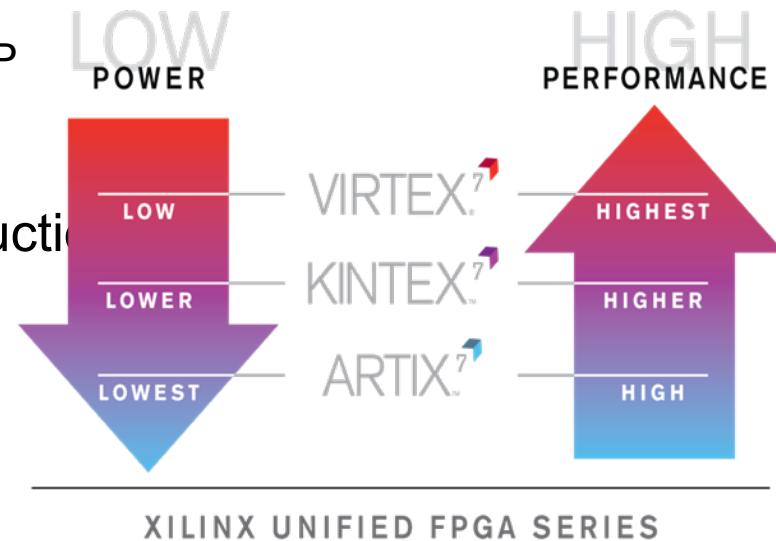
➤ Scalable Optimized Architecture, scalable across all families from high-volume to ultra high-end applications

- Each family is power, performance and price optimized to meet target application

Maximum Capability	Artix-7 FPGAs	Kintex-7 FPGAs	Virtex-7 FPGAs
Logic Cells	215K	478K	1,955K
Block RAM	13 Mb	34 Mb	68 Mb
DSP Slices	740	1,920	3,600
Peak DSP Performance (symmetric FIR)	929 GMACS	2,845 GMACS	5,335 GMACS
Transceiver Count	16	32	96
Peak Transceiver Speed	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Peak Serial Bandwidth (full duplex)	211 Gb/s	800 Gb/s	2,784 Gb/s
PCI Express Interface	Gen2x4	Gen2x8	Gen3x8*
Memory Interface	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	500	500	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V*
Packaging Options	Low cost wire-bond	Low cost lidless flip-chip and high performance flip-chip	Highest performance flip-chip

7 SERIES MEETS NEXT GENERATION DESIGN CHALLENGES

- Lowest Total Power Allowing Additional System Performance
 - > 65% lower static power consumption
 - > 25%+ lower dynamic power consumption
 - > 30% lower I/O dynamic power consumption
- Highest Productivity
 - > Scalable Optimized Architecture enables IP portability and design scalability saving engineering investments
 - > EasyPath™-7 for fastest cost reduction
- 2x System Performance
 - > Advanced features and industry leading capacity



ARTIX-7 FPGA PRODUCT TABLE

		Artix™-7 FPGAs Optimized for Lowest Cost and Lowest Power Applications (1.0 Volt, 0.9 Volt)									
Product Status		Artix™-7 SL FPGAs				Artix™-7 SLT FPGAs				Artix™-7T FPGAs	
		Advance		Advance		Advance		XC7A100T		XC7A200T	
Logic Resources	Part Number	XC7A20SL	XC7A35SL	XC7A50SL	XC7A75SL	XC7A20SLT	XC7A35SLT	XC7A50SLT	XC7A75SLT	XC7A100T	XC7A200T
	Slices	2,500	5,142	8,200	11,194	2,500	5,142	8,200	11,194	15,850	33,650
	Logic Cells	16,000	32,909	52,480	71,642	16,000	32,909	52,480	71,642	101,440	215,360
Memory Resources	CLB Flip-Flops	20,000	41,136	65,600	89,552	20,000	41,136	65,600	89,552	126,800	269,200
	Maximum Distributed RAM (Kbits)	208	453	688	974	208	453	688	974	1,188	2,888
	Block RAM/FIFO w/ ECC (36Kbits each)	30	65	95	125	30	65	95	125	135	365
Clock Resources	Total Block RAM (Kbits)	1,080	2,340	3,420	4,500	1,080	2,340	3,420	4,500	4,860	13,140
	CMTs (1 MMCM + 1 PLL)	3	3	4	4	3	3	4	4	6	10
I/O Resources	Maximum Single-Ended I/O	216	216	300	300	216	216	300	300	300	500
	Maximum Differential I/O Pairs	54	54	72	72	54	54	72	72	144	240
Embedded Hard IP Resources	DSP48E1 Slices	60	120	180	240	60	120	180	240	240	740
	PCI Express® ⁽¹⁾	—	—	—	—	1	1	1	1	1	1
	Agile Mixed Signal (AMS)/XADC	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)	—	—	—	—	4	4	8	8	8	16
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Package ⁽³⁾	Dimensions(mm)	Available User I/O: 3.3V SelectIO™ HR I/O, 3.3V SelectIO™ HD I/O Pins						Available User I/O: 3.3V SelectIO™ HR I/O Pins		
	CPG236	10 x 10	48, 52	48, 52							
	CSG325	15 x 15	108, 108	108, 108							
	CSG484	19 x 19		144, 156	144, 156						
	CPG237	10 x 10				48, 52 (1)	48, 52 (1)				
	CSG326	15 x 15				108, 77 (4)	108, 77 (4)	108, 77 (4)	108, 77 (4)		
	CSG485	19 x 19				108, 108 (4)	108, 108 (4)	126, 108 (6)	126, 108 (6)		
	FGG677	27 x 27						144, 156 (8)	144, 156 (8)		
	CSG324	15 x 15								210 (0)	
	FTG256	17 x 17								170 (0)	
	SBG484	19 x 19									285 (4)
Footprint Compatible	FGG484 ⁽²⁾	23 x 23									285 (4)
	FBG484 ⁽²⁾	23 x 23									285 (4)
Footprint Compatible	FGG676 ⁽²⁾	27 x 27								300 (8)	
	FBG676 ⁽²⁾	27 x 27								400 (8)	
	FFG1156 ⁽²⁾	35 x 35								500 (16)	

CPG: 0.6mm Wire-bond chip-scale; **CSG:** 0.8mm Wire-bond chip-scale; **FTG:** 1.0mm Wire-bond fine-pitch; **SBG:** 0.8mm Flip-chip bare-die; **FGG:** 1.0mm Wire-bond fine-pitch; **FBG:** 1.0mm Flip-chip bare-die; **FFG:** 1.0mm Flip-chip fine-pitch

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates .

2. Leaded package options available.

3. Design migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/



KINTEX-7 FPGA PRODUCT TABLE

		Kintex-7 FPGAs Optimized for Best Price-Performance (1.0V, 0.9V)						
Part Number		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XCE7K410T	XC7K420T	XC7K480T
EasyPath™ Cost Reduction Solutions ⁽¹⁾		—	—	—	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kbits)	838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36Kbits each)	135	325	445	715	795	835	955
	Total Block RAM (Kbits)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
Embedded Hard IP Resources	DSP48E1 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCI Express® ⁽²⁾	1	1	1	1	1	1	1
	Agile Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers	8	8	16	24	16	32	32
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
Configuration	Configuration Memory (Mbits)	23.0	51.1	87.3	107.3	121.1	143.0	143.0
Footprint Compatible	Package ⁽⁴⁾	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX Transceivers)						
	FBG484	23 x 23	185, 100 (4)	185, 100 (4)				
	FBG676	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)	250, 150 (8)		
	FFG676	27 x 27		250, 150 (8)	250, 150 (8)	250, 150 (8)		
	FBG900	31 x 31			350, 150 (16)	350, 150 (16)		
	FFG900	31 x 31			350, 150 (16)	350, 150 (16)		
	FFG901	31 x 31			300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156	35 x 35					400, 0 (32)	400, 0 (32)

XMP085 (v3.4)

FBG: 1.0mm Lidless flip-chip; FFG: 1.0mm Flip-chip fine-pitch

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.

2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.

3. Leaded package options ("FBxxx" or "FFxxx") available for the following Kintex-7 devices: XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T

4. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.



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VIRTEX-7 FPGA PRODUCT TABLE

		Optimized for Highest System Performance and Capacity										
		(1.0V, 0.9V)			(1.0V, 0.9V)			(1.0V)			(1.0V)	
	Part Number	XCE7V585T	XCE7V2000T	XCTVX330T	XCTVX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCTVX980T	XCTVX1140T	XCTVH580T	XCTVH870T
	EasyPath™ Cost Reduction Solutions ⁽¹⁾	XCE7V585T	XCE7V2000T	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	XCE7VX1140T	—	—
Logic Resources	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells	582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Stacked RAM/FIFO w/ ECC (36 Kb each)	795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O	850	1,200	700	600	700	600	1,000	900	1,100	600	650
	Maximum Differential I/O Pairs	408	576	336	288	336	288	480	432	528	288	312
Embedded IP Resources	DSP48E1 Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCI Express Gen2	3	4	—	—	4	—	—	—	—	—	—
	PCI Express Gen3	—	—	2	2	—	2	3	3	4	2	3
	Agile Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers ⁽²⁾	36	36	—	—	56	—	—	—	—	—	—
	GTH 13.1 Gb/s Transceivers ⁽³⁾	—	—	28	48	—	80	80	72	96	48	72
	—	—	—	—	—	—	—	—	—	—	8	16
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended ⁽⁴⁾	-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -2G	-2L, -2G	-2L, -2G	-2L, -2G
	Industrial	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—
Package ⁽⁵⁾		Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX, GTH Transceivers)									1.8V SelectIO Pins (GTH, GTZ)	
Flip chip, fine pitch BGA (1.0 mm ball spacing)												
Footprint Compatible	FFG1157	35 x 35 mm	0, 600 (20, 0)	—	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (20, 0)	—	0, 600 (0, 20)	—	—	—
	FFG1761	42.5 x 42.5 mm	100, 750 (36, 0)	—	50, 650 (0, 28)	—	0, 700 (28, 0)	—	0, 850 (0, 36)	—	—	—
	FLQ1761	42.5 x 42.5 mm	—	—	—	—	—	—	—	—	—	—
Footprint Compatible	FHG1761	45 x 45 mm	—	0, 850 (36, 0)	—	—	—	—	—	—	—	—
	FLG1925	45 x 45 mm	—	0, 1200 (16, 0)	—	—	—	—	—	—	—	—
	FFG1158	35 x 35 mm	—	—	—	0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)	—	—	—
Footprint Compatible	FFG1926	45 x 45 mm	—	—	—	—	—	—	—	0, 720 (0, 64)	0, 720 (0, 64)	—
	FLG1926	45 x 45 mm	—	—	—	—	—	—	—	—	0, 720 (0, 64)	—
	FFG1927	45 x 45 mm	—	—	—	0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)	—	—	—
Footprint Compatible	FFG1928	45 x 45 mm	—	—	—	—	—	—	—	0, 480 (0, 72)	—	—
	FLG1928	45 x 45 mm	—	—	—	—	—	—	—	—	0, 480 (0, 96)	—
Footprint Compatible	FFG1930	45 x 45 mm	—	—	—	0, 700 (24, 0)	—	0, 1000 (0, 24)	0, 900 (0, 24)	—	—	0, 1100 (0, 24)
	FLG1930	45 x 45 mm	—	—	—	—	—	—	—	—	—	—
Ceramic flip chip, fine pitch BGA (1.0 mm ball spacing)												
	HCG1155	35 x 35 mm	—	—	—	—	—	—	—	—	400 (24, 8)	—
	HCG1931	45 x 45 mm	—	—	—	—	—	—	—	—	600 (48, 8)	650 (48, 8)
	HCG1932	45 x 45 mm	—	—	—	—	—	—	—	—	300 (48, 8)	300 (72, 16)

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.

2. 12.5 Gb/s support in "-3E", "-2GE" speed/temperature grade; 10.3125 Gb/s support in "2C", "-2LE", and "-2I" speed grade.

3. 13.1 Gb/s support in "-3E", "-2GE" speed grade; 11.3 Gb/s support in "2C", "-2LE" and "-2I" speed/temperature grades.

4. -2G only applies to Stacked Silicon Interconnect devices and supports 12.5G GTX, 13.1G GTH, 28.05G GTZ with -2 fabric.

5. Leaded package options ("FFxxxx"/"FLxxxx"/"FHxxxx"/"HCxxxx") available for all packages.



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