WP469 (v1.0) September 28, 2015

Using the MicroBlaze Processor to Accelerate Cost-Sensitive Embedded System Development

By: Vaibhav Kale

The MicroBlaze™ soft processor core and the associated embedded solution reduce software development, IP integration, and design bring-up time for cost-sensitive, high-volume applications by enabling customers to build embedded systems faster.

ABSTRACT

The MicroBlaze processor is a full-featured, programmable device-optimized, 32-bit RISC soft processor core. It meets diverse requirements in the industrial, medical, automotive, consumer, and communications infrastructure markets, among others—for cost sensitive, high-volume applications. It is highly configurable and can be used as the microcontroller or embedded processor in FPGAs (Spartan®-6 or Artix®-7 FPGAs), or as a co-processor for the ARM® Cortex®-A9 based Zynq®-7000 All Programmable SoCs (AP SoCs).

For optimized embedded systems development, the availability of easy-to-use hardware and software development and debug tools, run-time software, and IP plays a big role. To fill this need, Xilinx also provides the Vivado® Design Suite, which includes the Vivado IP Integrator (IPI) and the ISE® Embedded edition (for Spartan-6 FPGAs). These tools deliver an IP- and system-centric development environment, featuring AXI4 based Plug-and-Play embedded IPs and a full Software Development Kit (SDK). These components help users build better systems faster, reducing overall solution development time.

Introduction

Despite the growing complexity and sophistication of embedded systems—even for low-end, cost-sensitive applications—the exceptional time-to-market pressure continues to increase.

Even low-end programmable solutions have moved far beyond glue logic to full-featured, high-value components that enable key system intelligence through embedded processing. Having the right programmable device and embedded processor is no longer a complete solution; it is now equally important to have capable software tools, run-time software, peripheral IP support, and documentation.

This white paper focuses not only on the key MicroBlaze processor features, but also on the complete Xilinx solution, which includes AXI4 Plug-and-Play IPs, the Vivado IP Integrator tool, SDK for rapid software development and debug, reference designs, kits and boards, and of course the silicon devices themselves.

Embedded Processor Characteristics

Xilinx FPGA embedded processor systems offer the designer many exceptional advantages when compared to typical microprocessors, including customization, obsolescence mitigation, component cost reduction, and hardware acceleration.

- **Customization:** The designer of an embedded processor system has complete flexibility to customize the embedded processor based on configuration options. As a soft IP core, multiple processors can be instantiated on the same hardware device, depending on the needs of the end application. The availability of configurable peripherals also helps in the creation of custom embedded solutions, because the Xilinx development tools facilitate both the design and integration of specific peripherals.
- **Obsolescence Mitigation:** Some industries—particularly those supporting the Aerospace and Defense market segment—have strict design requirements to ensure that a product's lifespan is much longer than that of a standard electronics product. The need to mitigate component obsolescence can be seen as a difficult issue; soft processors, however, provide an excellent solution, because the same core can be supported and migrated across various device families over an extended life span.
- **Cost Reduction through System Integration:** The advantage of a programmable device is not just customizable digital logic; it is, rather, the broad array of functions—in some cases, non-digital—available in today's technology. A system's high-value digital components can comprise processors, DSPs, ASSPs, FPGAs, SoCs, or a combination of these; its non-digital components can include ADCs, sensors, and PHY interfaces, among others. Devices from the Xilinx Low-End Portfolio can integrate much of this functionality on a single chip. By reducing the component count in a design, a company can reduce board size and inventory management, both of which save design time and cost.
- **Hardware Acceleration:** Perhaps the most compelling reason to choose a programmable device embedded processor is the flexibility to make trade-offs between hardware and software, thus maximizing efficiency and performance. For example, if an algorithm is identified as a software bottleneck, a custom co-processing engine can be designed in the FPGA specifically for that algorithm. This co-processor can be attached to the FPGA embedded

processor through special low-latency channels. Unlike off-the-shelf processors, Xilinx design tools support features and flows like Vivado High-Level Synthesis, which enables IP creation from C/C++ and SystemC without needing to manually write the RTL.

MicroBlaze Processor Advantages

Since 2002, the MicroBlaze processor has evolved to incorporate many sophisticated features to meet the demands of new and expanding markets. In Xilinx's Low-End Portfolio, which includes Spartan®-6 and Artix®-7 FPGAs, and Zynq®-7000 AP SoCs, the MicroBlaze processor is a key element in enabling faster system development. It is highly configurable and can be used as the microcontroller or embedded processor in FPGAs, or as a co-processor for the ARM Cortex-A9 based Zynq-7000 AP SoCs.

Figure 1 is a block diagram of the MicroBlaze processor core. The MicroBlaze IP core is highly customizable, supporting more than 70 configuration options. The block diagram shows fixed hardware features/blocks and configurable options such as the Instruction/Data Cache, the Floating Point Unit, the Memory Management Unit, and many others. With this highly flexible core, the user can implement virtually any processor use case—from a very-small-footprint state machine or microcontroller to a high-performance, compute-intensive microprocessor based system running Linux. The IP can be configured to operate in either a three-stage pipeline mode (to optimize for size), or a five-stage pipeline mode (to optimize for speed), delivering faster Dhrystone Million Instructions per Second (DMIPS) performance than any other FPGA-based soft processing solution.

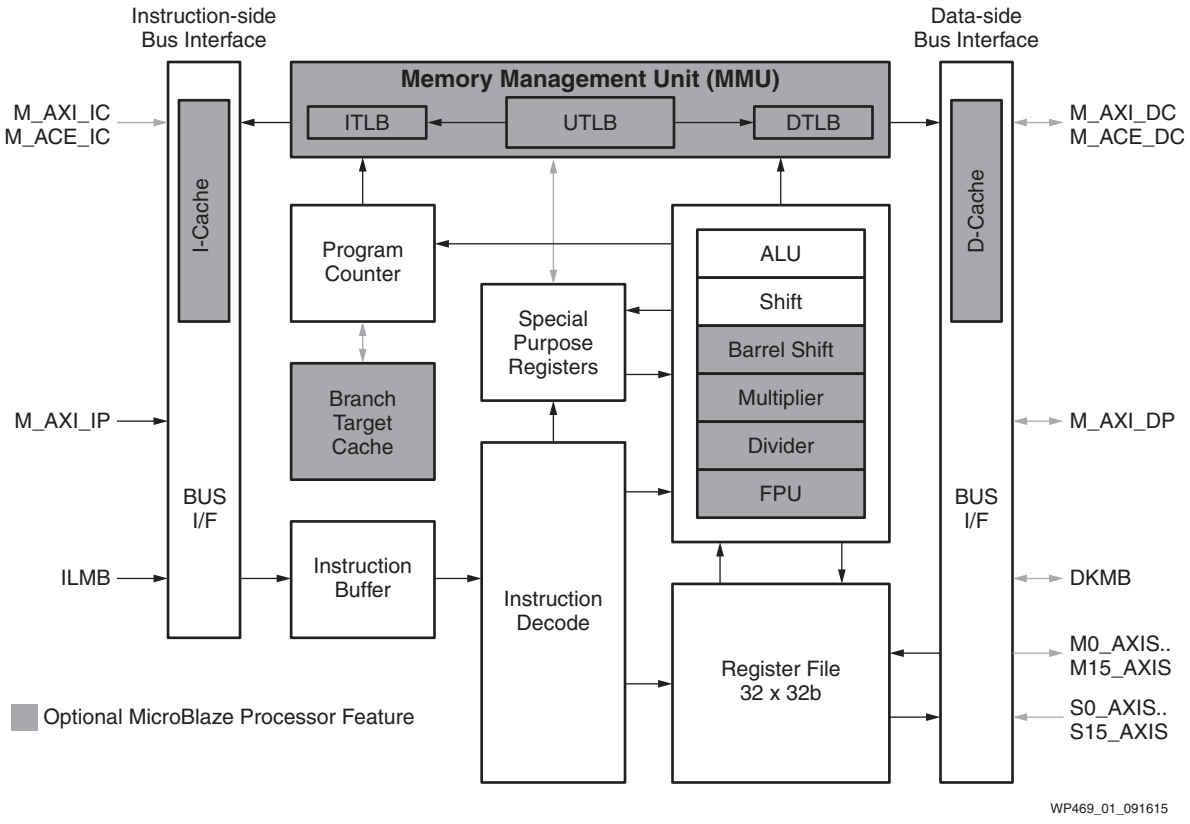

Figure 1: **MicroBlaze Processor Block Diagram**

Xilinx offers a Configuration Wizard to facilitate implementation of the MicroBlaze processor, providing quick, predefined configuration options to the user. Instead of being required to configure the processor from a palette of 70-some discrete options, the user can instead select sets of predefined options based on use cases. Table 1 shows various predefined configuration options and typical use case descriptions.

Table 1: **MicroBlaze Processor Configuration Wizard Predefined Options**

Predefined Configuration	Description
Minimum Area	Smallest possible MicroBlaze core, no caches, no debug.
Maximum Performance	Maximum performance, large caches, debug, and execution unit.
Maximum Frequency	Maximum achievable frequency. Small caches and no debug, with few execution units.
Linux with MMU	Settings suitable to get high performance when running Linux with Memory Management Unit (MMU). Memory Management enabled, large caches and debug, and all execution units.
Low-End Linux with MMU	Settings correspond to the MicroBlaze Processor Embedded Reference System. Provides suitable settings for Linux development on low-end systems. Memory Management enabled, small caches, and debug.
Typical	Settings giving a reasonable compromise between performance, area, and frequency. Suitable for stand-alone programs, and low-overhead kernels. Caches and debug enabled.

The user can opt for a two-step configuration flow. A predefined configuration (as listed in Table 1) is selected and then fine-tuned by choosing a few specific configuration options to suit the exact use case. For example, the user could select Minimum Area as the predefined configuration, then select Enable MicroBlaze Debug Module for debug purposes.

Following are brief descriptions of key MicroBlaze features, many of which are user-configurable—hence the need to be enabled as part of the configuration process.

Number of Pipelines

The MicroBlaze processor instruction executions are pipelined. Depending on design requirements, the user can select an Area Optimized configuration (a 3-stage pipeline architecture) or a Performance Optimized configuration (a 5-stage pipeline architecture).

Instruction and Data Cache

The MicroBlaze processor core can be used with optional instruction and data caches for improved performance. Activating caches significantly improves performance when using external memory, even if small cache sizes must be selected to reduce resource usage.

High-Performance AXI4 Interfaces

The MicroBlaze processor core natively supports high-performance industry standard buses: AXI4/AXI Coherency Extension (ACE) (for cache access), AXI4/AXI4-Lite (for peripheral access), and Master/Slave AXI4-Stream.

MMU Support

When an operating system that supports virtual memory (e.g., Linux) is being run, the MicroBlaze processor can manage it. Virtual memory management provides greater control over memory protection.

Select Bus Interface

The MicroBlaze processor bus interface can be set to AXI or ACE. An AXI bus selection causes both peripheral and cache access to be enabled. When the bus selection parameter is set to ACE, then AXI is selected for peripheral access, while ACE is selected for cache access, providing cache coherency support.

Stream Link Interfaces

The MicroBlaze processor can be configured with up to 16 AXI4-Stream interfaces, each comprising one input port and one output port. The channels are dedicated unidirectional, point-to-point, data-streaming, 32-bit-wide interfaces between the MicroBlaze processor and a hardware accelerator or co-processor. Each link provides a low-latency dedicated interface to the processor pipeline, making it ideal for extending the processor's execution unit with custom hardware accelerators.

FPU Enable

As a hardware feature, the Floating Point Unit (FPU) provides better performance compared with implementing floating point in software. The single-precision FPU is based on IEEE Std 754, significantly improving the single-precision floating point performance of the application while significantly increasing the size of the MicroBlaze processor instantiation.

Low Power Mode

This mode is supported through the SLEEP instruction. After all outstanding transactions on any MicroBlaze processor interface have been completed, SLEEP stops the MicroBlaze processor from executing further instructions and causes it to enter a sleep state.

Hardware Multiplier and Divider Enable

A hardware integer multiplier/divider feature can be enabled in the MicroBlaze processor, allowing instructions to multiply and divide 32- or 64-bit operands in hardware. This implementation is much faster than a software-only approach.

Lockstep Interface

The lockstep interface is one of the key features implemented in the MicroBlaze processor used to facilitate fault-tolerant system design. The processor core is able to operate in lockstep configuration, where two or more identical MicroBlaze processor cores execute the same program. By comparing the outputs of the cores, any tampering attempts, transient faults, or permanent

hardware failures can be detected. A typical use case of this feature enables tamper protection, as shown in Figure 2. Lockstep operation also provides the basis for implementing triple modular redundancy using a MicroBlaze processor core.

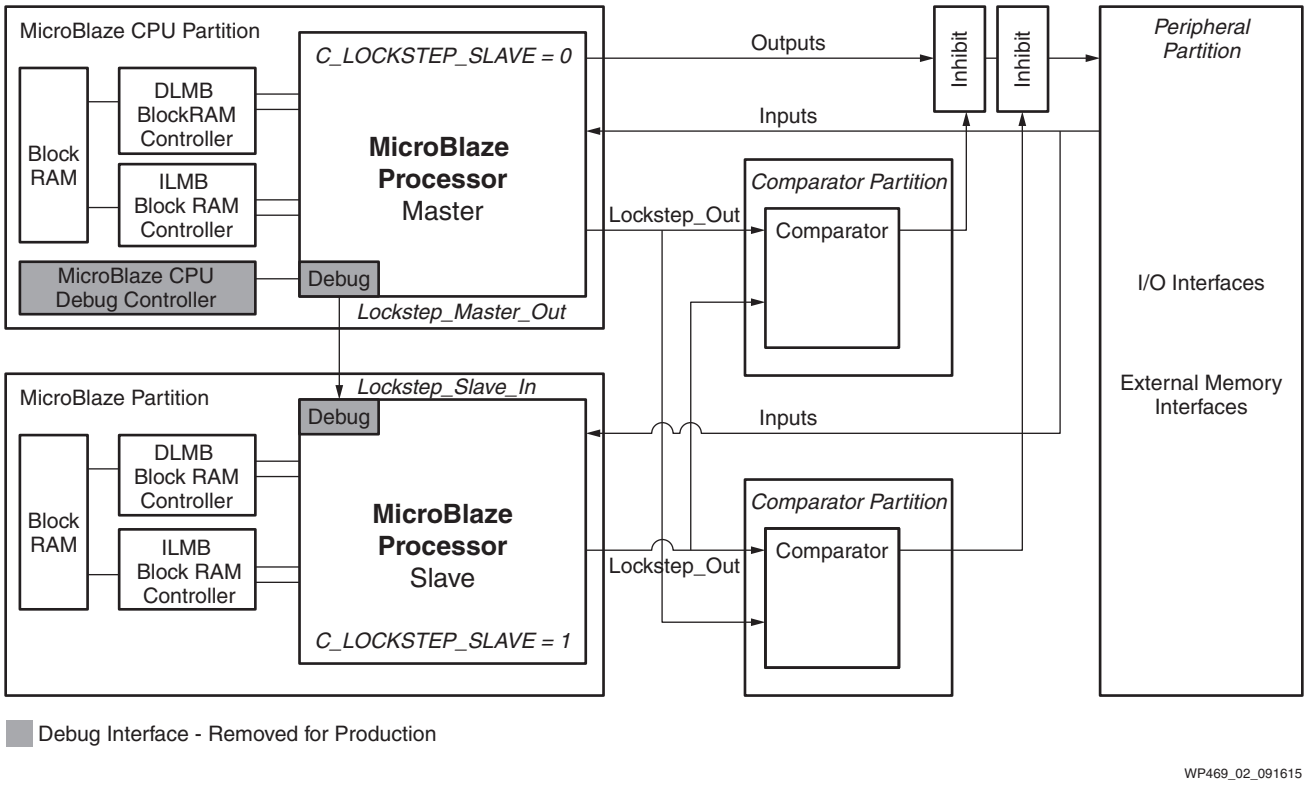

Figure 2: **MicroBlaze Processor in Lockstep Mode for a Fault Tolerant Operation**

Debug Support

This option enables the download and debug of programs using Xilinx System Debugger (XSDB). With this option, a user can employ XSDB to debug the processor over the JTAG boundary-scan interface. This feature can be used only during development for debug; it is disabled in the production design to reduce the size of the MicroBlaze processor.

The basic mode enables the debug module to interface with the MicroBlaze processor for debugging purposes. Multiple instances of the MicroBlaze processor can be interfaced with a single debug module to enable multiprocessor debugging. The extended mode makes the enhanced debug features of the MicroBlaze processor available, such as cross-trigger, trace, and profiling.

Performance Monitoring

With extended debugging, the MicroBlaze processor provides performance monitoring counters to count various events and to measure latency during program execution.

Fault Tolerance

The fault tolerance features included in the MicroBlaze processor provide Error Detection for internal block RAMs and support for Error Detection and Correction (ECC) in LMB block RAMs. When fault tolerance is enabled, all soft errors in block RAMs are detected and corrected, which significantly reduces overall failure intensity. Instruction and Data Cache Protection, Memory Management Unit Protection, and Exception Handling features are also supported.

MicroBlaze Processor Performance

To achieve maximum performance, the user can operate the MicroBlaze processor in the Performance Optimized configuration. Table 2 shows that the performance of 7 series and Zynq devices using Vivado Design Suite 2015.1 have approximately a 1.4X improvement over Spartan-6 devices using the ISE® Embedded Design Suite. The processor performance in Table 2 is based on three different configurations:

- Maximized performance using a 5-stage pipeline model *with* branch optimization
- Maximized performance using a 5-stage pipeline model *without* branch optimization
- Minimized area using a 3-stage pipeline model

Table 2: **MicroBlaze Processor Performance Benchmarks**

Product Family (-3 Speed Grade)	Performance Optimized *with* Branch Optimization		Performance Optimized *without* Branch Optimization		Area Optimized	
	F_{MAX} (MHz)	DMIPS	F_{MAX} (MHz)	DMIPS	F_{MAX} (MHz)	DMIPS
Zynq-7000 (1)	173	249	224	300	214	229
Virtex-7 (2)	246	354	343	460	303	324
Kintex-7 (2)	241	347	337	452	303	324
Artix-7 (2)	173	249	224	300	214	229
Spartan-6 (3)	130	174	150	195	135	145

Notes:

1. Zynq-7000 devices based on Artix-7 FPGA fabric in Z-7010, Z-7015, and Z-7020 devices
2. 7 series devices based on Vivado Design Suite 2015.1
3. Spartan-6 devices based on ISE Embedded Design Suite 14.7

Leveraging the MicroBlaze Soft Processor with Xilinx Low-End Portfolio Devices

To derive the best performance, a capable soft processor core needs to be coupled with the right silicon. The Xilinx All Programmable Low-End Portfolio delivers the broadest, most cost-effective solution for diverse requirements. Each device family delivers the best value for its target applications:

- **Spartan-6 FPGA:** With best-in-class I/O ratios and form factor, the Spartan-6 family is ideal for simple to moderately complex bridging applications or companion co-processing chips commonly found in infotainment, consumer, and industrial automation. The MicroBlaze processor can be optimized to complement existing or preferred host processors for rapid extension of system interfaces, peripherals, or processing capabilities with minimal development effort.

- **Artix-7 FPGA:** For FPGA applications that demand more advanced functionality, the 28nm-based Artix-7 family offers exceptional performance per watt. The Artix-7 family leads the industry in nearly every aspect of performance in a low-end device, including logic fabric performance, memory line rates, signal processing bandwidth, and particularly transceiver line rates. With 30% greater processor performance than Spartan-6 FPGAs due to fabric, and support for more advanced serial protocols like PCIe® Gen2 and JESD204B, Artix-7 devices can be leveraged for more advanced embedded tasks.
- **Zynq-7000 AP SoC:** For applications that demand the robust processing power of a dual-core ARM Cortex-A9 processor, the low-end Zynq-7000 AP SoC devices (Z-7010, Z-7015, and Z-7020) provide the highest level of system integration of the three families by fusing an ARM APU subsystem with the Artix-7 device fabric. Multiple MicroBlaze processor cores can be implemented in the fabric and co-exist with the Cortex-A9 as a form of offloading less demanding tasks, such as system management and input monitoring.

As shown in Figure 3, these three product families ensure that designers can select from a diverse set of capabilities over a broad range of densities for their cost-sensitive end applications.

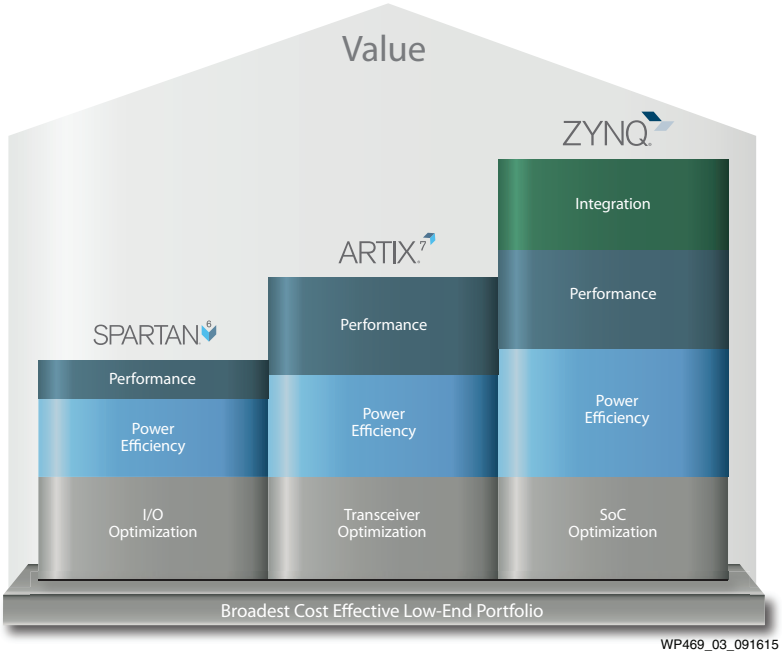

Figure 3: **Xilinx Low-End Portfolio Value**

Embedded Development Tools and Plug-and-Play IPs

In cost-sensitive, high-volume markets, where time-to-market is of the highest importance, selecting a suitable programmable device and embedded processor is critical. Designers need to consider efficiency and ease-of-use of the supporting tools and IP for a complete embedded design development solution.

Vivado Design Suite: Integrated Design Environment

The Vivado Design Suite implements an SoC-strength next-generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation. With full support for MicroBlaze processor development, the Vivado Design Suite provides a completely integrated software development environment, seamless design and integration with IP Integrator (IPI), and rapid design creation for optimal performance and area results.

Intelligent IP Integration with Vivado IPI

Built on the foundation of the Vivado Integrated Design Environment (IDE), the IPI feature provides an interactive device- and platform-aware environment that supports intelligent auto-connection of key IP interfaces, one-click IP subsystem generation, real-time DRCs, and interface change propagation, all supported by a powerful debug capability. For MicroBlaze processor-based embedded systems, multiple interfaces need to be connected with various peripheral IPs such as Ethernet, USB, and PCIe, among others, and to memory devices such as DDR. Care needs to be taken when connecting multiple masters and multiple slaves to ensure careful matching of address, data width, and interrupt connections.

SDK: Software Development and Debug

SDK is the Xilinx Integrated Design Environment (IDE) for creating embedded applications on the MicroBlaze soft processor, as well as for the Zynq-7000 AP SoC. SDK is the first application IDE to deliver true homogeneous (multiple MicroBlaze processors) and heterogeneous multi-processor design and debug (ARM Cortex-A9 plus MicroBlaze processor). SDK is included with the Vivado Design Suite, but is also uniquely available as a separate free download for embedded software developers. Based on Eclipse, it directly interfaces to the Vivado embedded hardware design environment. SDK supports complete software design and debug flows and includes an editor, compilers, build tools, flash memory management, JTAG System Debugger/GDB debug integration, and a full suite of libraries and device drivers.

Plug-and-Play IP Catalog

As today's designs integrate increasing amounts of functionality, designers must have access to proven, up-to-date, easy-to-use IP from reliable sources to accelerate their design cycles. The Plug-and-Play IP initiative is the Xilinx response to the growing customer demand for system-level design support when using multiple IP cores from various internal and third-party sources.

Plug-and-Play IP cores from Xilinx and its Alliance Program members meet this demand by providing simple yet powerful capabilities that significantly improve designer productivity. The Plug-and-Play environment enables design teams to create complex systems with minimal effort. The user also has the ability to create their own custom IP with AXI interface using the Create and Package IP utility in the Vivado design tools that they can connect to the MicroBlaze processor.

To ensure portability and interoperability among IP offerings from Xilinx and its Alliance members, Xilinx has taken a standards-based approach to delivering proven, easy-to-use IP cores. The three critical standards that enable the development of Plug-and-Play IP are:

- The AMBA® AXI™4 interconnect protocol, developed in conjunction with ARM
- The IEEE P1735 encryption and rights-management standard for design IP
- The IP-XACT XML Schema specifying IP metadata and interconnection from Accellera, based on IEEE Std 1685-2009

Xilinx has raised Plug-and-Play IP to the next productivity level by leveraging key industry standards and by adding major ease-of use improvements and other enhancements to the Vivado Design Suite's intelligent integration feature, IP Integrator.

Accelerating Embedded System Development

Embedded systems are complex. Hardware and software portions of an embedded design are extensive projects in themselves. Merging the two design components so that they function as one system creates additional challenges. Add configurable logic to the mix, and the design project becomes complicated. Complexity can slow down the pace of design development and implementation, and can increase the likelihood of fundamental design errors going undetected until late in the project.

To simplify the design process, Xilinx offers the Vivado Design Suite, which is a fully integrated hardware development tool that includes Vivado IPI for quick system development using the MicroBlaze processor core with plug-and-play IPs. Xilinx also offers SDK for software development and debug. This set of tools provides the user with everything needed to simplify and accelerate embedded system development for bare-metal as well as for Linux development. This includes hardware and software application design, debug, code execution, and transfer of the design onto actual boards for verification and validation.

Figure 4 shows typical hardware and software design flow and hand-off.

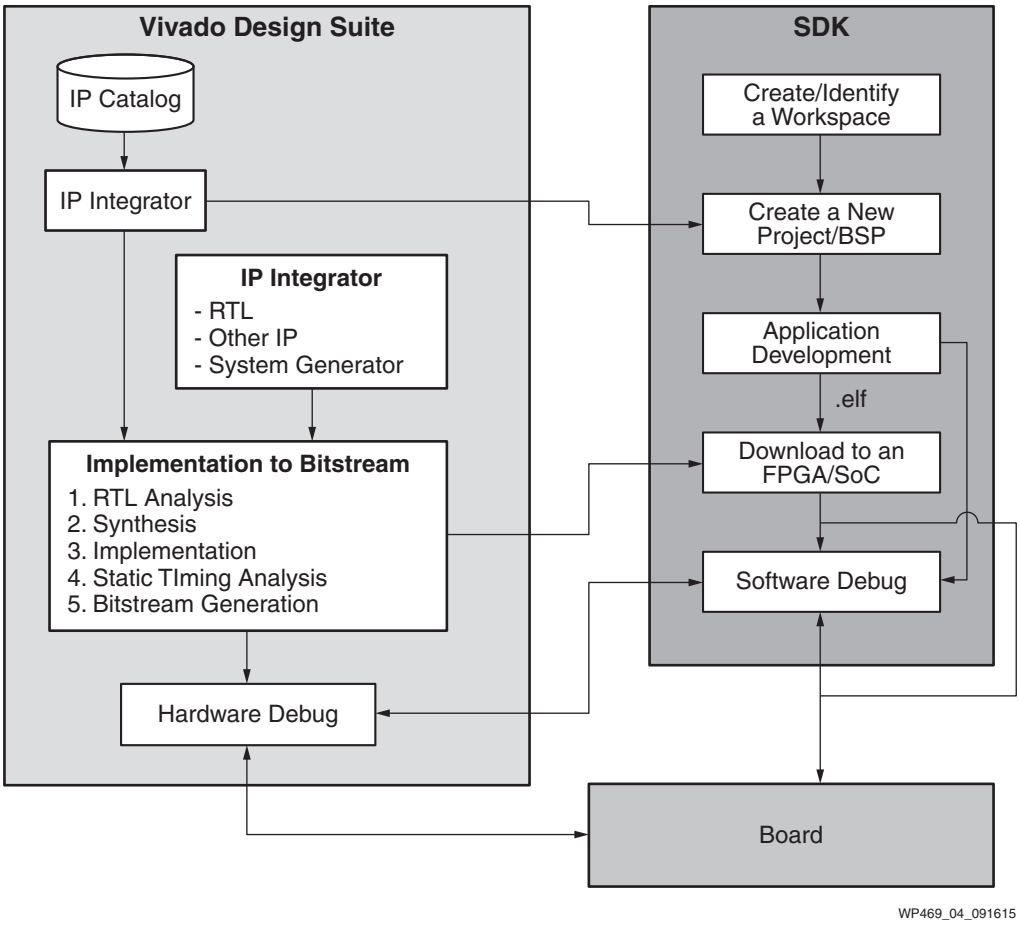

Figure 4: **Embedded System Development Flow and Hand-off**

IP connectivity is correct-by-construction. Working at the interface level, design teams can rapidly assemble complex systems and leverage Vivado tools to ensure that designs and IP are configured correctly. The built-in automated IPI interface, device driver, and address map generation capability accelerate assembly of the design.

Leveraging the extensible IP catalog, IPI provides automated IP subsystem generation. As an example, to generate a MicroBlaze subsystem, a designer selects the MicroBlaze core, drag and drops it into the design, and then uses the IPI built-in block generation feature and one-click IP customization to rapidly configure the interconnect, peripherals, memory map, and device driver. Doing all these tasks through a streamlined user interface increases designer productivity.

Vivado IPI also provides features for block and connection automation. After using these options and some manual iterations, the user can complete the hardware design, as shown in Figure 5.

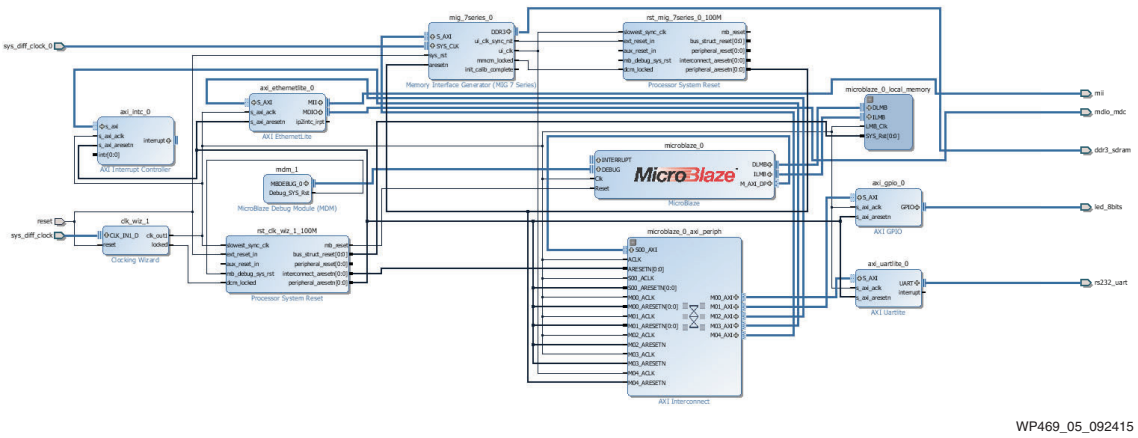

Figure 5: **Vivado IPI-Based Design Block Diagram**

Once the hardware design is complete, the user can generate a bitstream and export the hardware to SDK for software development and debug. The SDK screen shot in Figure 6 shows a few key features.

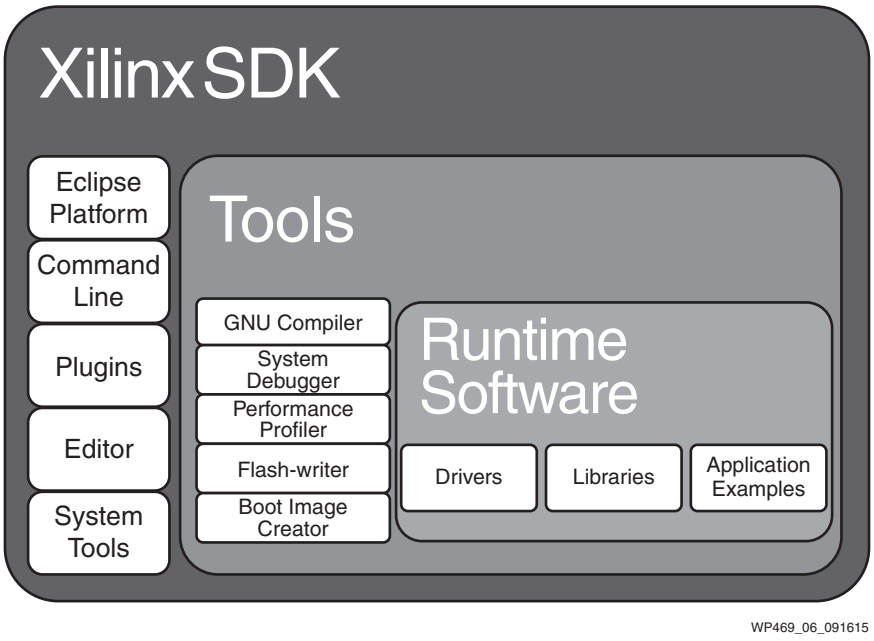

Figure 6: **SDK Screen Shot**

SDK is used to develop Linux and bare-metal applications. Xilinx provides project templates for the Board Support Package, Boot Loader, C/C++, Memory, and Peripheral Tests. SDK automatically deploys to the target, connects the debugger, and begins program execution. This works with both Cortex A9 and MicroBlaze targets.

Using the IP- and system-centric Vivado Design Suite and Eclipse-based SDK Integrated Design Environment, a user can develop embedded systems faster, accelerating overall development time.

Conclusion

Xilinx offers a comprehensive embedded solution consisting of the MicroBlaze embedded processor, AXI4-based Plug-and-Play IPs, bare-metal and Linux device drivers, and Vivado IPI and SDK tools that help customers build embedded applications faster. This reduces the overall development time for hardware, firmware, and application software. Customers can download the Vivado Design Suite edition and start developing MicroBlaze-based embedded designs. These development environments are also supported with a free web-pack edition with device lock support.

For additional details on the Xilinx All Programmable Low End Portfolio and MicroBlaze soft processor core, visit the Xilinx website. Some useful starting points are given in the Additional Information section.

Additional Information

Xilinx MicroBlaze Processor landing page:
http://www.xilinx.com/tools/microblaze.htm

Xilinx Embedded Computing landing page:
http://www.xilinx.com/products/design-tools/software-zone/embedded-computing.html

Artix-7 FPGA A35T Kit landing page:
www.xilinx.com/arty

Xilinx Spartan-6 FPGA landing page:
http://www.xilinx.com/products/silicon-devices/fpga/spartan-6.html

Xilinx Artix-7 FPGA landing page:
http://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

Xilinx Zynq-7000 AP SoC landing page:
http://www.xilinx.com/products/silicon-devices/soc/zynq-7000.html

Xilinx User Guide UG940, *Vivado Design Suite Tutorial: Embedded Processor Hardware Design*

Xilinx White Paper WP460, *Reducing System BOM Cost with Xilinx's Low-End Portfolio*

Xilinx Application Note XAPP584, *Spartan-6 FPGA Dual-Lockstep MicroBlaze Processor with Isolation Design Flow*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/28/2015	1.0	Initial Xilinx release.

Disclaimer

Automotive Applications Disclaimer