VLSI PROJECT
8x4 SRAM Designing and Simulation

Appendix

Name	UFID
Cortland P Bailey	**61933919**
Rujuta D Vaze	**99354820**
Sharayu P Sabane	**91284785**
Sri Vivek Nalamothu	**40023881**

Work Distribution

SRAM cell : Rujuta D Vaze

Rujuta was responsible for designing the SRAM cell circuitry. She has successfully completed the designing schematic,layout and symbol for the schematic, and testing the circuitry. Rujuta was also responsible for designing the layout for 8*4 6T_SRAM array.

Row/Column Decoder : Cortland P Bailey

Cortland was responsible for designing the row and column decoders circuitry. This includes the schematic, making the layout, designing a symbol for the schematic, and testing the circuitry. Cortland was responsible for writing the final Report.

Read/Write circuit : Sharayu P Sabane

Sharayu was responsible for designing the circuits for Read and Write operations. This includes the schematic, making the layout, designing a symbol for the schematic, and testing the circuitry. Sharayu was responsible for integrating all components together in schematic and performing simulations for testing Read and Write operations. .

Sense Amplifier : Sri Vivek Nalamothu

Vivek was responsible for designing the sense amplifier. This includes the schematic, making the layout, designing a symbol for the schematic, and testing the circuitry. He was also responsible for making the appendix for the final report submission.

Results/Simulations screenshots:

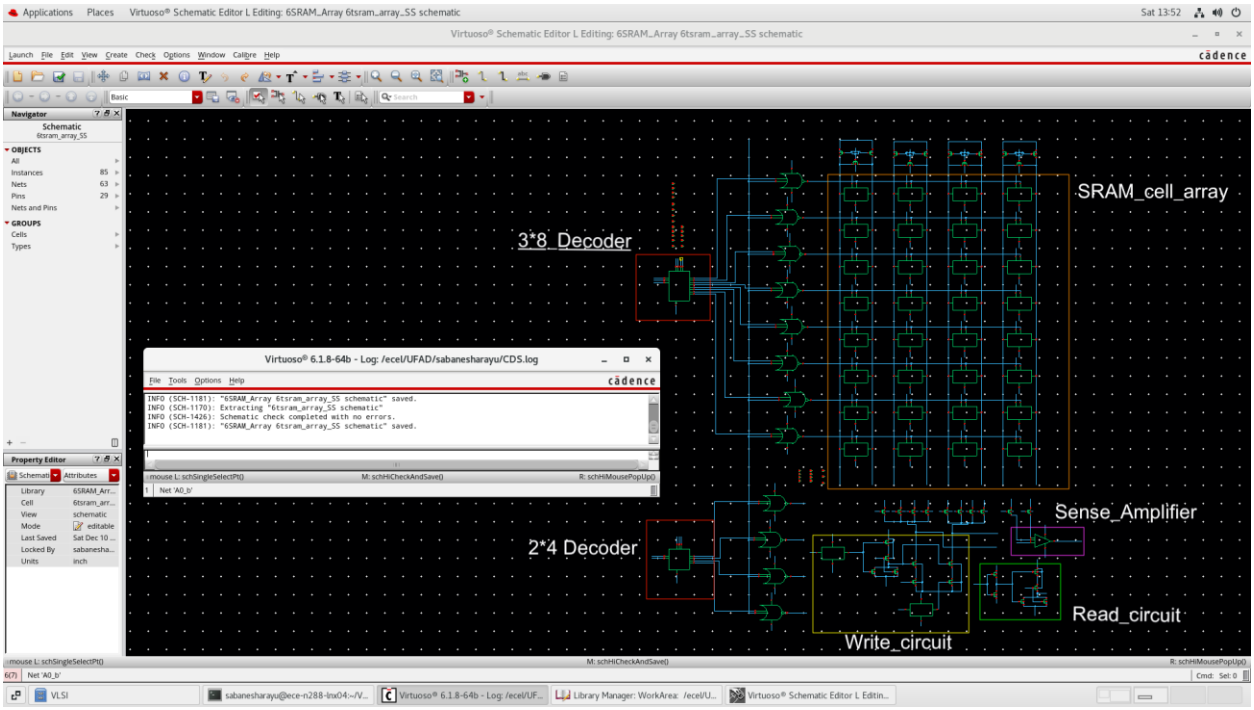

Fig 1: 8x4 SRAM Array Schematic

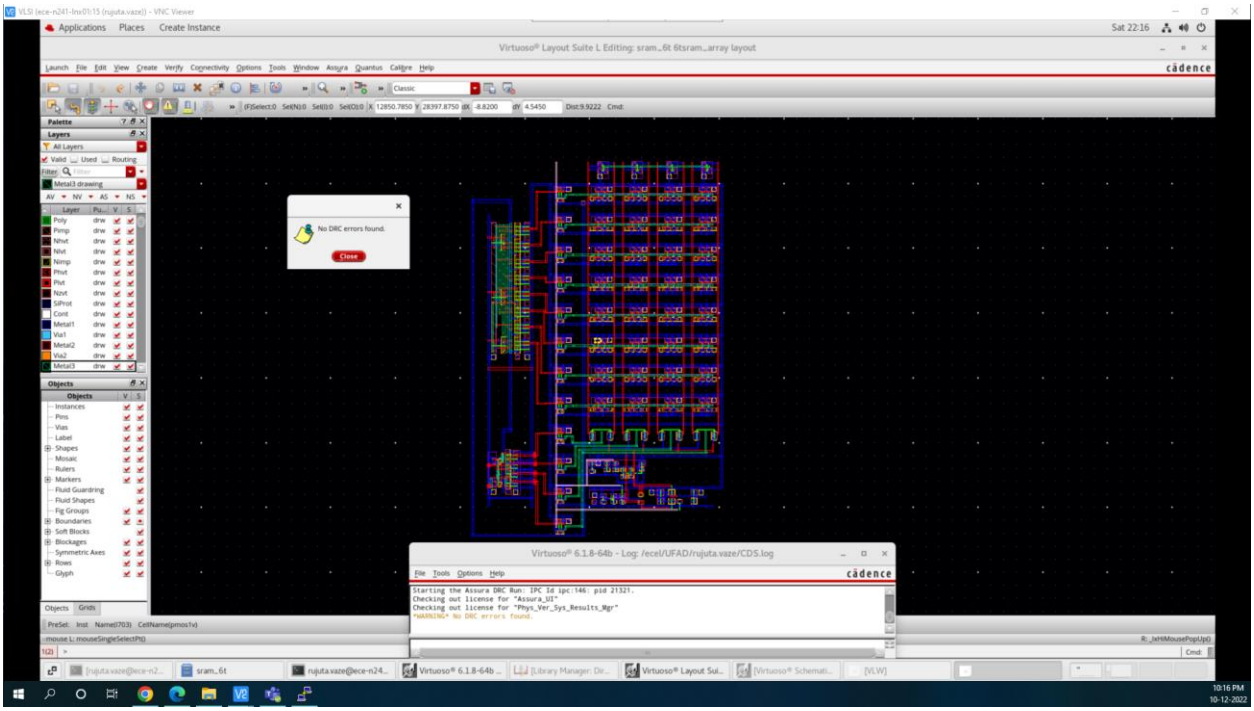

Fig 2: 8x4 SRAM Array Layout - w/DRC check

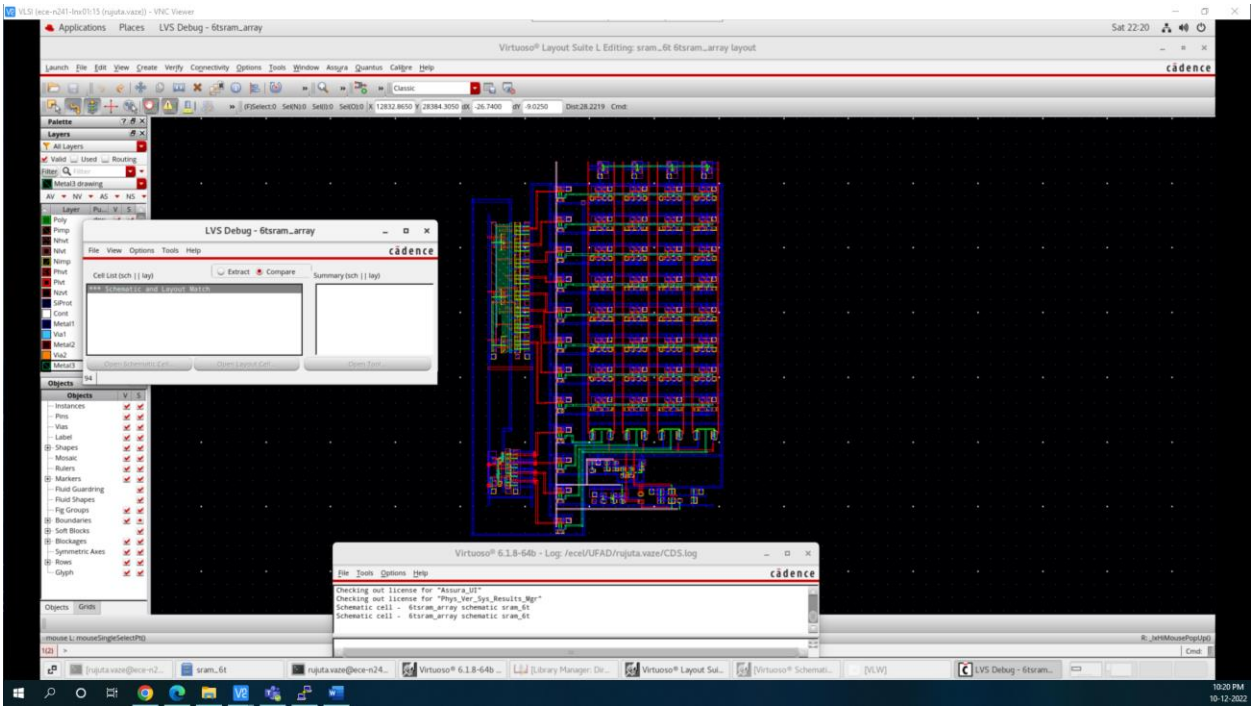

Fig 3: 8x4 SRAM Array Layout - w/LVS check

Fig 4: SRAM Simulation - Write ‘0’ to Address “00000”

Fig 5: SRAM Simulation - Write ‘0’ and ‘1’ to multiple Addresses: “10001”, “00000”, “00001”

Fig 6: SRAM Simulation - Write ‘0’ and ‘1’ to multiple Addresses: “01000”, “1000”, “11000”

Fig 7: Write_1 & Read_1 and Write_0 & Read_0 on SRAM Simulation -

Fig 8: SRAM Simulation - Read '1' from multiple Addresses

Fig 9: SRAM Simulation - Precharge Time

Fig 10: SRAM Simulation - Precharge Time

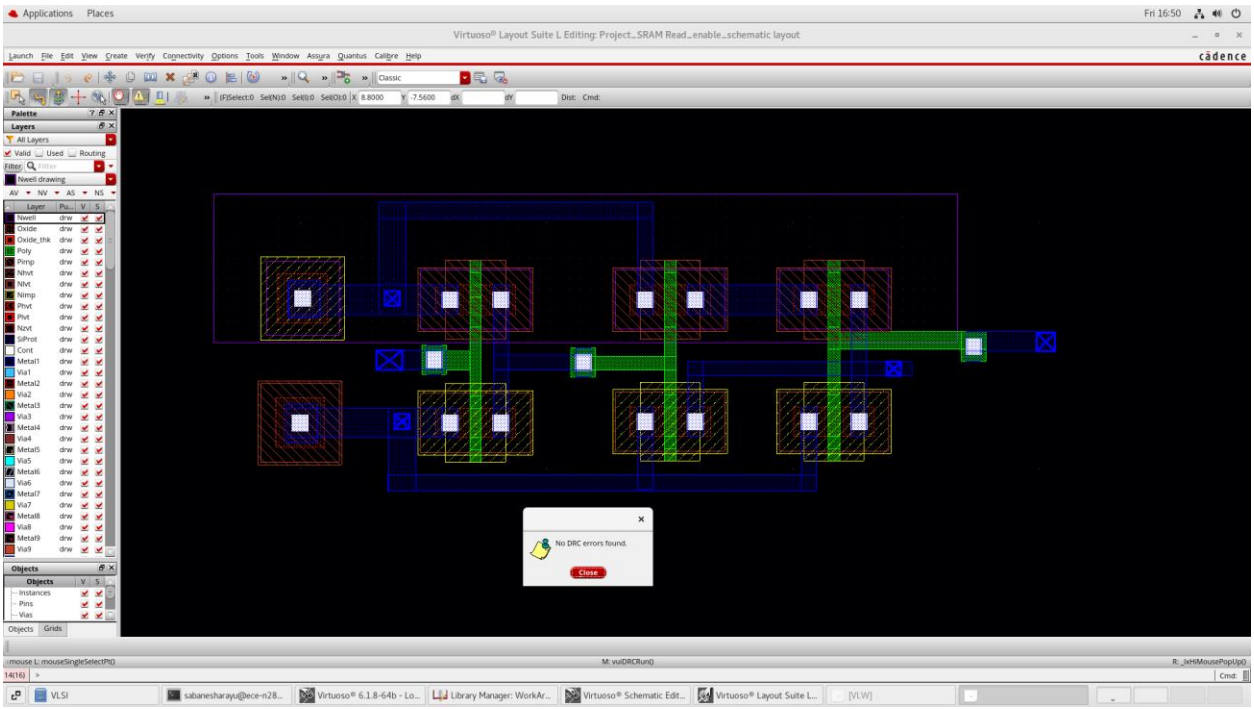

Fig 11: SRAM Read Enable layout w/ DRC

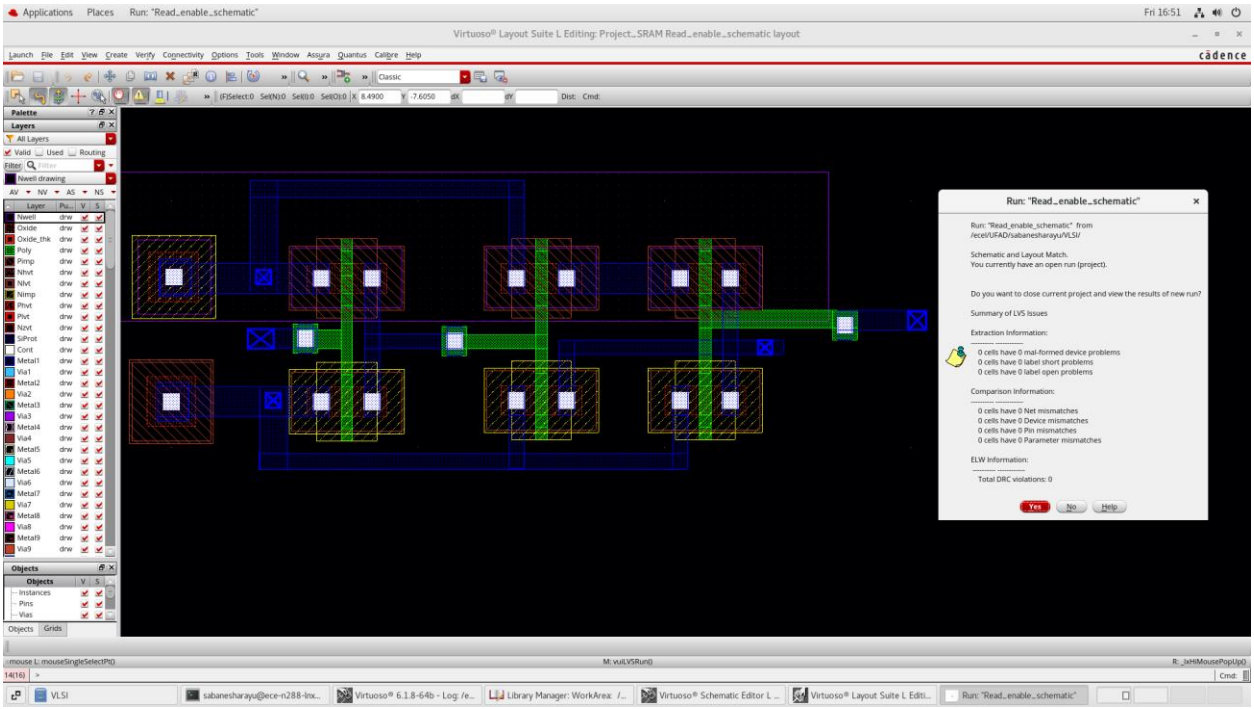

Fig 12: SRAM Read Enable layout w/ LVS

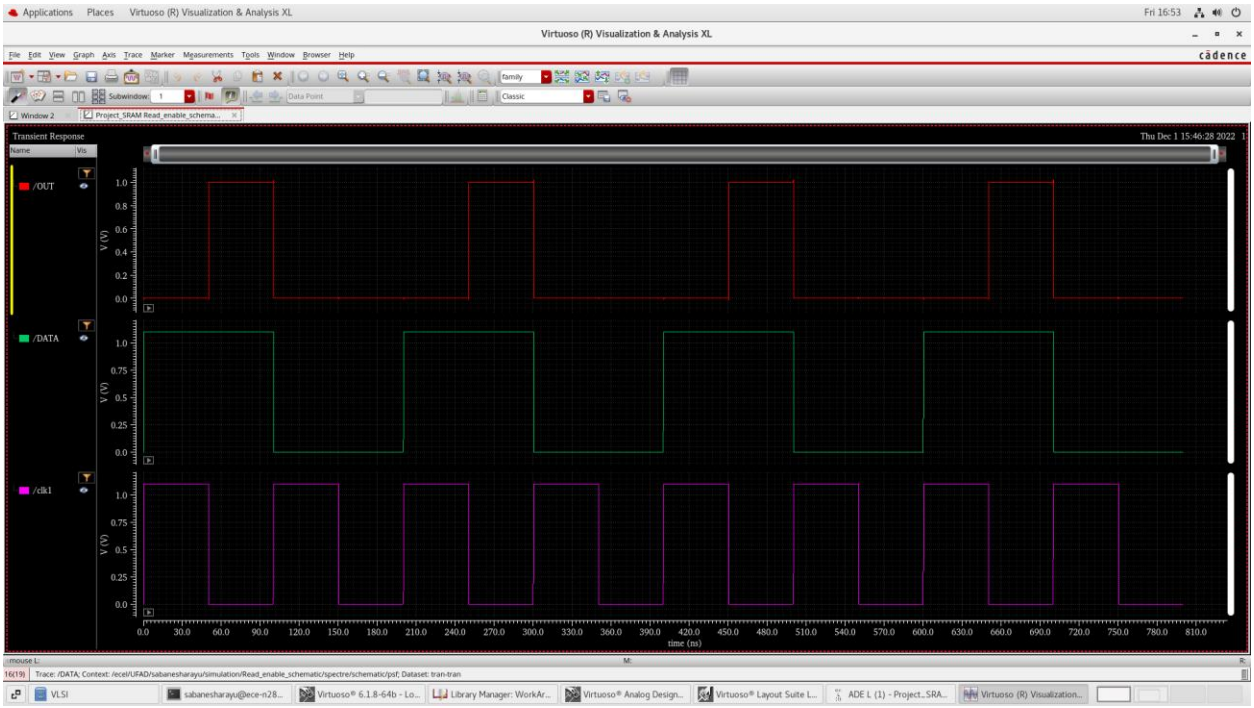

Fig 13: SRAM Read Enable simulation

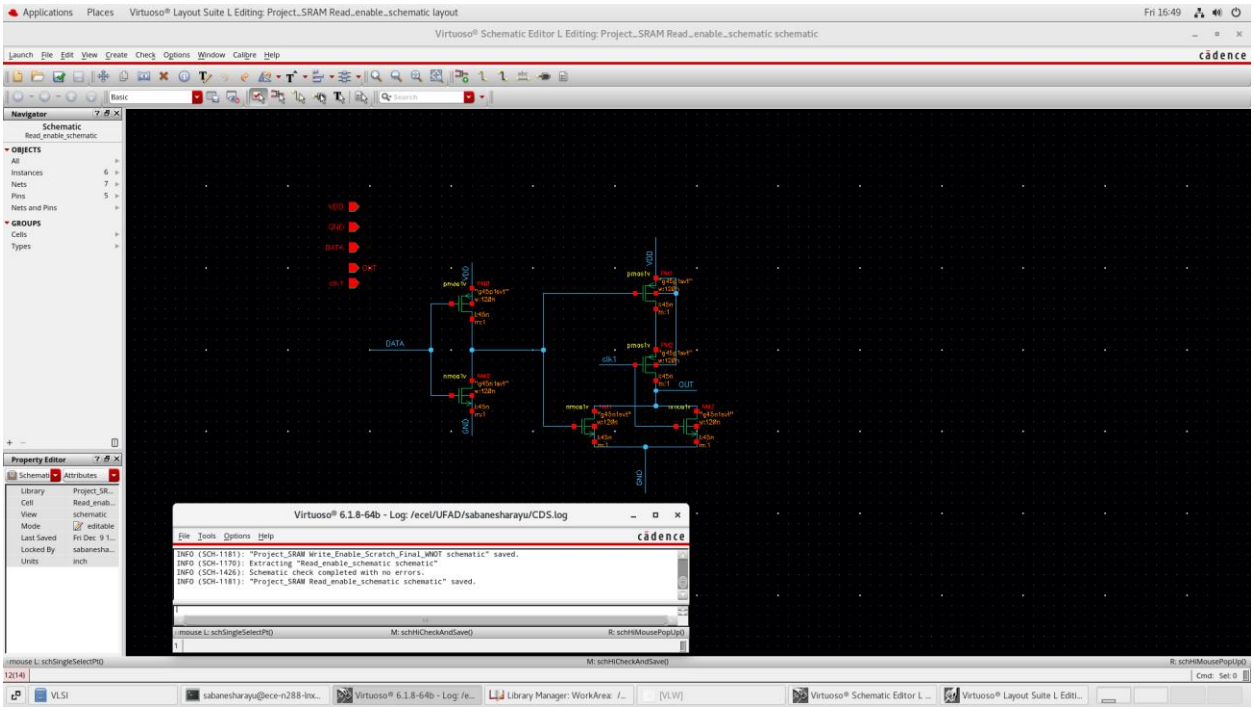

Fig 14: SRAM Read Enable schematic

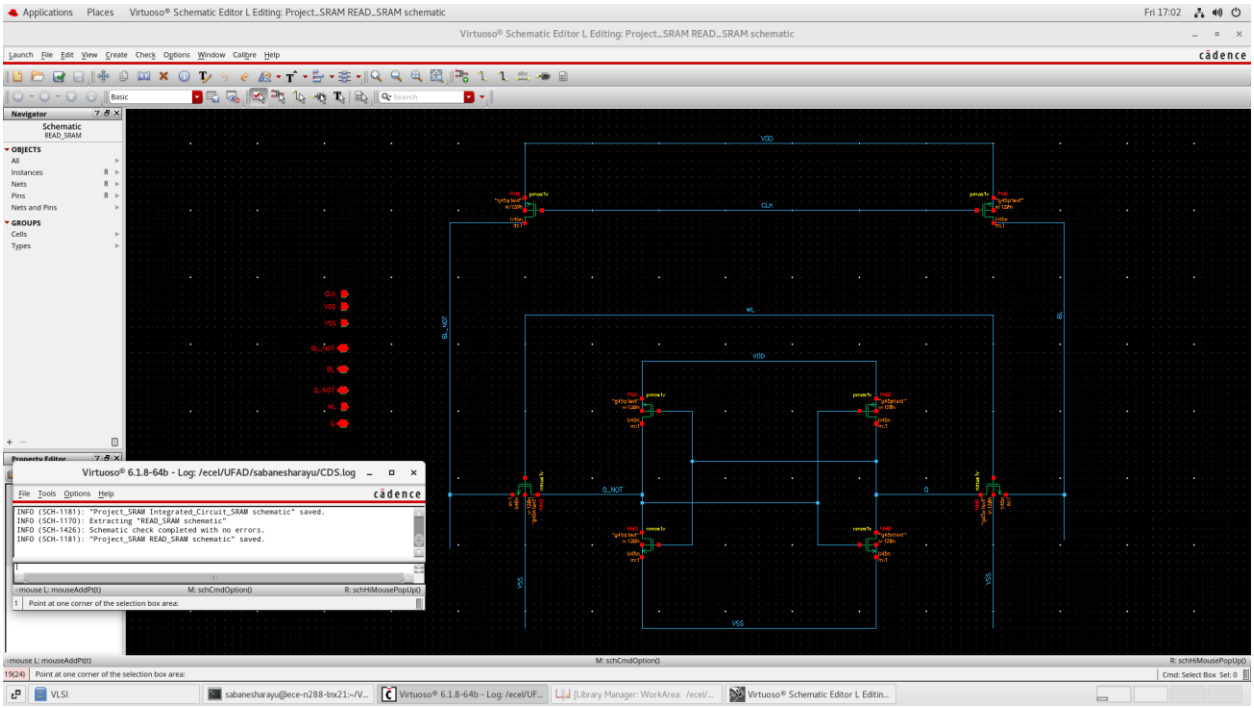

Fig 15: SRAM 6T Cell Schematic

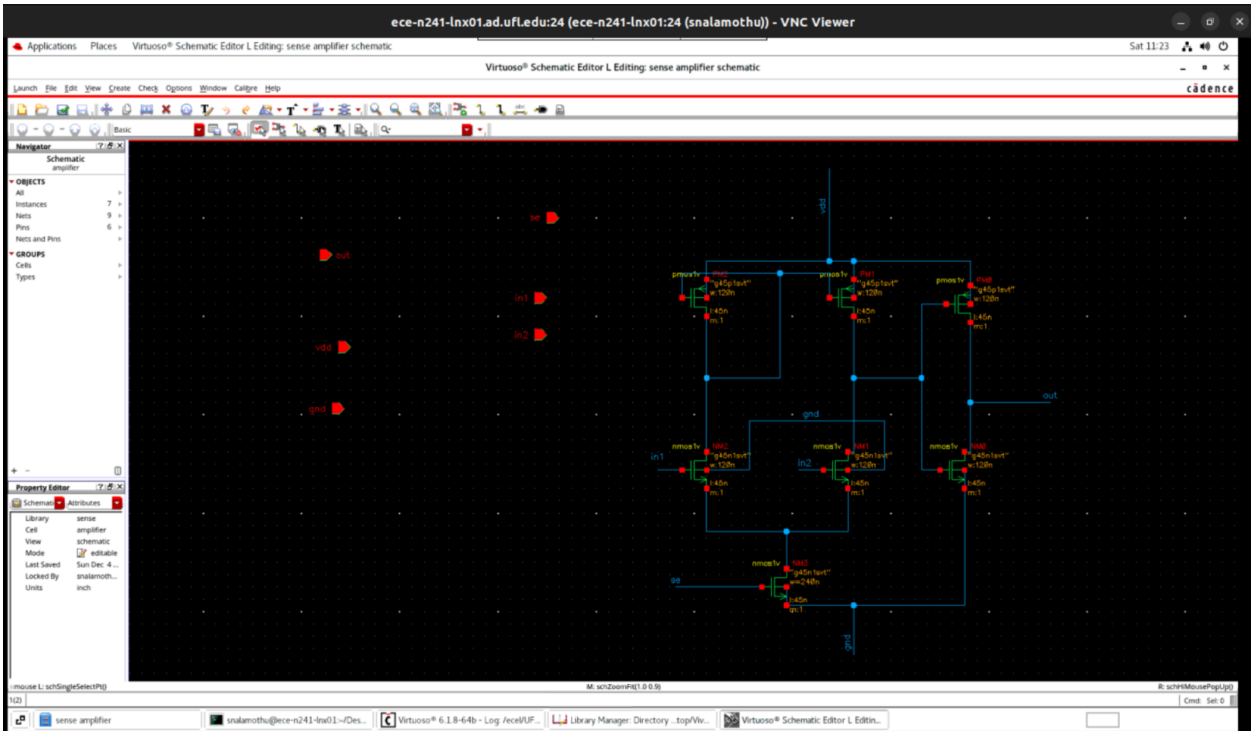

Fig 16 : SRAM Sense Amplifier Schematic

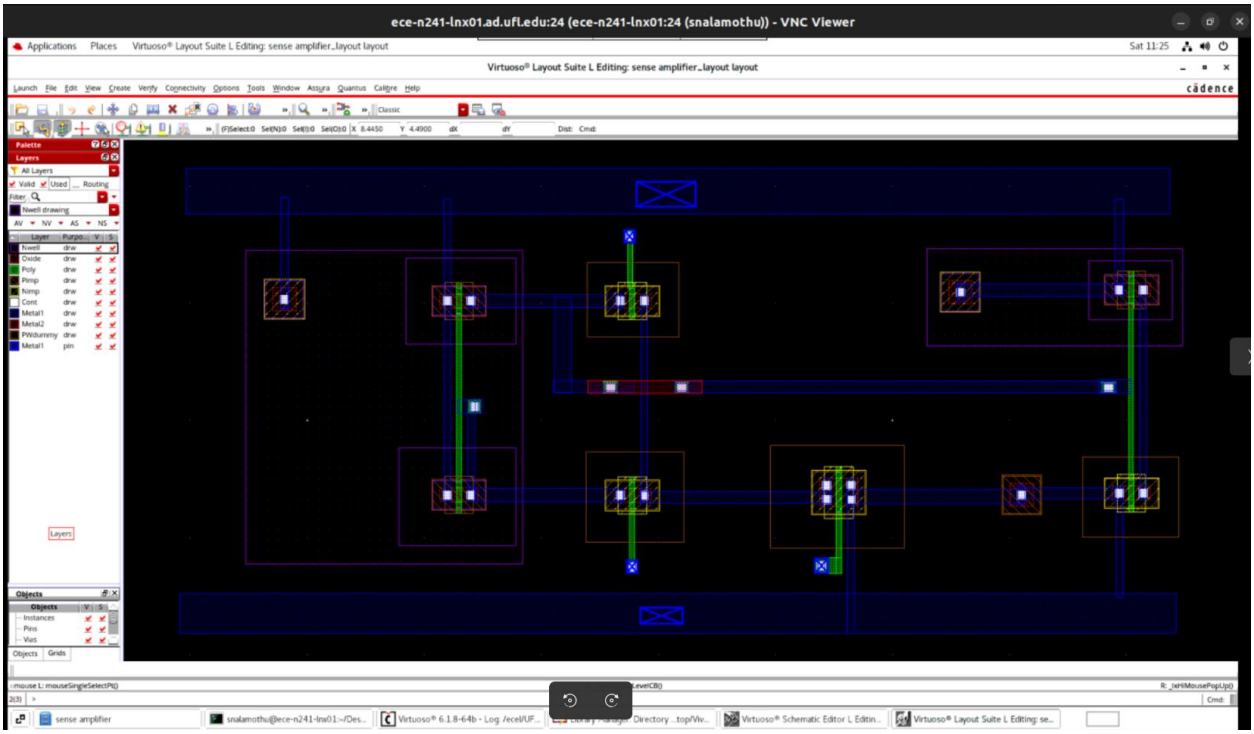

Fig 17 : SRAM Sense Amplifier Layout with 0 DRC

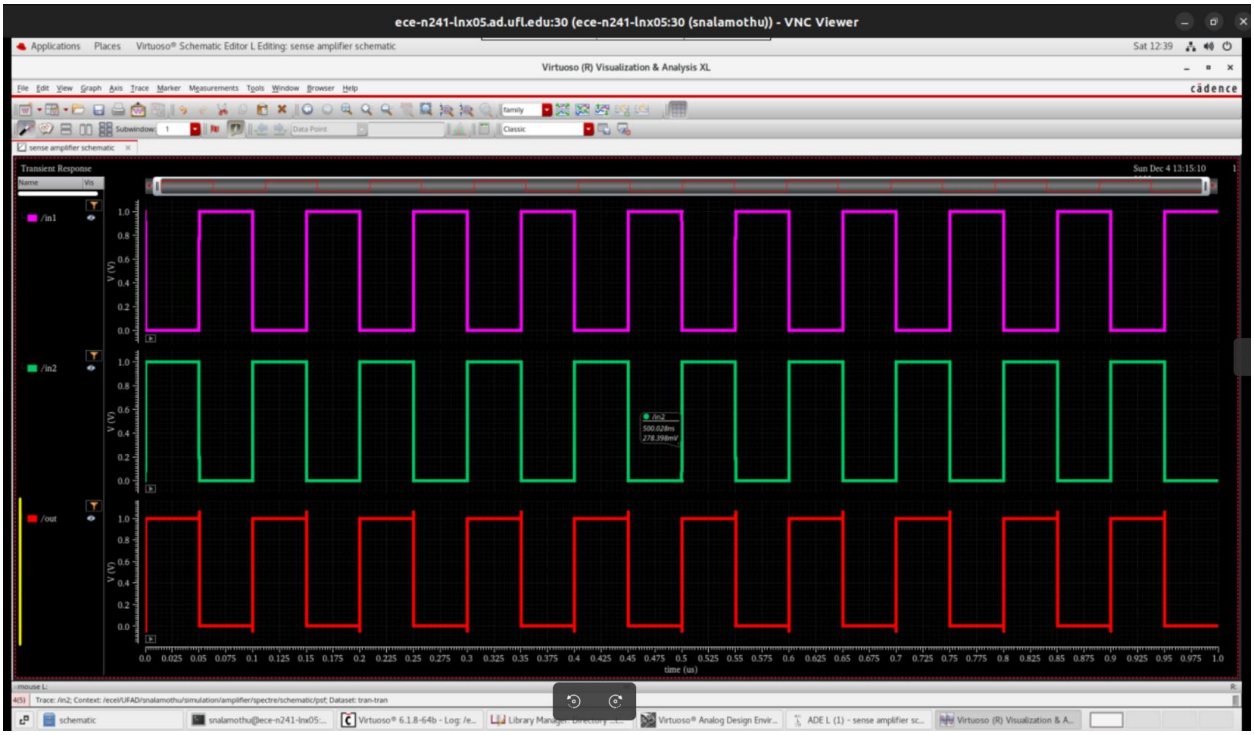

Fig 18: SRAM Sense Amplifier Simulation