Designing and Simulation of 8*4 6T-SRAM

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***Abstract*— The majority of the equipment we frequently use advances technologically every day. Devices are getting smaller while using less power and operating more effectively. Consequently, there is a greater need for smaller, more efficient chips. This research uses 45nm technology to construct an 8*4 SRAM with six transistors. We used Cadence and the "gpdk045 library" from the Cadence library to design a layout and characterize a 6T-SRAM.**

Keywords*— *Row/Column-Decoder, SRAM, Read, Write, sense amplifier, schematic, layout.

I. INTRODUCTION

Six-transistor SRAM is static random-access memory (SRAM). The two types of memories are volatile memory and non-volatile memory. Non-volatile memory is static and can hold data even in the absence of power, which is the main distinction between the two types of memory. While data can be stored in volatile memory until a power source is present. Both SRAM and DRAM are non-volatile memories. However, the majority of logic chips use SRAM instead of DRAM, which employs one transistor to store each bit of data. The cause is that DRAM has a unique technology flow, making it challenging to produce on the same logic device. This report includes an illustrated explanation of the schematic design process for an 8*4(32-bit) SRAM. Detailed information about designing and simulation is mentioned in the following report. In the report that follows, specific information on designing and simulation is presented.

II. DESIGNING OF EACH COMPONENT

The designing of an SRAM memory on cadence involves schematics and layout. We have used Assura DRC and Assura LVS to validate designs.

A. 6T-SRAM

The 6T-SRAM bitcell consists of six transistors, one worldline (WL), and two-bit lines (BL and BL_BAR) which carry complementary data. When the WL is high, a bit of data can be written or read by the SRAM bitcell. The bit lines are used as both input and output terminals. The six internal transistors consist of two pass-gate transistors, two pull-up transistors and two pull-down driver transistors.

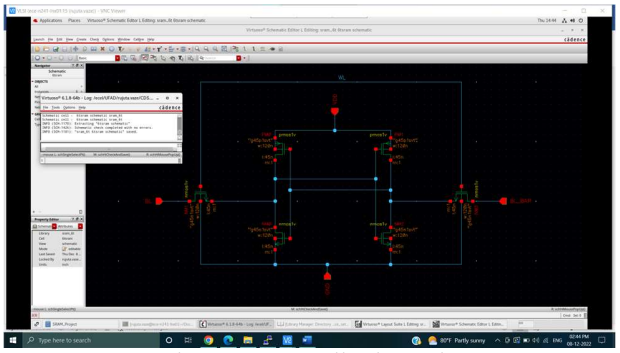

Fig 1: SRAM cell schematic

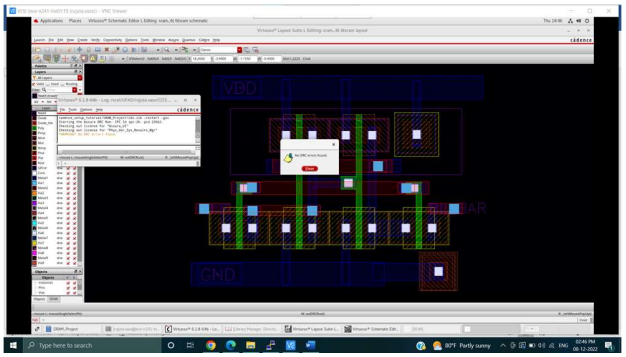

Fig 2: SRAM Cell Layout with 0 DRC Errors

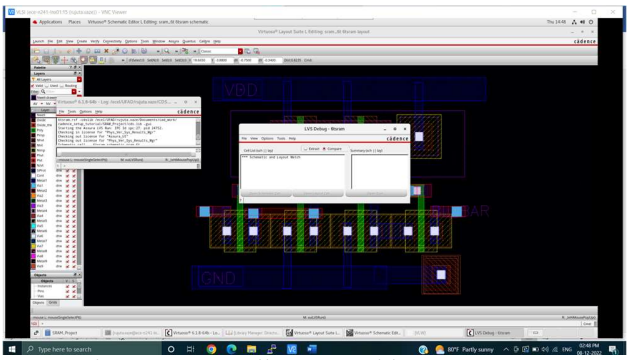

Fig 3: SRAM Cell Layout with 0 LVS Errors

B. Column/Row Decoder circuit:

The Column and Row Decoders are responsible for interpreting a given Address signal and decoding which of the SRAM Cells to read or write to. These circuits are constructed with inverters

and NAND gates alone, and are “active low”. Active low circuits output a HIGH (“1”) when the signal is not active, and a LOW(“0”) when it is activated. They are arranged in such a way to activate only one of the output bits for any given input.

- 3 to 8 Decoder - Row Decoder: Cadence was used to create the schematic and layout of the Row Decoder. Images are shown below.

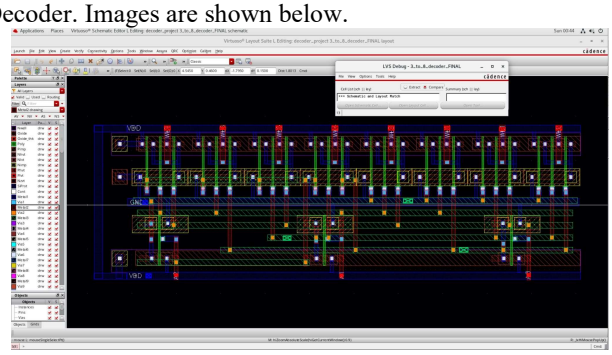

Fig 4_a: 3-8 Decoder (Row) Layout with LVS

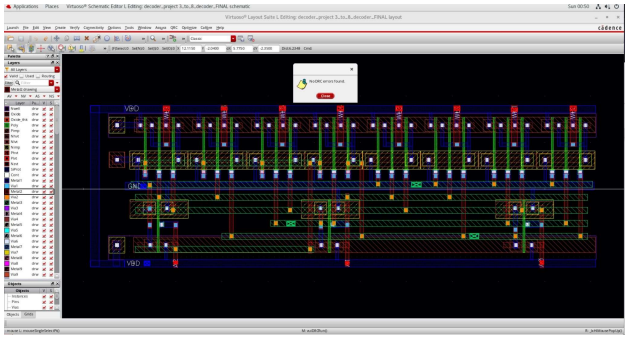

Fig 4_b: 3-8 Decoder (Row) Layout with DRC

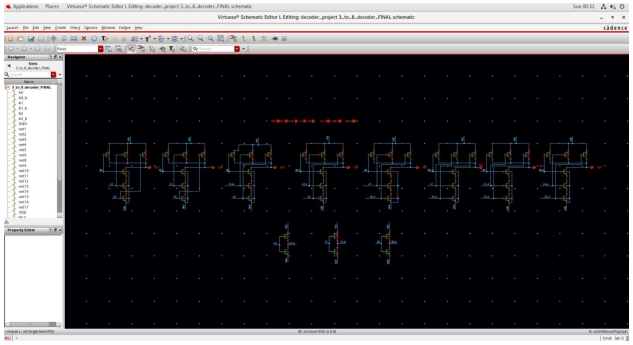

Fig 5: 3-8 Decoder (Row) Schematic

- 2 to 4 Decoder - Column Decoder: Cadence was used to create the schematic and layout of the Column Decoder. Images are shown below.

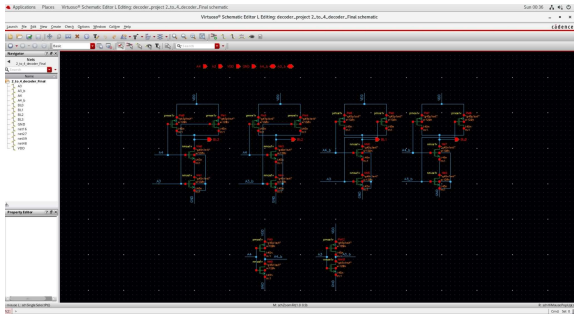

Fig 6: 2-4 Decoder (Column) Schematic

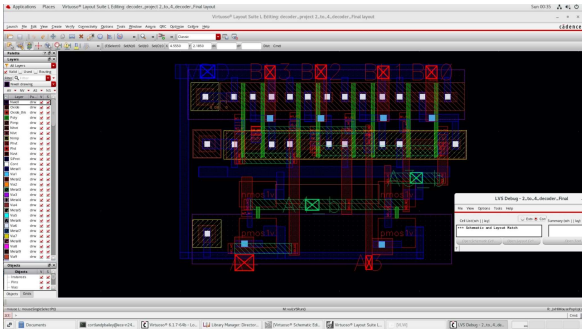

Fig 7_a: 2-4 Decoder (Column) Layout with LVS

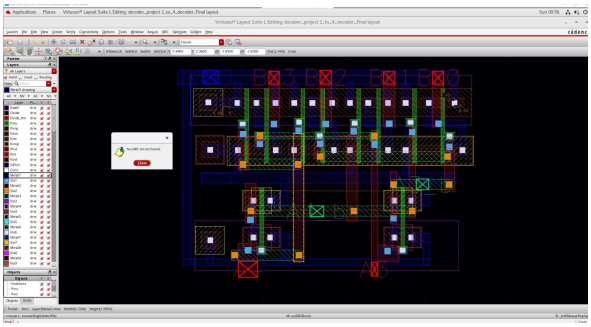

Fig 7_b: 2-4 Decoder (Column) Layout with DRC

C. Read-Write circuit:

The layout of the Column/Row-Decoder and the entire 6T-SRAM array circuitry determines how the Read-Write circuitry functions. This report's decoder operates on an active low, or "0." An inverter, a NOR gate, and 4 transistors with a 4X total width make up the write circuit. The transistors that aid in pulling down node Q are also present, along with the buffer circuit. The read circuit has an Inverter followed by a NOR gate and 2 transistors.

- Write Circuit:

Cadence was used in the schematic and layout design of the write circuit. The layout and schematic images are shown below.

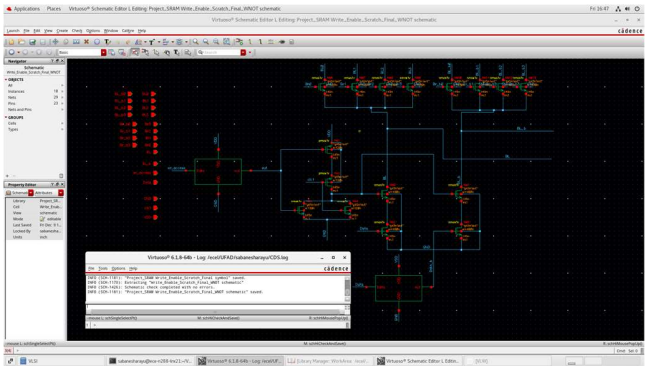

Fig 8: Write Schematic

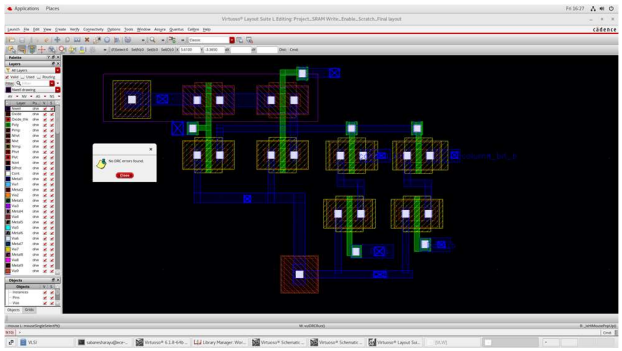

Fig 9a: Layout of Write with 0 DRC error

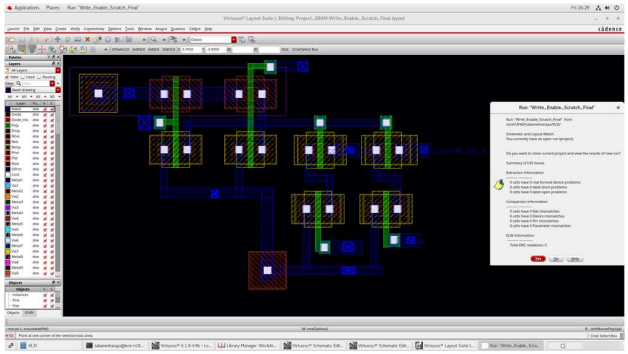

Fig 9b: LVS of Write circuit

- Read Circuit:

The layout and schematic images are shown below.

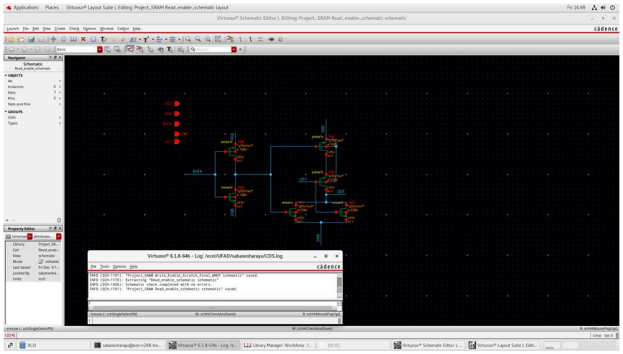

Fig 10: Read Schematic

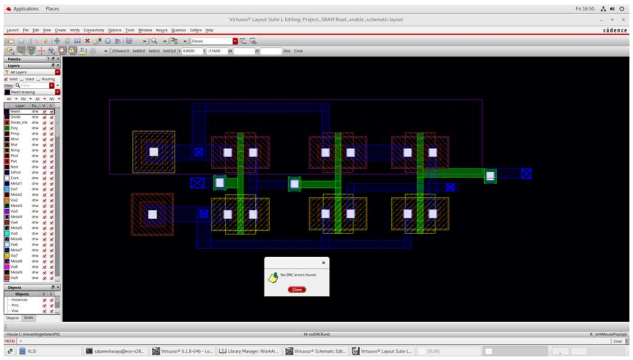

Fig 11a: Layout of Read with 0 DRC error

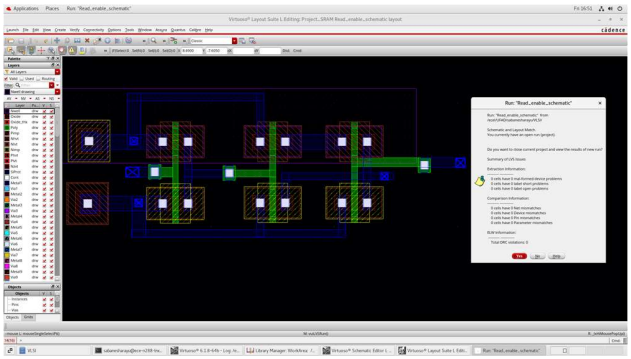

Fig 11b: LVS of Read circuit

D. Sense Amplifier:

During a read cycle, the sensing amplifier is in charge of determining the value that is stored in an SRAM cell and displaying it at the output. Each column of cells in the SRAM array only needs one sensing amplifier since each read cycle only accesses one row of data.

Any small variation between bit and bitline bar, represented by the numbers in1 and in2 in the schematic, would result in a differential voltage driven by a bigger nmos, where se is the gate voltage of the transistor.

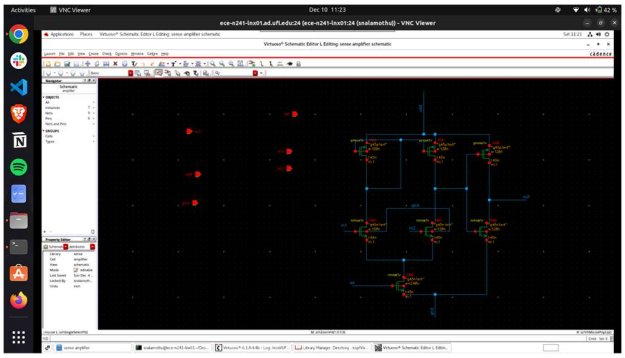

Fig 12 : Sense Amplifier Schematic

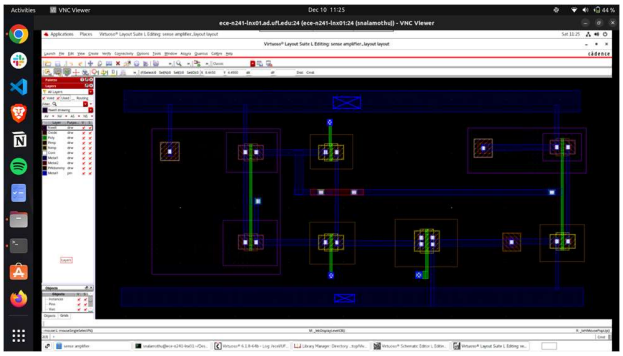

Fig 13 : Sense Amplifier Layout with 0 DRC errors

E. Pre-charge:

The two bit-lines are charged using the pre-charge circuit. Set to high before switching to float. The initial stage in executing read and write operations is pre-charging.

Fig 14: Precharge Circuit Schematic

*F. 8*4 6T-SRAM full array:*

The full array of SRAM has each row/column decoder output connected to one SRAM cell in the row and column of the full array. Since we are using a decoder that operates on active low, we need to add a buffer. We are using NOR as a buffer throughout the SRAM. The bit lines are fed to 8 transistors with 4X total width since we need them pulled down for write operation. This is called the write stability criteria.
2 inverters are used at the input of write. The bit lines are further connected to the sense amplifier. The Read circuit along with the buffer is connected to the sense amplifier. Below are screenshots from cadence for a complete schematic with no errors and the layout with 0 DRC and clean LVS.

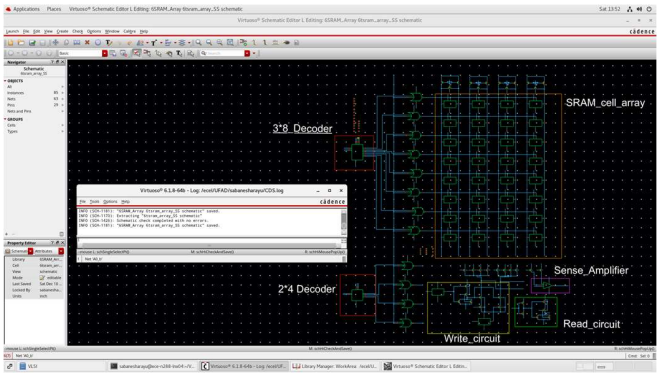

Fig 15: Full-array SRAM Circuit Schematic

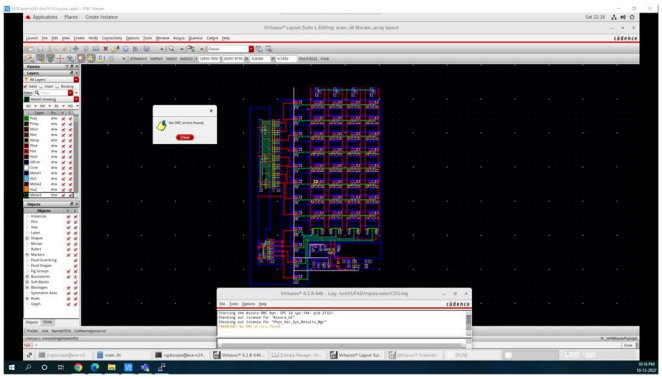

Fig 16: Full-array SRAM Layout with 0-DRC error.

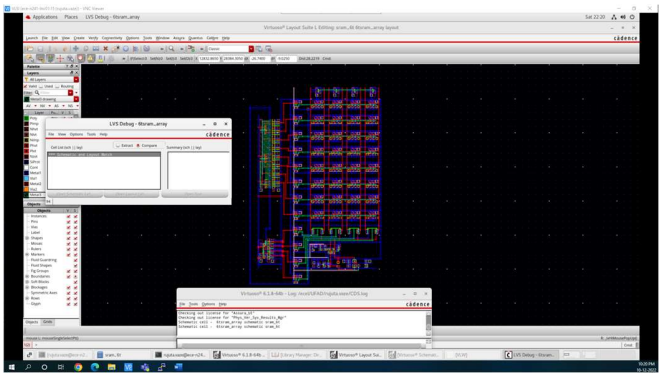

Fig 17: Full-array SRAM Layout with clean LVS

III. TESTING AND SIMULATION OF EACH COMPONENT

To know the correctness of the design we need to perform a few tests and simulations to validate and verify our design of the SRAM array. Below are screenshots from simulations run of cadence.

A. 6T-SRAM Array:

The pre-charge setup must be activated to form write and read operations. The pre-charge setup test included simulation of the pre-charge circuitry by feeding in clock 1 and clock 2.

Pre-charge time is the time required for the circuit to pre-charge the bit lines.

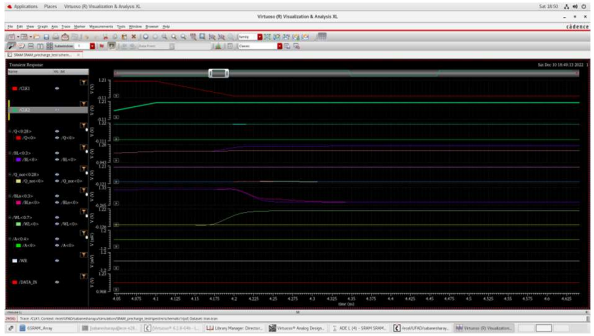

Fig 18: Precharge-setup_Time.

The actual time required to write 0 and 1 on the SRAM are plotted here.

Fig 19: Time for Writing 0.

Fig 20: Write_1 & Read_1 and Write_0 & Read_0 on SRAM.

Fig 19: Read/Write 01 along the column on SRAM.

Fig 20: Reading and Writing 0 1 along the row on SRAM.

B. Read_write Operation:

- Read Operation: Read Operation is performed on "High" WL and the bit lines i.e. BL & BL_b are precharged. SRAM memory initially should have some content to be read. Let's assume memory has Q=1 and Q'=0 as a result. There will be a node voltage Vdd at bit and bit b. There won't be a circuit discharge because Q and bit are both high. Given that Q' is 0, there will be a voltage differential between Q' and the node voltage at bit b, which results in a decrease in bit b voltage.

The sensing amplifier, which also serves as a comparator, is connected to the Bit and bit b. If bit' is low, the output will be 1. As a result, we received an output of 1 and the read operation was validated. Consider Q=0 and Q'=1 in the memory in the same manner. Due to the voltage differential, there will be a discharge in the circuit at Q and bit. The transistors' ratio must be such that Q is below the P2/D2 threshold region. The term for this is read constraint. The output will be zero as bit voltage drops. The result is 0 when the input Q is equal to 0. Therefore, read operation is confirmed in both instances. In the image below, the output waveforms for READ operations are displayed.

RD(input to read circuit)	output from Inverter (Input to NOR)	clk1 (input to NOR)	output from read circuit
X	X	X	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0

Fig 18: Truth Table of Read operation

- Write Operation: Take into account that the memory bits are Q=0 and Q'=1. Since the word line is high at first, writing operations are possible. Bit and Bit' are input lines for the write operation. As we have control over the bit lines, let's first connect bit b to ground in order to measure the voltage between Q' and bit b. D2 must be more powerful than P2 in

order to write 1 into the SRAM cell; this can be done by altering the transistors' aspect ratios. Q will therefore be 1. Q initially equals 0, but after the operation, Q becomes 1, so we successfully write to memory.

WR_access (Input to Write circuit)	Output from Inverter (Input to NOR)	clk1 (Input to NOR)	OUTPUT from write circuit
X	X	X	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0

Fig 19: Truth Table of Write operation

Fig 20: Read operation simulation output.

C. *Column/Row Decoder:*

The logic used for designing of row decoder is given below in the form of a truth table.

clk1	A0	A1	A2	W0	W1	W2	W3	W4	W5	W6	W7
X	X	X	X	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

Fig 21: Truth Table of Row-Decoder

The logic used for designing a column decoder is given below in the form of a truth table.

clk1	A4	A3	BL0	BL1	BL2	BL3
X	X	X	1	1	1	1
0	0	0	0	1	1	1
1	0	1	1	0	1	1
0	1	0	1	1	0	1
1	1	1	1	1	1	0

Fig 22: Truth Table of Column-Decoder

D. *Sense Amplifier*

In the simulation of the sense amplifier for the designed circuit what we observed was the output follows the in2 at every read cycle that depicts the right functionality of the sense amplifier. Inorder to make the output get good levels we have assumed the width of driver nmos twice that of the others.

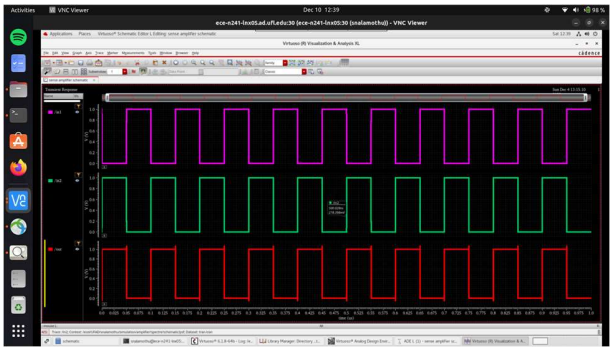

Fig 23 : Simulated graph of Sense Amplifier

IV. Conclusion

A SRAM memory with 8*4 6T-SRAM was designed successfully. The verification and validation of the design was completed successfully using transient simulation at 160 ns period on ADEL lunch in cadence. The optimisation of the design with minimum area and a clean layout was achieved successfully.

V. REFERENCES

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[2] Bhaskar, Akshay. "Design and analysis of low power SRAM cells." *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*. IEEE, 2017.