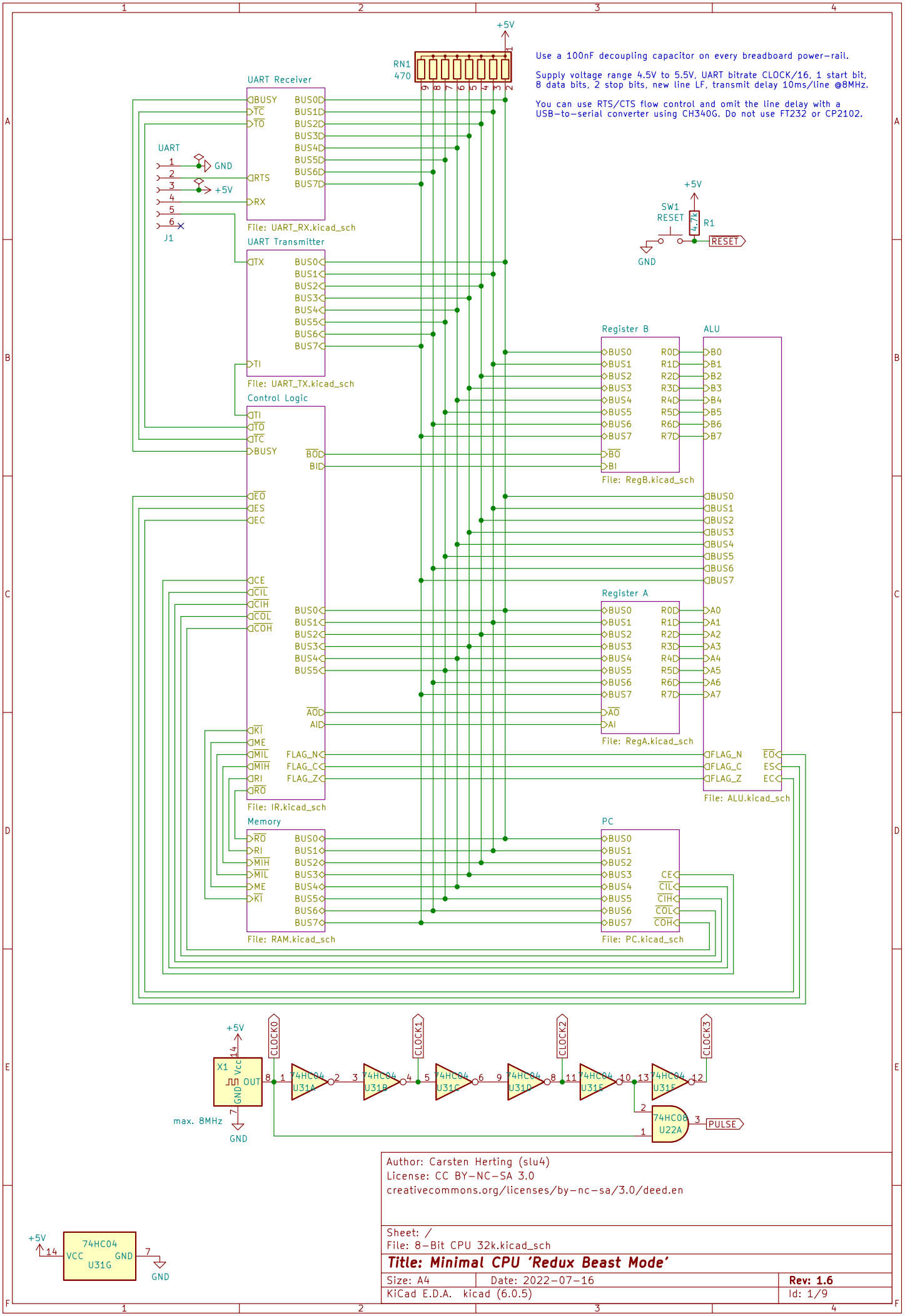
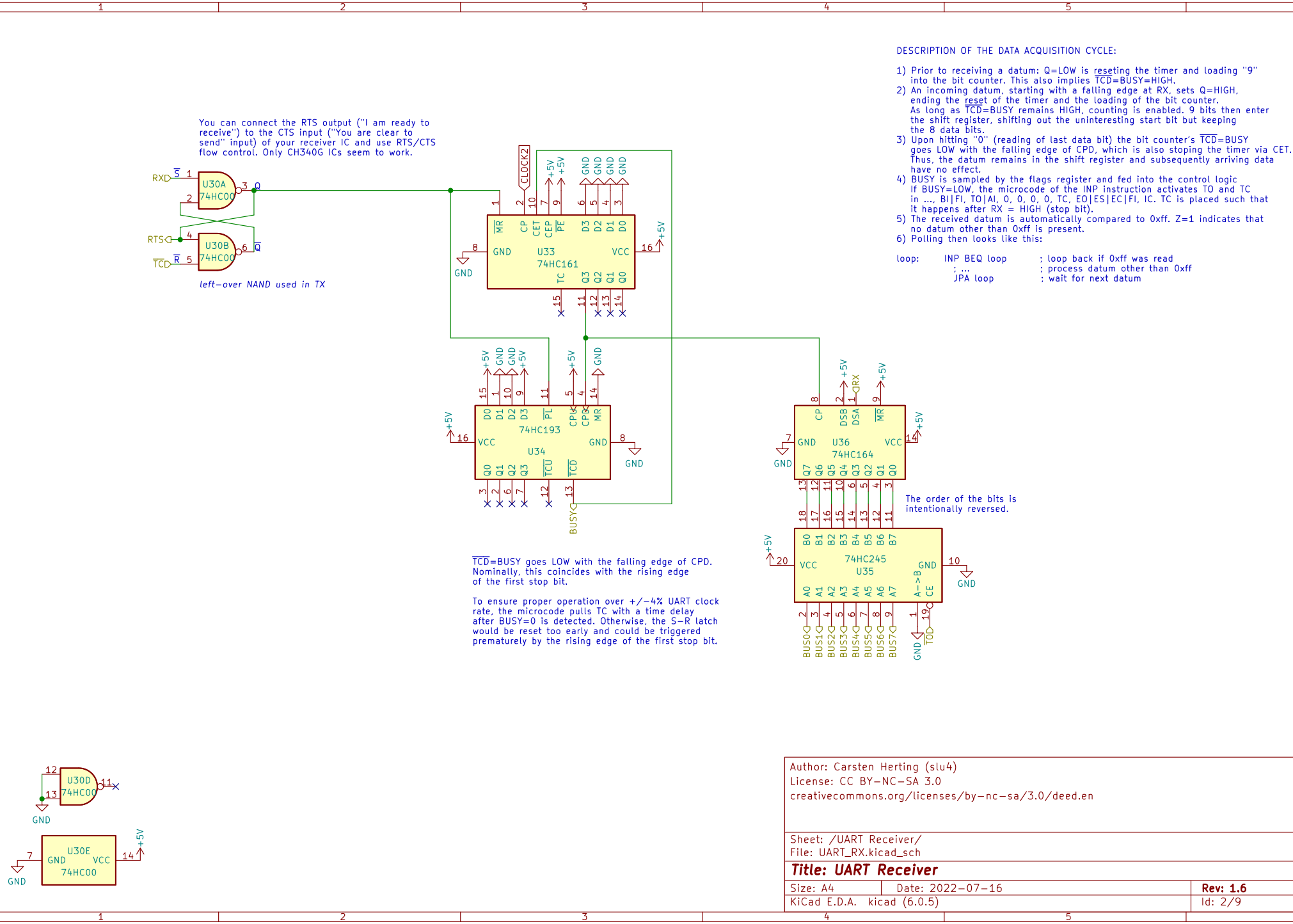

Use a 100nF decoupling capacitor on every breadboard power-rail.
Supply voltage range 4.5V to 5.5V, UART bitrate CLOCK/16, 1 start bit, 8 data bits, 2 stop bits, new line LF, transmit delay 10ms/line @8MHz.
You can use RTS/CTS flow control and omit the line delay with a USB-to-serial converter using CH340G. Do not use FT232 or CP2102.
+5V
RN1
470
UART Receiver
BUSY
TC
TO
RTS
RX
BUS0D
BUS1D
BUS2D
BUS3D
BUS4D
BUS5D
BUS6D
BUS7D
File: UART_RX.kicad_sch
UART
GND
+5V
J1
UART Transmitter
TX
TI
BUS0
BUS1
BUS2
BUS3
BUS4
BUS5
BUS6
BUS7
File: UART_TX.kicad_sch
SW1
RESET
4.7k
R1
RESET
GND
Register B
ALU
R0D
R1D
R2D
R3D
R4D
R5D
R6D
R7D
B0
B1
B2
B3
B4
B5
B6
B7
BO
BI
File: RegB.kicad_sch
Control Logic
TI
TO
TC
BUSY
BOD
BID
EO
ES
EC
CE
CIL
CIH
COL
COH
KI
ME
MIL
MIH
RI
RO
FLAG_N
FLAG_C
FLAG_Z
File: IR.kicad_sch
Register A
A0
A1
A2
A3
A4
A5
A6
A7
AO
AI
File: RegA.kicad_sch
File: ALU.kicad_sch
Memory
File: RAM.kicad_sch
PC
File: PC.kicad_sch
CLOCK0
CLOCK1
CLOCK2
CLOCK3
X1
OUT
max. 8MHz
74HC04
U31A
U31B
U31C
U31D
U31E
U31F
74HC08
U22A
PULSE
Author: Carsten Herting (slu4)
License: CC BY-NC-SA 3.0
creativecommons.org/licenses/by-nc-sa/3.0/deed.en
Sheet: /
File: 8-Bit CPU 32k.kicad_sch
Title: Minimal CPU 'Redux Beast Mode'
Size: A4
Date: 2022-07-16
Rev: 1.6
KiCad E.D.A. kicad (6.0.5)
Id: 1/9

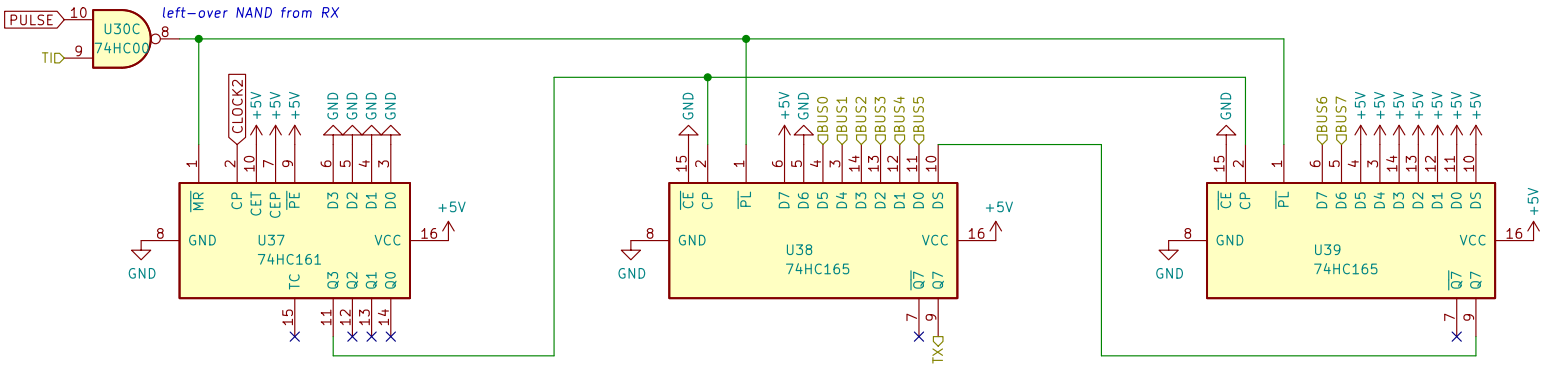





Sheet: /UART Receiver/
File: UART_RX.kicad_sch

**Title: UART Receiver**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 2/9 |

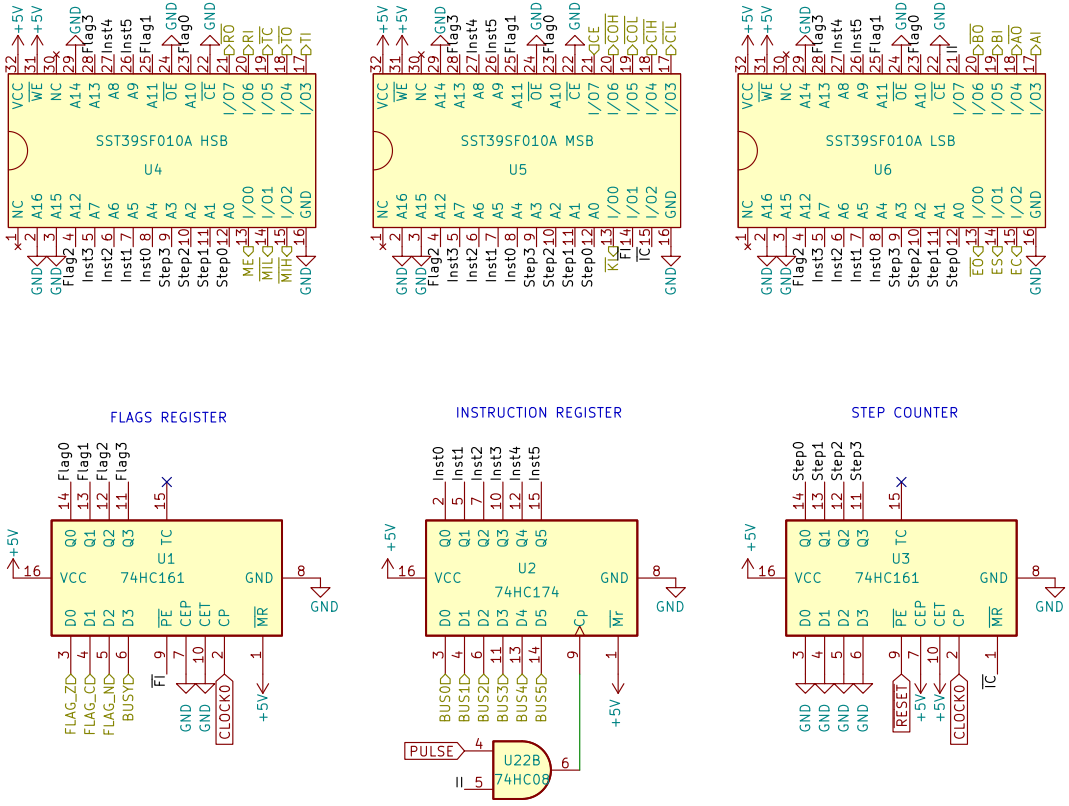





Sheet: /UART Transmitter/
File: UART_TX.kicad_sch

**Title: UART Transmitter**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 3/9 |



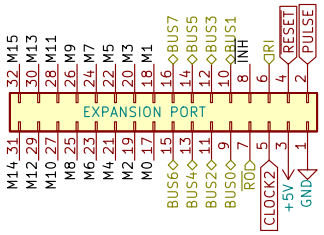


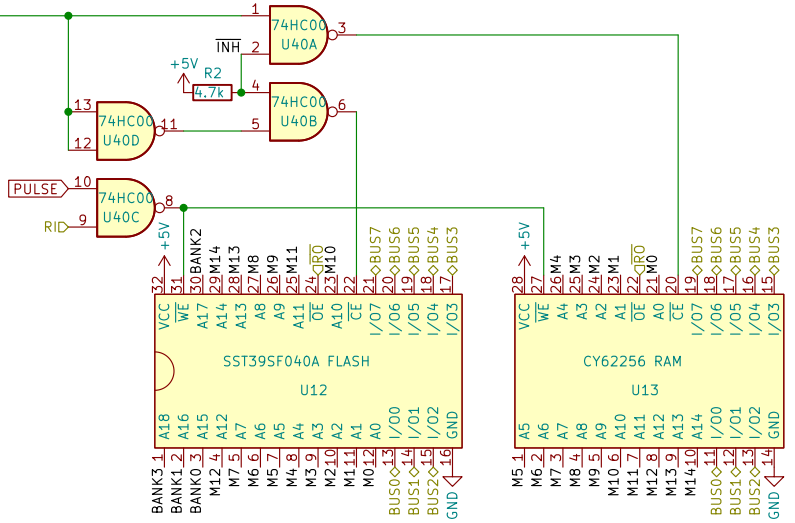

Sheet: /Control Logic/
File: IR.kicad_sch

**Title: Control Logic**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 4/9 |

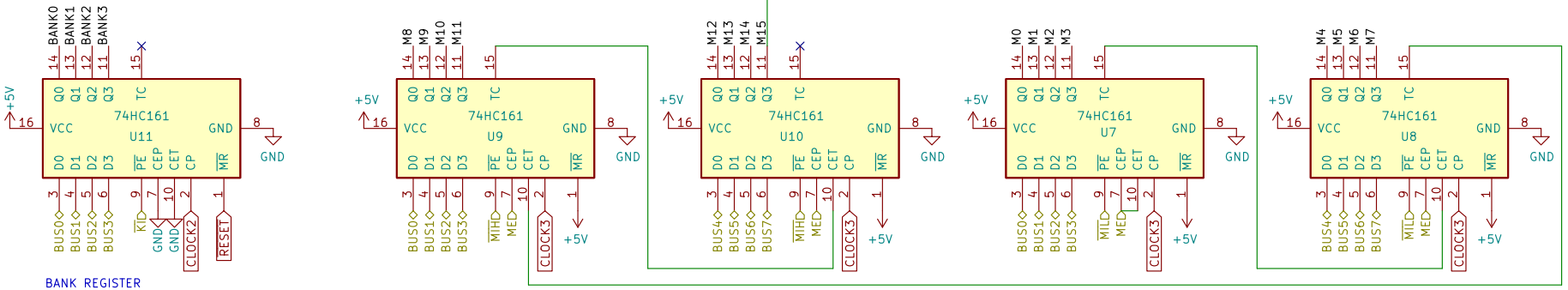
The expansion port pinout is included here just for completeness. It may not be sensible to implement it on breadboards.



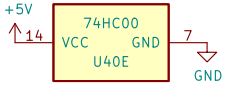

MEMORY ADDRESS REGISTER MSB

MEMORY ADDRESS REGISTER LSB




BANK REGISTER

A MAR reset is not needed: While $\overline{\text{RESET}}$ is pressed, the clock runs with Step=0 and PC=0. This ensures that after COL|MIL and COH|MIH also MAR=0.

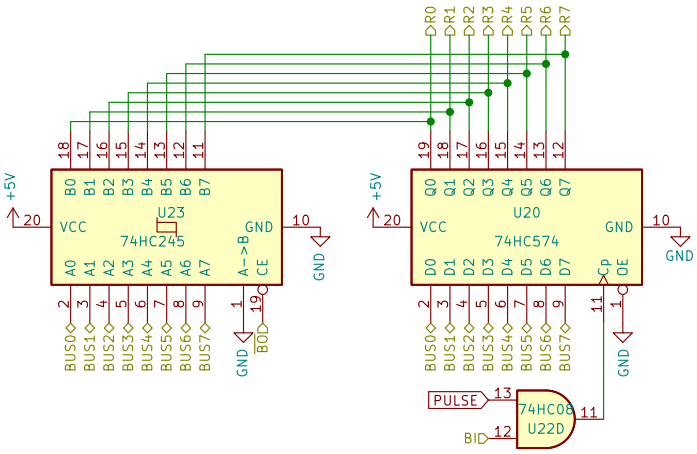





Sheet: /Memory/
File: RAM.kicad_sch

**Title: RAM, ROM and MAR**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 5/9 |

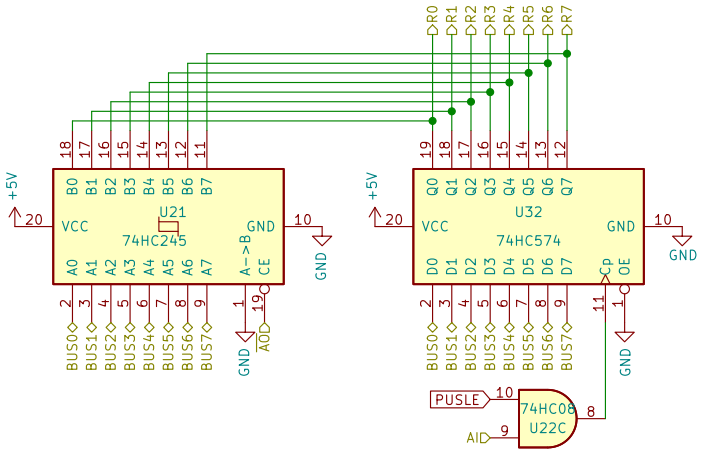


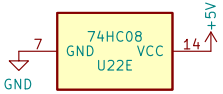



Sheet: /Register B/
File: RegB.kicad_sch

**Title: B Register**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 7/9 |



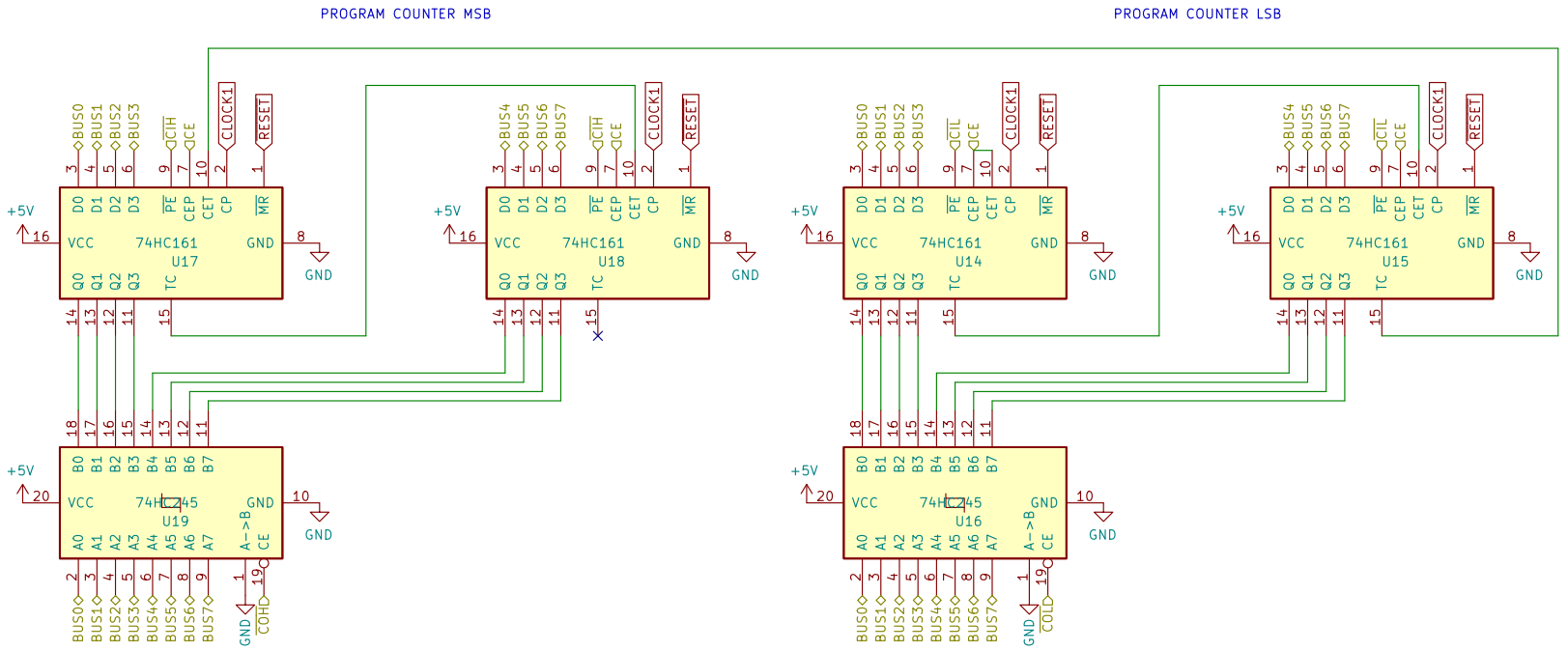






Sheet: /Register A/
File: RegA.kicad_sch

**Title: A Register**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 8/9 |

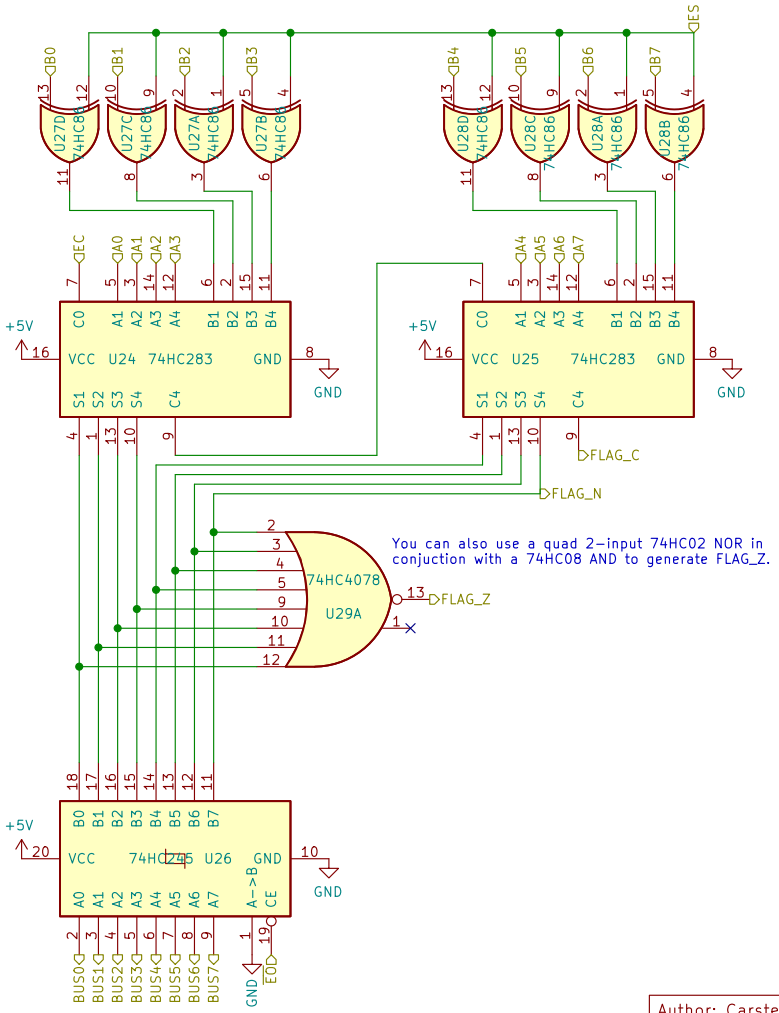





Sheet: /PC/
File: PC.kicad_sch

**Title: Program Counter**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 9/9 |







Sheet: /ALU/
File: ALU.kicad_sch

**Title: Arithmetic and Logic Unit**

| Size: A4 | Date: 2022-07-16 | **Rev: 1.6** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.5) | | Id: 10/9 |