CPU System 1.6 Redux Beast Mode

- Von-Neumann architecture, 8-bit data bus, 16-bit address bus
- 64 instructions including conditional branching, subroutines, stack and word operations
- UART interface for terminal display, keyboard input, data I/O & upload via 'cut & paste'
- 32KB RAM, 512KB FLASH with file system (format, load, save, dir, delete commands)
- Expansion port
- **Maximum clock speed 8.3MHz**

- 2 data registers A and B
- Simple adder
- 3 flags (negative, carry and zero)
- **24** control signals
- **40 TTL chips** (74HCxx logic, 62256 SRAM, 39SF0x0 FLASH)

- Online reference manual
- Games, cross-assembler (Win10 or Python), cycle-exact emulator (Win10)
- **Native tool-chain: Operating system, text editor, assembler, Python-like interpreter**

1.6 Redux

Control Signals
Components
Functional Blocks
Data Lines
Data Bus

TI = UART Transmitter Register In
TO = UART Receiver Register Out
TC = UART Receiver Register Clear
MIL = Memory Address Register In (LSB)
MIH = Memory Address Register In (MSB)
ME = Memory Address Register Increment
KI = Bank Register In
RI = RAM In
RO = RAM Out
CIL = Program Counter In (LSB)
CIH = Program Counter In (MSB)
COL = Program Counter Out (LSB)
COH = Program Counter Out (MSB)
CE = Program Counter Increment
AI = A Register In
AO = A Register Out
BI = B Register In
BO = B Register Out
EO = Adder Sum Out
ES = Adder Invert Operand B
EC = Adder Carry In
FI = Flags Register In
II = Instruction Register In
IC = Step Counter Clear

TI → UART Transmitter

BI → B Register ← BO

TO → UART Receiver
TC →

AI → A Register ← AO

ES → Inverter

MIL → MAR_LSB
ME →
MIH → MAR_MSB

EO → Buffer

Adder & Subtractor — Flags NCZ ← EC

KI → BANK

RI → 512KB FLASH 32KB RAM
RO →
A18-A15 MSB LSB Address

Instruction ← 6
Flags NCZ
Step

II FI IC

COL → Buffer
CIL → PC_LSB
CE →
COH → Buffer
CIH → PC_MSB

Address
Control ROM

CIL CIH COL COH CE TI TO TC FI II IC KI
ES EO EC MIL MIH ME RI RO AI AO BI BO