## CPU System 1.6 Redux Beast Mode

- Von-Neumann architecture, 8-bit data bus, 16-bit address bus
- 64 instructions including conditional branching, subroutines, stack and word operations
- UART interface for terminal display, keyboard input, data I/O & upload via 'cut & paste'
- 32KB RAM, 512KB FLASH with file system (format, load, save, dir, delete commands)
- Expansion port (I/O card, VGA card)
- Maximum clock speed 8.3MHz, 1.01Mips (= 2.3 x



- 2 data registers A and B
- Simple adder
- 3 flags (negative, carry and zero)
- 24 control signals
- 40 TTL chips (74HCxx logic, 62256 SRAM, 39SF0x0 FLASH)
- Online reference manual
- Games like TETRIS, cross-assembler (Win10 or Python), cycle-exact emulator (Win10)
- Native tool-chain: Operating system, text editor, assembler, Python-like interpreter

## lini\mak 1.6 Redux

**Control Signals** Components **Functional Blocks** Data Lines

= UART Transmitter Register In = UART Receiver Register Out = UART Receiver Register Clear MIL = Memory Address Register In (LSB) MIH = Memory Address Register In (MSB) = Memory Address Register Increment = Bank Register In = RAM In = RAM Out CIL = Program Counter In (LSB) CIH = Program Counter In (MSB) COL = Program Counter Out (LSB) COH = Program Counter Out (MSB) = Program Counter Increment = A Register In = A Register Out

= B Register In = B Register Out = Adder Sum Out

= Adder Invert Operand B

= Adder Carry In = Flags Register In = Instruction Register In

= Step Counter Clear

UART 8 8 ransmitter Register - BO **UART Data Bus** 8 8 Receiver Register — AO 8 MIL-Inverter FS MAR<sub>LSB</sub> 8 ME **←**EC MAR<sub>MSB</sub> 8 MIH Buffer 8 Adder & Subtractor KI-BANK Flags NCZ EO  $\infty$  $\infty$ A18-A15 MSB LSB Address W 8 512KB FLASH FI IC 8 RO-32KB RAM Instruction Step Flags COI Buffer 0 ω **CIL**→ **PC**<sub>LSB</sub> CE Address **Control ROM** COH-CIL CIH COL COH CE TI TO TC FI II IC KI 8