Circuits Lab 9

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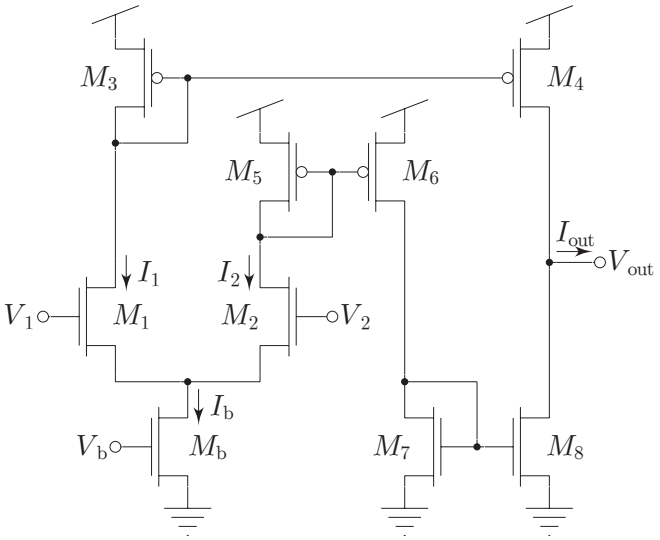

Figure 1:

Experiment 1

The first experiment we conducted involved finding the voltage transfer characteristic of our new and improved differential amplifier. We held the bias voltage a small amount over threshold, and then swept V_1 as we held V_2 constant. The results of our experiment are in figure 2.

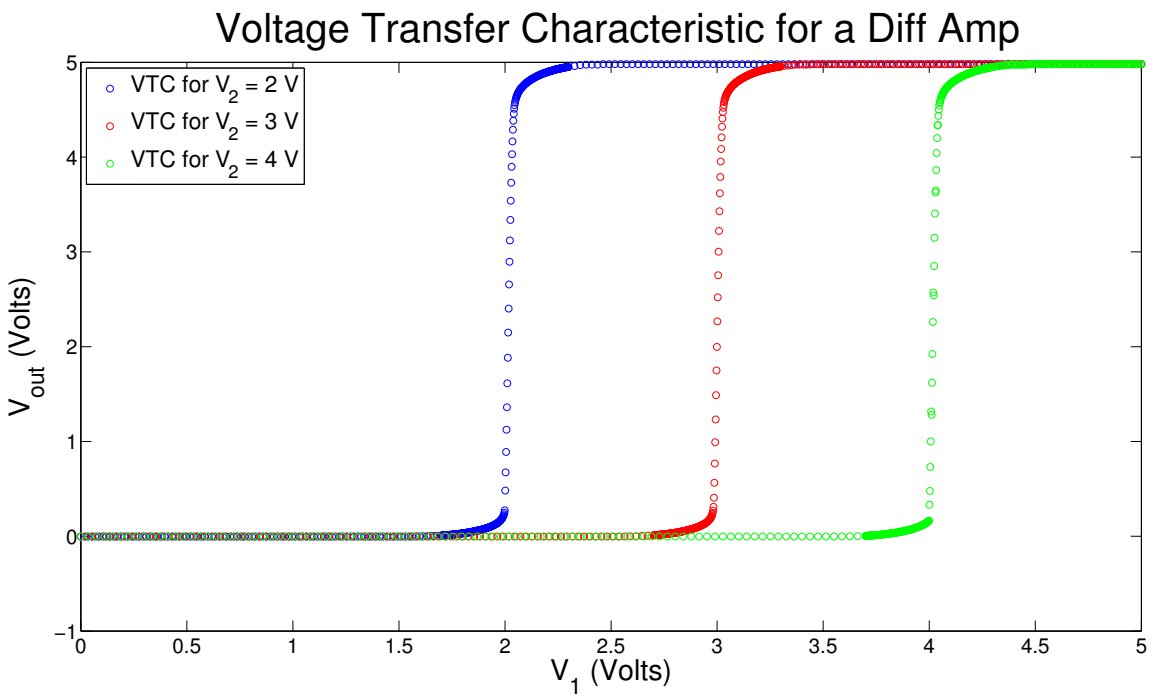

Figure 2: Voltage transfer characteristic of the improved differential amplifier. We can see that this improved differential amplifier displays ideal rail-to-rail output voltage response to both positive and negative values of V_{dm} , as well as a rapid climb from the bottom rail to the top rail with increasing V_{dm} .

The VTC of the improved differential amplifier displays rail-rail operation for all values of V_1 , and a very climb from 0 to V_{dd} once $V_1 > V_2$. The transition region between railing low and railing high is approximately 800 mV wide for all three values of V_2 . We next compared the VTC of the improved differential amp with the VTC of the differential amp we worked with during Lab 8, which is reproduced in figure 3 for convenience.

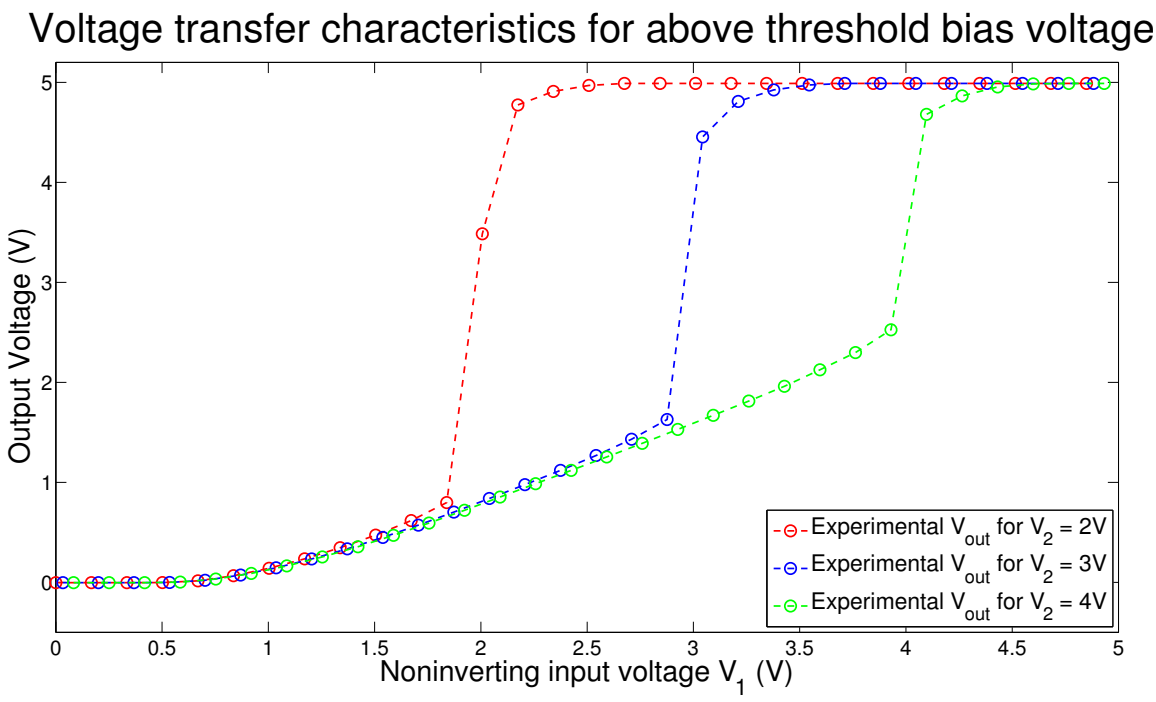

Figure 3: Voltage transfer characteristic of the differential amplifier used in Lab 8. This circuit doesn't display rail-to-rail output voltage response; rather, V_{out} increases linearly with V_{in} for negative values of V_{dm} . In addition, V_{out} doesn't change very rapidly towards the top rail with once $V_{dm} > 0$.

The first obvious different is the poor flooring performance of the old differential amplifier compared to the new one. When $V_1 > V_2$, we expect the output to rail low (as we see in figure 2), but in the old diff amp V_{out} instead followed V_1 linearly, a phenomenon we explained in post-lab 8. The top rail seems to behave the same for both differential amplifiers.

The width of the transition region (from bottom rail to top rail) for the old differential amplifier is far larger, due to the V_{out} following V_1 linearly for some values of V_1 . The slope of transition is also less steep, which indicates that the old diff amp is more likely to be stuck between either rail.

The improved diff amp shows better performance characteristics due to the added current mirrors that more effectively isolate the input and output circuitry. The current mirrors prevent the bias transistors from shutting off when V_{out} is very high or low, which avoids the V_{out} following V_{in} linearly for $V_{dm} < 0$, and overall creates a more ideal differential voltage amplifier.

Experiment 2

For a single value of the inverting input voltage, we then swept the non-inverting input around the inverting one while measuring V_{out} . We then fit a straight line to the steep portion of the curve in order to determine the differential-mode voltage (A_{dm}) gain of the circuit. The experimental results, along with the differential mode gain fit to the curve is shown in Figure 4.

From the experimental data, we found $A_{dm} \approx 110$

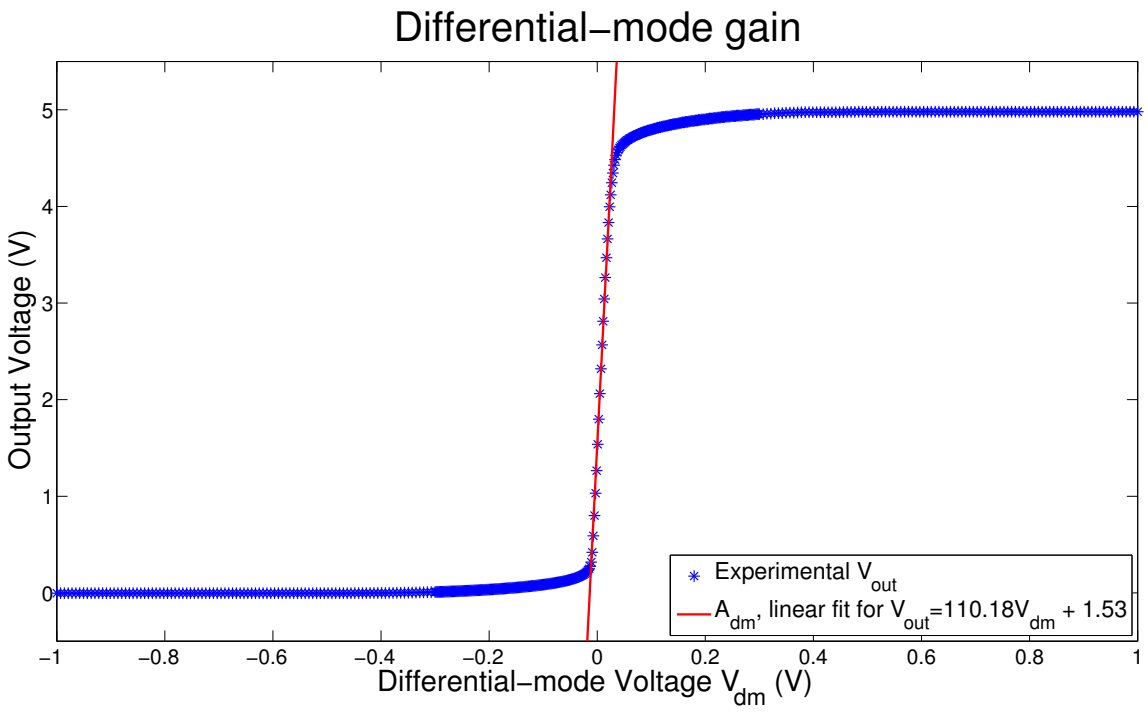

Figure 4:

Next, we set the differential-mode input voltage to zero and measured the current flowing into the output of the amplifier as we swept V_{out} from one rail to the other. We fit a straight line to the shallow part of this output current–voltage characteristic in order to determine the incremental output resistance of the circuit. The voltage transfer characteristic in this region can be seen below in Figure 5. From the linear fit, we extracted an incremental output resistance of $489.6k\Omega$.

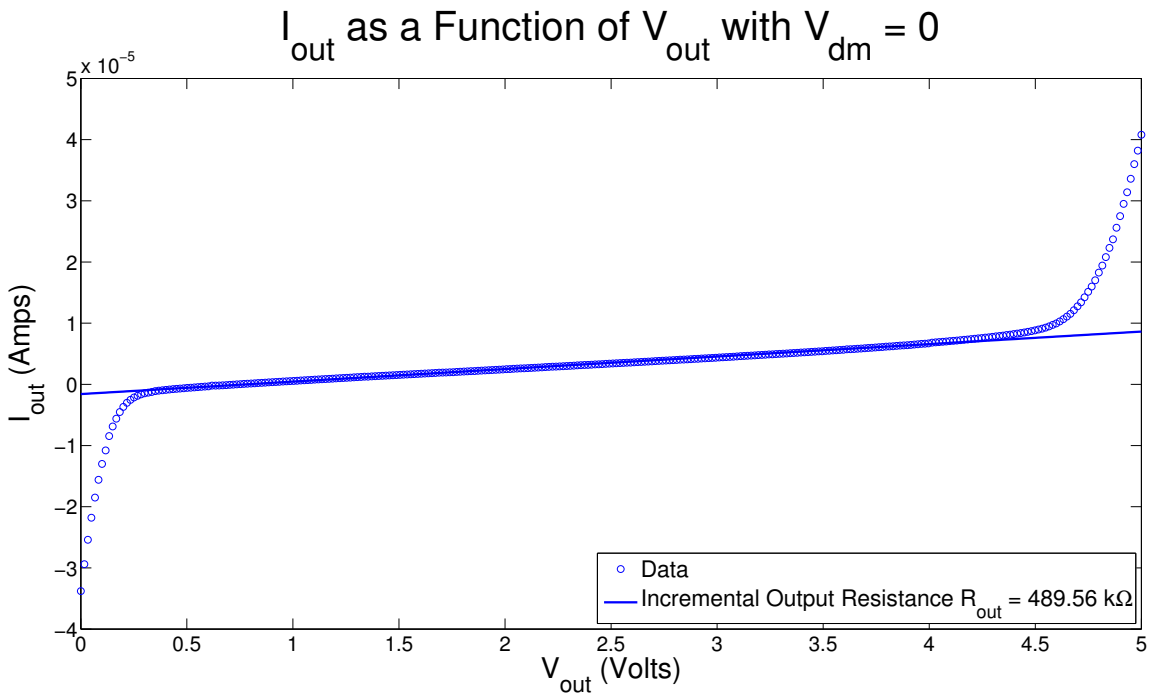

Figure 5:

Next, we fixed the output voltage at $2.5V$ and measured the current flowing out of the amplifier as we swept V_{dm} around zero. We then fit a straight line to the curve around where $V_{dm} = 0$ in order to extract the incremental transconductance gain of the circuit. This voltage transfer characteristic can be seen in Figure 6. From the linear fit, we extracted an incremental transconductance gain of $2.3687 \times 10^{-4}\Omega^{-1}$

In this experiment, we found the limiting values of I_{out} to be $+66.69\mu A$, and $-70.01\mu A$, fairly symmetric on both rails.

We then calculated the differential-mode gain of the circuit by computing the product of G_m and R_o .

$$A_{dm} = 2.3687 \times 10^{-4}\Omega^{-1} \cdot 489.6k\Omega = 115.477$$

This theoretical differential-mode gain is slightly higher than our extracted value, of 110. This represents a relative percent error of roughly 4.9%.

In comparison to our previous lab's VTC and A_{dm} value, this circuit is a much better amplifier. It not only can achieve a larger range of output voltages, with a rail-to-rail swing, but the differential-mode-gain is almost twice that of Lab 8's amplifier. In Lab 8, we found $A_{dm} = 62.4146$. Thus this amplifier is far more reactive to small changes in voltage and would be more useful in the real world!

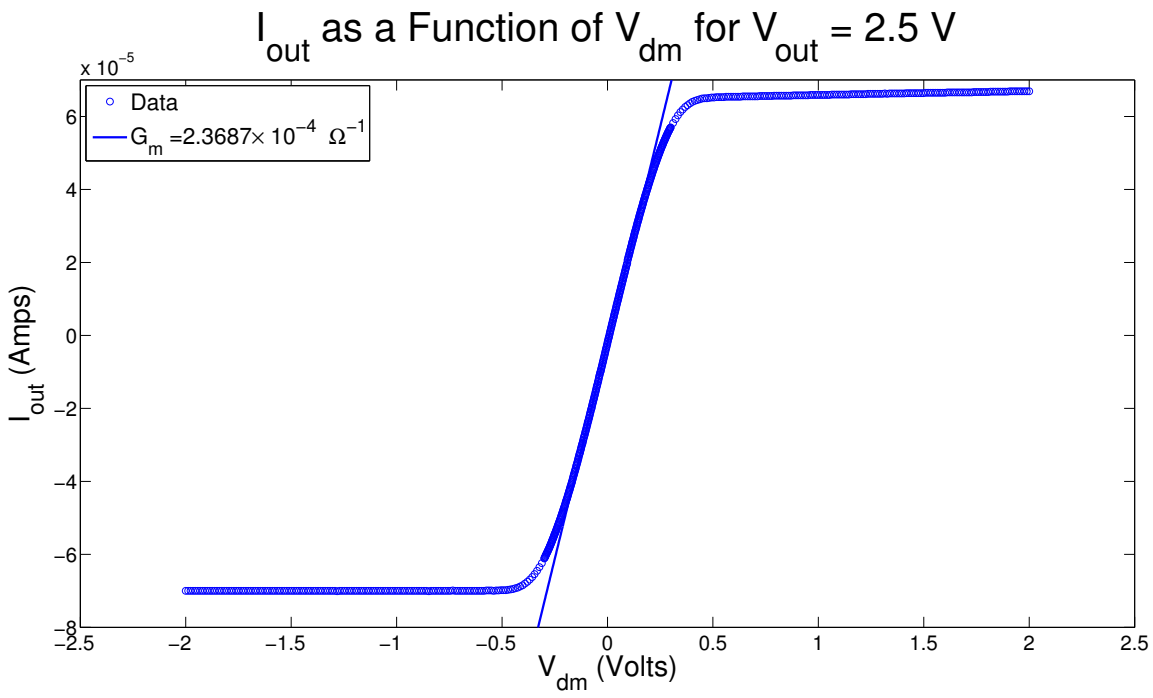

Figure 6:

Experiment 3

Differential amplifiers are often used in AC contexts, where the output voltage often has to change rapidly depending on the inputs. One case is when a unity-gain amplifier must pass a square wave. We saw in pre-lab 9 that an improved diff amp with a small capacitive load can only change V_{out} so quickly, and in this experiment we tested the step response of the diff amp to both large and small steps, with a $1nF$ capacitor parallel to the feedback loop. We saw that given a small step, V_{out} takes a first-order approach to V_{in} , and extracted time constants for both the up- and down-swings. We also saw that given a large step, V_{out} approaches V_{in} linearly, and we extracted values for the slew rate for both the up- and down-swings.

Small Signal Analysis

We first started by sending a $3.2kHz$ square wave into the unity-gain follower, with a peak to peak voltage of 30 mV. This low amplitude ensured that we would see that small signal response of the unity-gain buffer. We used the oscilloscope to take data for V_{in} and V_{out} , and then extracted experimental values for time constants. We also used the value of G_m we extracted in experiment 2, along with the known value of the capacitor, to derive a theoretical value for the time constant τ.

Recalling pre-lab 9, we know that V_{out} follows V_{in} according to the following equation:

$$V_{out} = V_{in} - V_{out}(0)e^{-\frac{G_m}{C}t} \tag{1}$$

Where G_m is the incremental transconductance gain of the circuit and C is the capacitance of the capacitive load to the circuit. We define our time constant τ as:

$$\tau = \frac{C}{G_m} \tag{2}$$

Given our extracted value for G_m from experiment 2 and the $1nF$ capacitor, we expect our theoretical time constant to have a value of 4.22×10^{-6} seconds. In figure 7, we plotted the experimental results from our small-signal experiment along with theoretical fits using our theoretical time constant. We also extracted time constants for the up- and down-swing using the 63% trick, and plotted curves for using those values of τ as well.

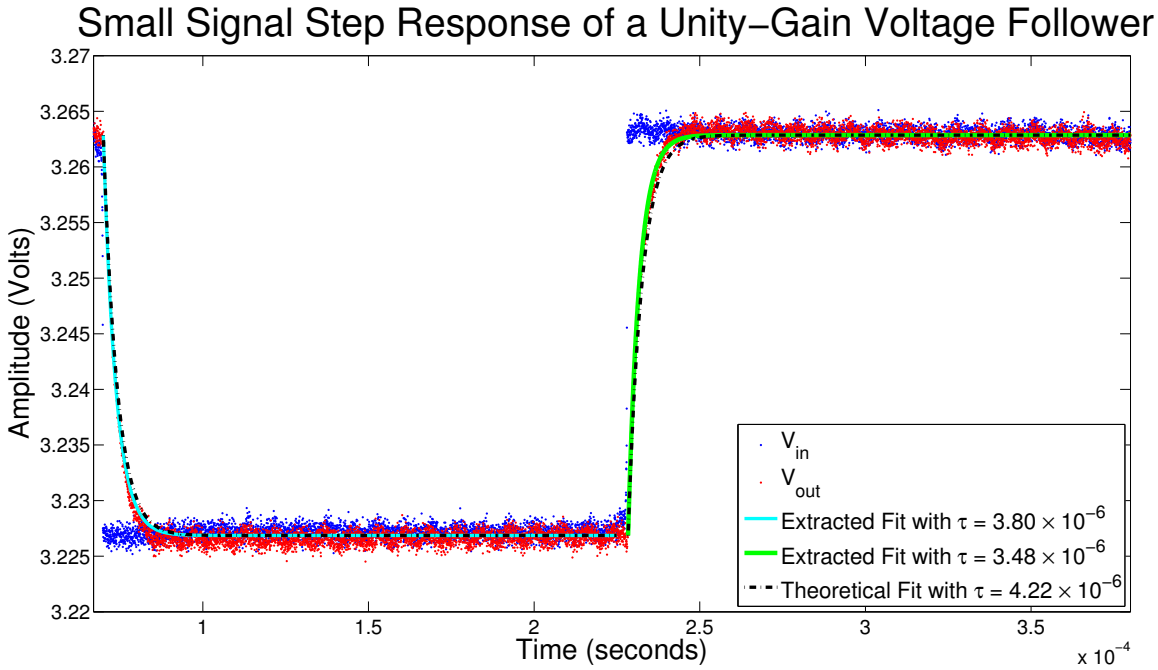

Figure 7: Small-signal step response of a unity-gain voltage follower. We can see that V_{out} follows a first-order approach to V_{in} . The following is slightly asymmetrical, with extracted time constants that are about 10% apart.

We first saw that the down- and up-swing of V_{out} following a first-order approach to V_{in} , which is the kind of approach we expect for small steps. For the down-swinging change in V_{out} , we found that $\tau = 3.8 \times 10^{-6}$, and for the up-swing change in V_{out} we found that $\tau = 3.48 \times 10^{-6}$. The experimentally-derived values for τ deviate from our theoretical value by an average of 15%, which is pretty close considering the magnitude of the time constant. We expect that the slight difference (about 10%) between the down-swing and up-swing time constants could be due to the different inherent properties of the pMOS and nMOS transistors used in the current mirrors that generate V_{out} . Small differences in these transistors could cause V_{out} to deviate slightly when $V_{dm} = 0$, which would in turn change how V_{out} approaches V_{in} when increasing or decreasing.

Large Signal Analysis

We then sent the same square wave through the unity-gain follower, but increased the amplitude to about 2 volts. We know from the pre-lab that differential amplifiers can only increase the output voltage so quickly. Specifically, given a large step change, the unity-gain buffer will follow a linear equation:

$$V_{out} = \frac{I_b}{C} t + V_{out}(0) \tag{3}$$

We therefore expect V_{out} to follow V_{in} linearly for a large step change. Figure 8 confirms this assumption, as we see that V_{out} has very linear regions.

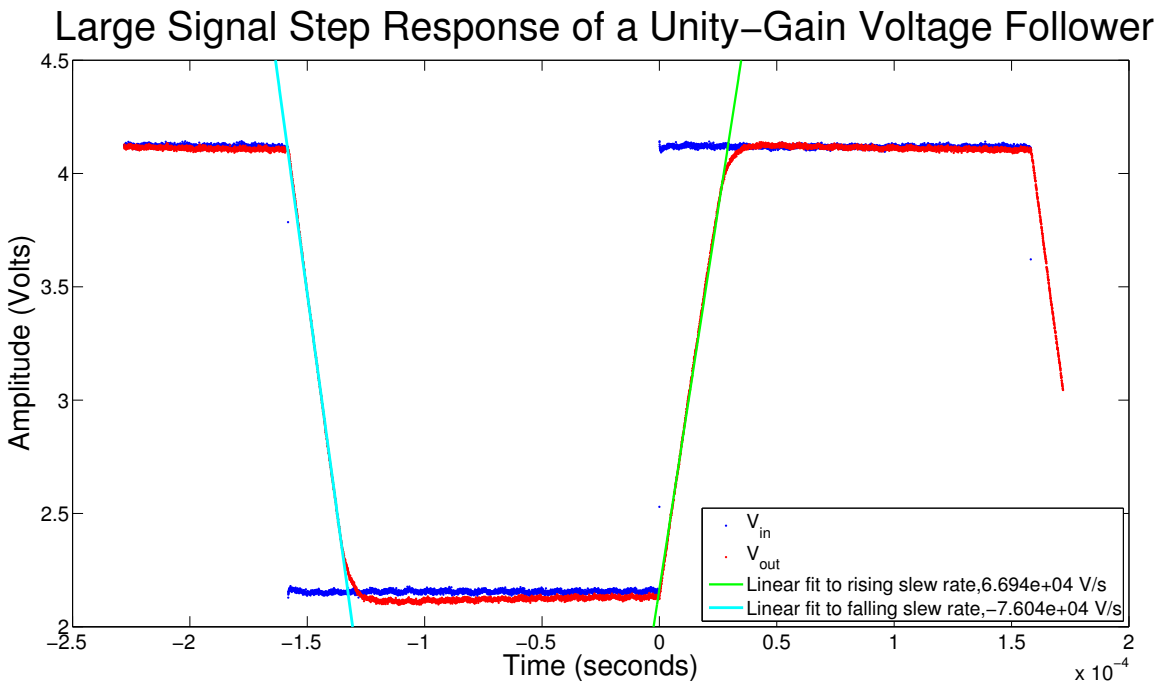

Figure 8: Large-signal step response of a unity-gain voltage follower. The up- and down-swing slew rates are about 13% off in magnitude, a deviation that is likely caused by the pMOS and nMOS transistors not being exactly matched. The extracted slew rate values match our theoretical values very closely.

We then extracted values for the down- and up-swing slew rates. We found that the extracted down-swing slew rate had value of $6.69 \times 10^4 \frac{Volts}{s}$, and the up-swing slew rate had a value of $-7.6 \times 10^4 \frac{Volts}{s}$. We then used the maximum and minimum current values we found in experiment two, and the value of the load capacitor, to find theoretical values for these slopes. For the down-swing voltage, when the current output is railing low, we found the theoretical slope to be $-7.071 \times 10^4 \frac{Volts}{s}$, and for the up-swing, we found the theoretical slope to be $6.69 \times 10^4 \frac{Volts}{s}$. The values we found for the up-swing are almost the same, but the values for the down-swing are off by about 7%. Largely, however, our theoretical values match our extracted values very closely, indicated how effective the linear estimation is at predicted the unity-gain follower's behavior given large voltage steps.