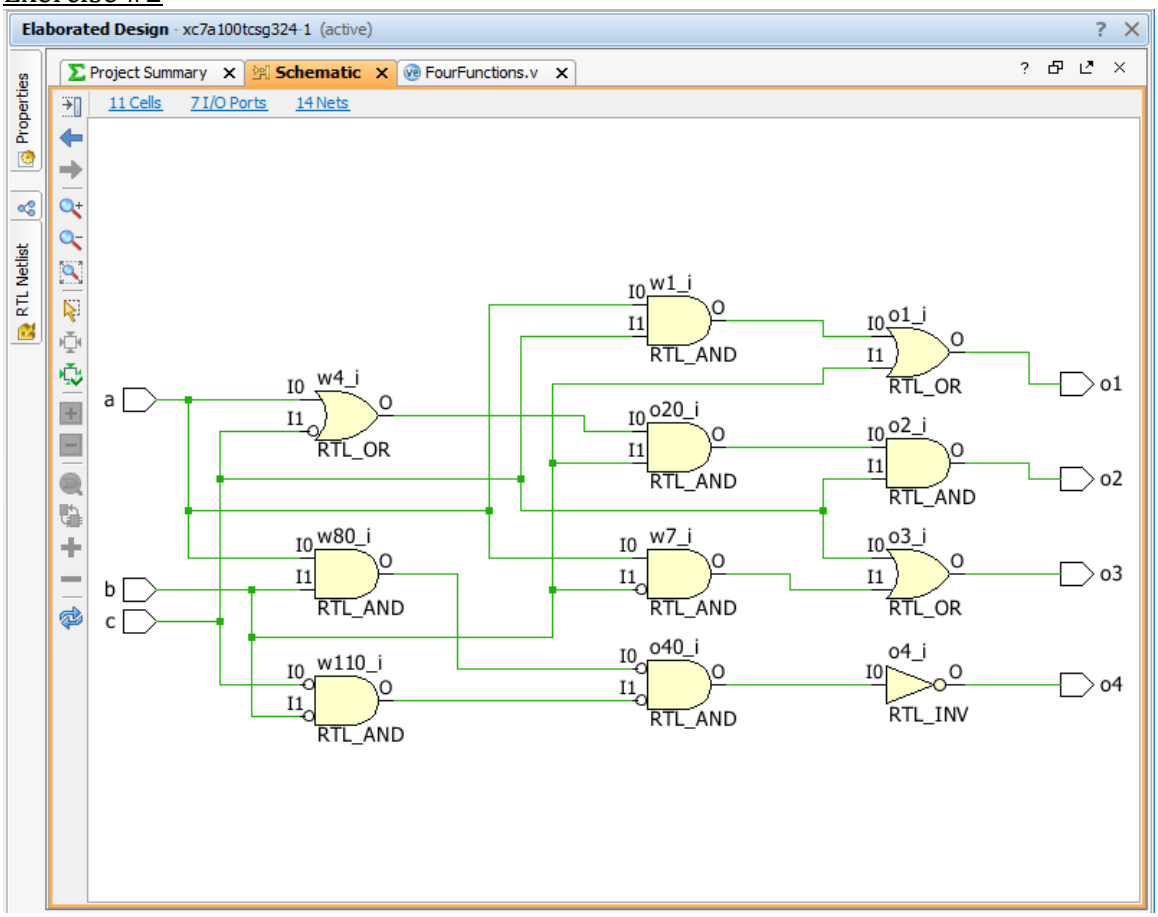
ECEN 220 – Fall 2017
<Lab 3: Structural Verilog>
<Coryell>, <Jack>
<Section 002>

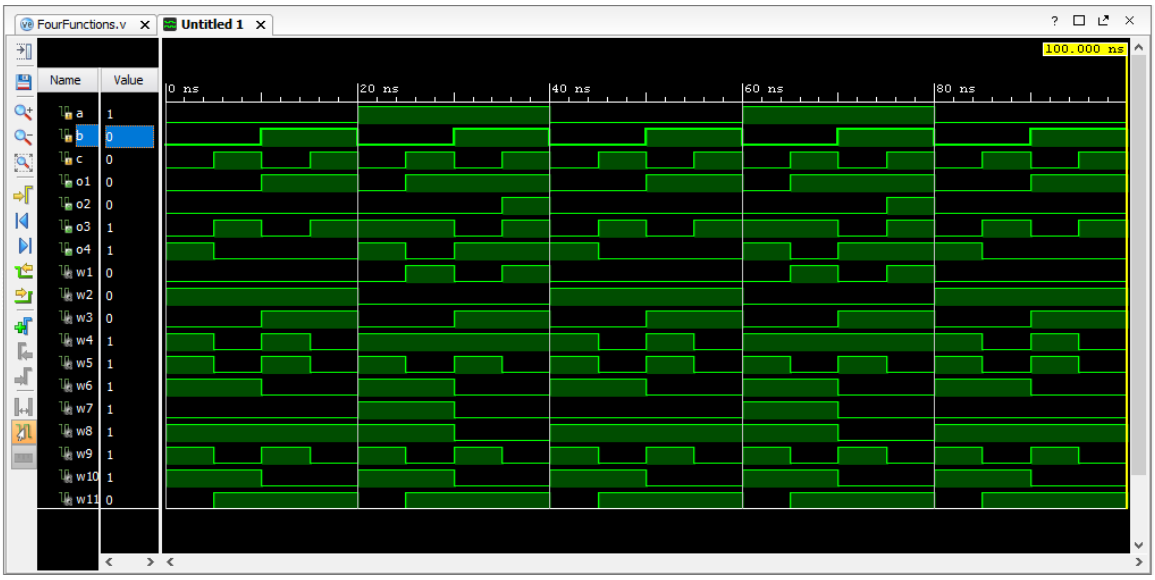
Preliminary
N/A

Exercise #1
N/A

Exercise #2



Exercise #3
add_force a {0 0} {1 20} -repeat_every 40
add_force b {0 0} {1 10} -repeat_every 20
add_force c {0 0} {1 5} -repeat_every 10

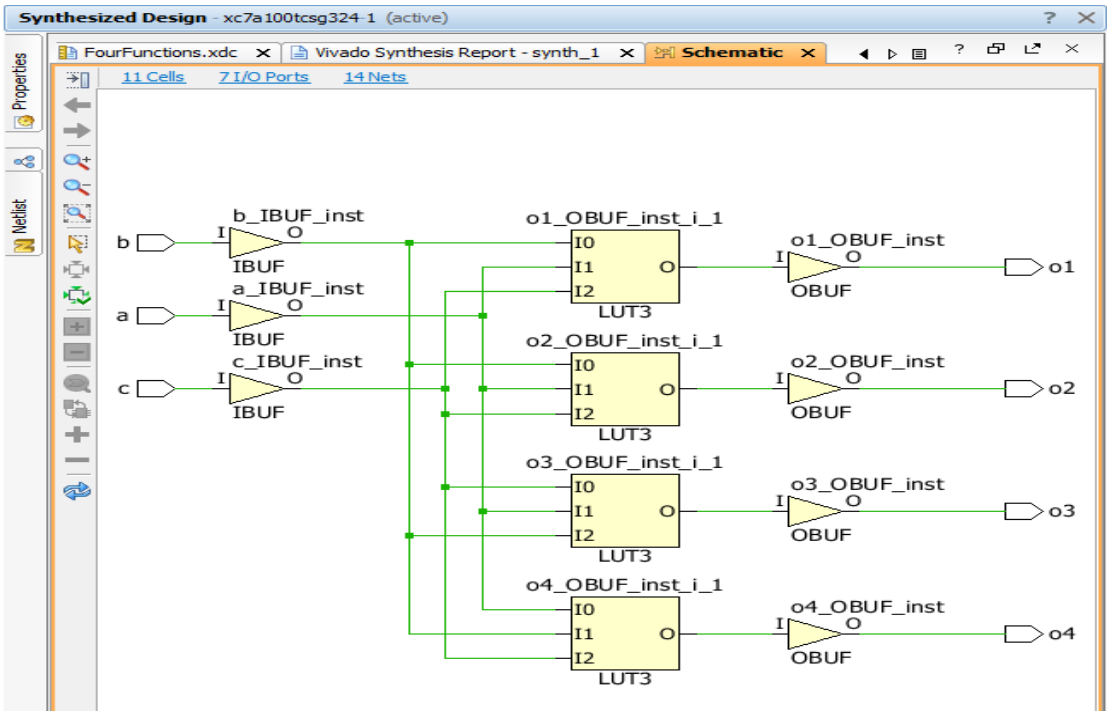


Exercise #4

```
set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { a }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { b }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { c }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { o4 }]; #IO_L18P_T2_A24_15 Sch=led[0]
set_property -dict { PACKAGE_PIN K15   IOSTANDARD LVCMOS33 } [get_ports { o3 }]; #IO_L24P_T3_RS1_15 Sch=led[1]
set_property -dict { PACKAGE_PIN J13   IOSTANDARD LVCMOS33 } [get_ports { o2 }]; #IO_L17N_T2_A25_15 Sch=led[2]
set_property -dict { PACKAGE_PIN N14   IOSTANDARD LVCMOS33 } [get_ports { o1 }]; #IO_L8P_T1_D11_14 Sch=led[3]
```

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Some of the differences between my original schematic and the synthesis schematic include NOT gates immediately following the inputs, a centralized set of gates with 3 inputs each and one output each that directly leads into another NOT gate and then the respective outputs (screenshot included).



There are 2 Look-up tables and 7 Input / Output pins.

Exercise #5

FINAL VERILOG CODE:

```
/**********************************************************************
*
* Module: <FourFunctions>
*
* Author: <John Coryell>
* Class: <ECEN 220, Section 2, Fall 2017>
* Date: <09/21/2017>
*
* Description: <FourFunctions verilog assignment for Lab #3>
*
*
**********************************************************************/
module fourfunctions (a, b, c, o1, o2, o3, o4);
        input a, b, c;
        output o1, o2, o3, o4;
        wire w1, w2, w3, w4, w5, w6, w7, w8, w9, w10, w11;

        and (w1, a, c);
        not (w2, a);
        and (w3, b);
        or (o1, w1, w3);
```

```
    or (w4, a, w5);
    not (w5, c);
    and (o2, w4, b, c);

    not (w6, b);
    and (w7, a, w6);
    or (o3, c, w7);

    nand (w8, a, b);
    not (w9, c);
    not (w10, b);
    nand (w11, w9, w10);
    nand (o4, w8, w11);

endmodule
```

Personal Exploration

As part of my personal exploration, I created a truth table based on every possible outcome of switch combinations and LEDs.

A	B	C	LED0	LED1	LED2	LED3
0	0	0	1	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	1	0	1	0	1
1	1	0	1	0	1	0
1	1	1	1	1	1	1

How many hours did you work on the lab?

About 4 and a half.

Please provide any suggestions for improving this lab in the future:

N/A.