Project of the Digital Part

Due: December 28, 2019

Phase1: Multisim Simulation

In this phase, you will implement a counter in Multisim. The input is a square wave only. The output is two seven-segment displays and two LEDs. The total cycles to be counted T is the addition of each bit of your ShanghaiTech student ID. Two seven-segment displays show the counting result in decimal. In the intermediate state, the red LDE is lighted 3 cycles, and the yellow LED is lighted 5 cycles immediately. The intermediate state occurs at T/2 cycles approximately. Especially, your counter can be reset after T square waves and count again.

Phase2: VHDL Programming

In this phase, you will implement a counter in VHDL, and synthesize in vivado. The input signal are clock(CLK), reset(RST), and count enable(CE). The output signal are counting result(multi-bit vector), and finish counting flag(F). The total cycles to be counted T is the addition of each bit of your ShanghaiTech student ID. When CE is high, counter works. After T clock cycles, the count is complete and F become high.You should complete the VHDL code and the pre-simulation in vivado. Then synthesize and get your circuit diagram in the gate level.

Phase3: Project Report

In this phase, firstly, you will report the design ideas completely with necessary screen-shots, and secondly, you will report the results of the comparison and your gains.