US Micro Products
ENGINEERED DISPLAY SOLUTIONS

PMOLED APPLICATION NOTES

Upgrade your product with the bright and beautiful colors of a PMOLED

Part Number	USMP-P27201
Size	1.3"
Panel Size	128 x 96
Color	white
IC	SSD1327

OLED Benefits:

- **Great outdoor readability**
- **Affordable**
- **Low profile** (very thin)
- **Flexible**
  (bendable to a certain degree)
- **Low power consumption**
- **Bright and vivid colors**
- **Deeper blacks**

FOR ADDITIONAL INFORMATION PLEASE CONTACT:
engineering@usmicroproducts.com

Manufactured for US Micro Products by Rit Display Corporation

Issue Date	Approved by (customer use)	Checked by	Prepared by

(800) 741-7755
www.usmicroproducts.com

Revision History

Version	Content
X01	First release

DESCRIPTION

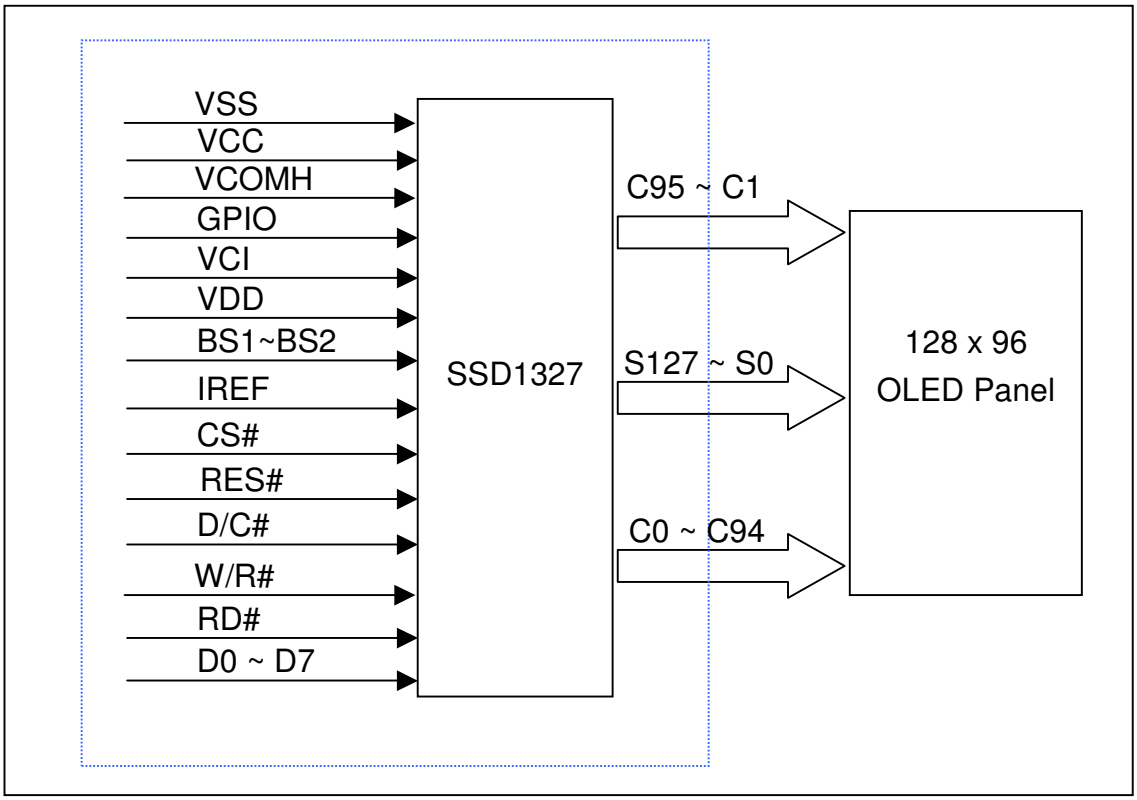
P27201 is a 128X96 dot matrix white passive OLED module with controller for many compact portable applications.

FEATURE

- Panel matrix: 128x96.
- Driver IC: SSD1327.
- 16 gray scale
- V_{CC} =15V
  Internal VDD: VCI =2.6V~3.5V
  (Must use relative the circuit and the initial code.)
  External VDD: VCI =1.65V~2.6V
  (Must use relative the circuit and the initial code.)

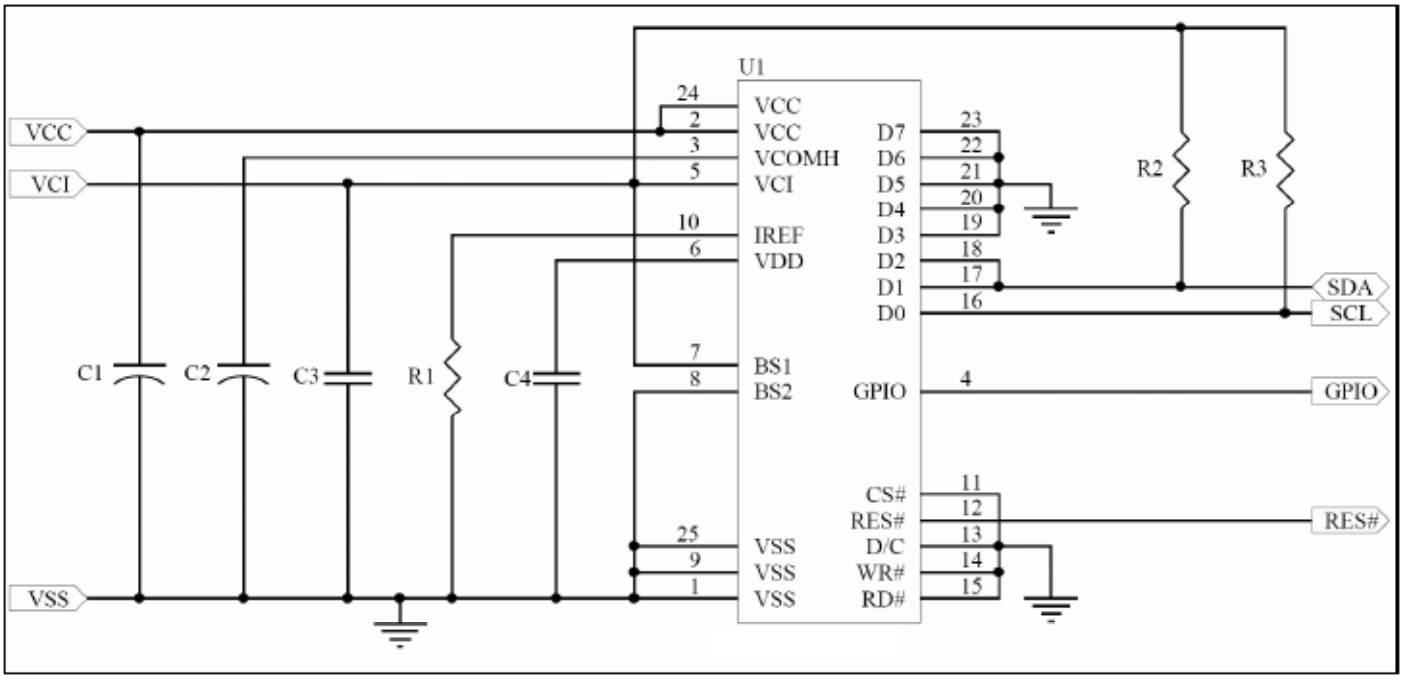
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, IIC Interface.

FUNCTION BLOCK DIAGRAM



RiTdisplay 128x96 OLED Module

Application circuit (*Internal VDD*: VCI =2.6V~3.5V)



Component:

C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

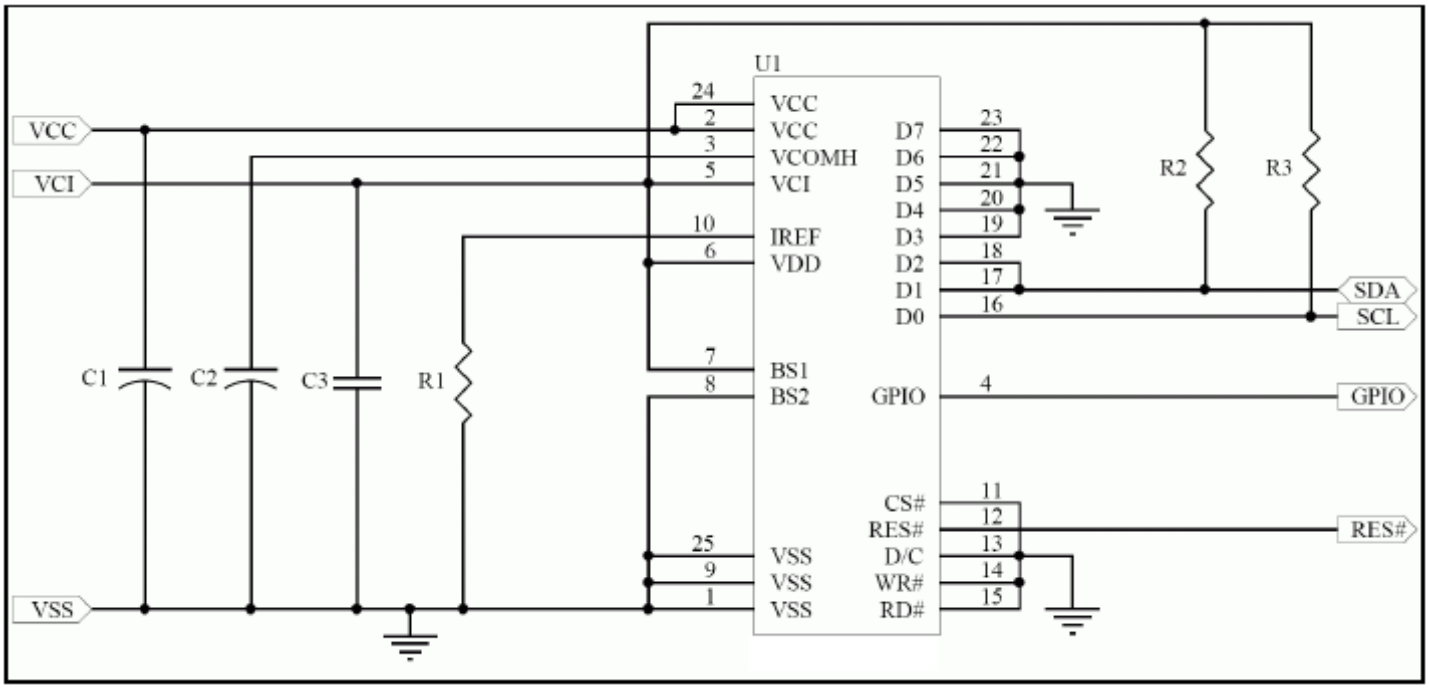
C3, C4: 1uF/16V(0603)

R1: 1M ohm (0603) 1%

R2, R3: 10K ohm (0603)

This circuit is for IIC interface.

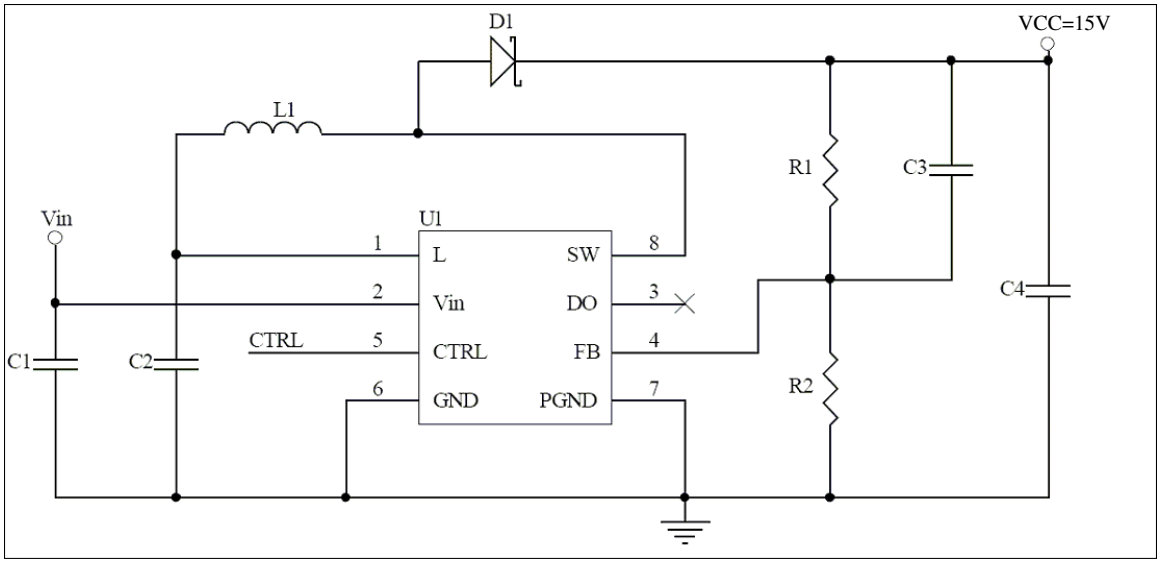
Application circuit (*External VDD*: VCI =1.65V~2.6V)



Component:
C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)
C3: 1uF/16V(0603)
R1: 1M ohm (0603) 1%
R2, R3: 10K ohm (0603)

This circuit is for IIC interface.

DC-DC application circuit for OLED module



Recommend components:

The C1: 0.1uF/6.3V.

The C2: 4.7 uF/6.3V.

The C3: 22pF/16V.

The C4: 4.7uF/35V Tantalum type capacitor.

The R1: 1.27M ohm 1%.

The R2: 113K ohm 1%.

The D1: SCHOTTY DIODE.

The L1: 10uH.

The U1: HPA00483DRBR

The R1, R2 and C3 value should be fine tune by customer.

NOTE a. The HPA00483DRBR is low cost DC/DC for TI.

b. The HPA00483DRBR spec. is same as TPS61045.

Pin Assignments

PIN NAME	PIN NO	DESCRIPTION
VSS	1	Ground.
VCC	2	Power supply for analog circuit.
VCOMH	3	Com Voltage Output. A capacitor should be connected between this pin and V_{SS}.
GPIO	4	General I/O port.
VCI	5	Power supply for logic circuit.
VDD	6	A capacitor should be connected between this pin and V_{SS}.
BS1	7	Interface selection input. In Serial interface.
BS2	8	
VSS	9	Ground.
IREF	10	Reference current input pin. A resistor should be connected between this pin and V_{SS}.
CS#	11	Chip select input.
RES#	12	Reset signal input. When it's low, initialization of SSD1327 is executed.
D/C	13	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
WR#	14	This pin is used to receive the write data signal.
RD#	15	This pin is used to receive the read data signal.
D0	16	Data bus (for parallel interface) When IIC mode is selected, D2, D1 should be tied together and serve as SDAout, SDA in application and D0 is the serial clock input, SCL.
D1	17	
D2	18	
D3	19	
D4	20	
D5	21	
D6	22	
D7	23	
VCC	24	Power supply for analog circuit.
VSS	25	Ground.

Application Initial Setting (*Internal VDD*: VCI =2.6V~3.5V)

```
/*128x96 OLED driver program */
void initial(void)
{
start(); //IIC Start
comm_out(0x78);//Mast code
comm_out(0x00);//Control byte
comm_out(0xae);//Set display off
comm_out(0xa0);//Set re-map
comm_out(0x52);
comm_out(0xa1);//Set display start line
comm_out(0x00);
comm_out(0xa2);//Set display offset
comm_out(0x20);
comm_out(0xa4);//Normal Display
comm_out(0xa8);//Set multiplex ratio
comm_out(0x5f);//96 MUX
comm_out(0xab);//Function Selection A
comm_out(0x01);//Enable internal VDD regulator
comm_out(0x81);//Set contrast
comm_out(0x5F);//normal mode (type brightness)
comm_out(0xb9);//Linear Gray
comm_out(0xb1);//Set Phase Length
comm_out(0x31);
comm_out(0xb3);//Set Front Clock Divider /Oscillator Frequency
comm_out(0x41);//105Hz
comm_out(0xb4); //For brightness enhancement
comm_out(0xb5);
comm_out(0xb6);//Set Second pre-charge Period
comm_out(0x04);
comm_out(0xbc);//Set Pre-charge voltage
comm_out(0x05);
comm_out(0xbe);//Set VCOMH
comm_out(0x07);
comm_out(0xd5);//Function Selection B
comm_out(0x02);//Enable second pre-charge
stop(); //IIC Stop
cleanDDR ();//Clear the whole DDRAM
```

```
start(); //IIC Start
comm_out(0x78);//Mast code
comm_out(0x00);//Control byte
comm_out(0xaf);//Display on
stop(); //IIC Stop
}

void cleanDDR(void)
{
   int i,j;
   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x00);//Control byte
   comm_out(0x15);//Set column address
   comm_out(0x00);//Column Start Address
   comm_out(0x3f);//Column End Address
   comm_out(0x75);//Set row address
   comm_out(0x00);//Row Start Address
   comm_out(0x7f);//Row End Address
   stop(); //IIC Stop

   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x40);//Control byte
   for(i=0;i<128;i++)
   {
      for(j=0;j<64;j++)
      {
        data_out(0x00);
      }
   }
   stop(); //IIC Stop
}
```

After initial the driver IC, user can display all pixels on.

```
void show_data(void)
{
   int i,j;
   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x00);//Control byte
   comm_out(0x15);//Set column address
   comm_out(0x00);//Column Start Address
   comm_out(0x3f);//Column End Address
   comm_out(0x75);//Set row address
   comm_out(0x00);//Row Start Address
   comm_out(0x5f);//Row End Address
   stop(); //IIC Stop

   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x40);//Control byte
   for(i=0;i<96;i++)
   {
      for(j=0;j<64;j++)
      {
        data_out(0xff);
      }
   }
   stop(); //IIC Stop
}
```

Application Initial Setting (*External VDD*: VCI =1.65V~2.6V)

```
/*128x96 OLED driver program */
void initial(void)
{
start(); //IIC Start
comm_out(0x78);//Mast code
comm_out(0x00);//Control byte
comm_out(0xae);//Set display off
comm_out(0xa0);//Set re-map
comm_out(0x52);
comm_out(0xa1);//Set display start line
comm_out(0x00);
comm_out(0xa2);//Set display offset
comm_out(0x20);
comm_out(0xa4);//Normal Display
comm_out(0xa8);//Set multiplex ratio
comm_out(0x5f);//96 MUX
comm_out(0xab);//Function Selection A
comm_out(0x00);//Enable internal VDD regulator
comm_out(0x81);//Set contrast
comm_out(0x5F);//normal mode (type brightness)
comm_out(0xb9);//Linear Gray
comm_out(0xb1);//Set Phase Length
comm_out(0x31);
comm_out(0xb3);//Set Front Clock Divider /Oscillator Frequency
comm_out(0x41);//105Hz
comm_out(0xb4); //For brightness enhancement
comm_out(0xb5);
comm_out(0xb6);//Set Second pre-charge Period
comm_out(0x04);
comm_out(0xbc);//Set Pre-charge voltage
comm_out(0x05);
comm_out(0xbe);//Set VCOMH
comm_out(0x07);
comm_out(0xd5);//Function Selection B
comm_out(0x02);//Enable second pre-charge
stop(); //IIC Stop
cleanDDR ();//Clear the whole DDRAM
```

```
start(); //IIC Start
comm_out(0x78);//Mast code
comm_out(0x00);//Control byte
comm_out(0xaf);//Display on
stop(); //IIC Stop
}

void cleanDDR(void)
{
   int i,j;
   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x00);//Control byte
   comm_out(0x15);//Set column address
   comm_out(0x00);//Column Start Address
   comm_out(0x3f);//Column End Address
   comm_out(0x75);//Set row address
   comm_out(0x00);//Row Start Address
   comm_out(0x7f);//Row End Address
   stop(); //IIC Stop

   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x40);//Control byte
   for(i=0;i<128;i++)
   {
      for(j=0;j<64;j++)
      {
        data_out(0x00);
      }
   }
   stop(); //IIC Stop
}
```

After initial the driver IC, user can display all pixels on.

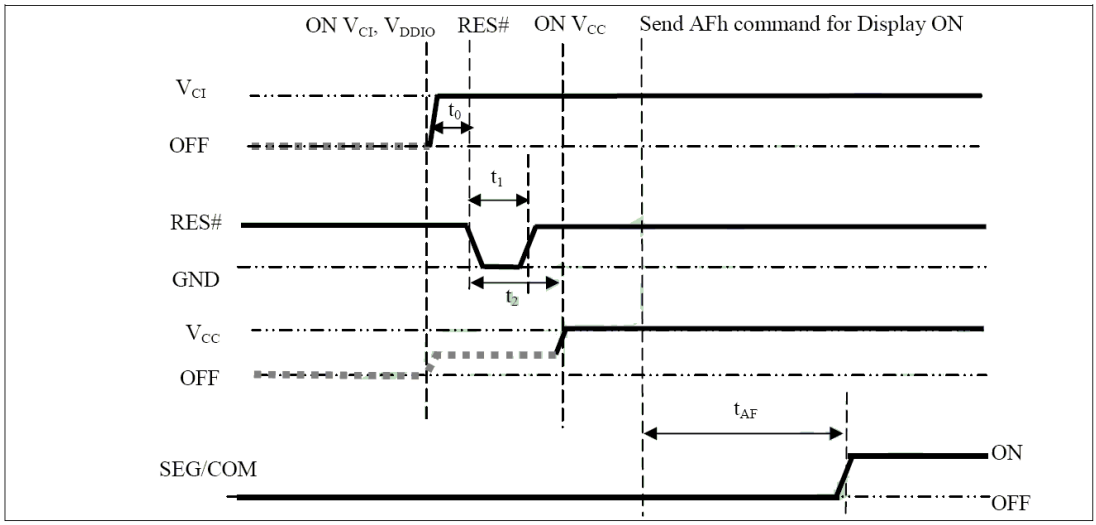
```
void show_data(void)
{
   int i,j;
   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x00);//Control byte
   comm_out(0x15);//Set column address
   comm_out(0x00);//Column Start Address
   comm_out(0x3f);//Column End Address
   comm_out(0x75);//Set row address
   comm_out(0x00);//Row Start Address
   comm_out(0x5f);//Row End Address
   stop(); //IIC Stop

   start(); //IIC Start
   comm_out(0x78);//Mast code
   comm_out(0x40);//Control byte
   for(i=0;i<96;i++)
   {
      for(j=0;j<64;j++)
      {
        data_out(0xff);
      }
   }
   stop(); //IIC Stop
}
```

Power ON / OFF Sequence

Power ON sequence:

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

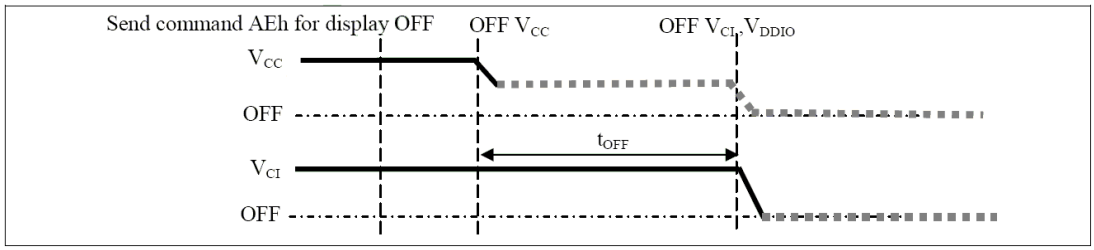
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2), (3)
3. Wait for t_{OFF}. Power OFF V_{CI}.(where Minimum t_{OFF}=80ms (5), Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
(2) V_{CC} should be kept disable when it is OFF.
(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.
(4) The register values are reset after t_1.
(5) V_{CI} should not be Power OFF before V_{CC} Power OFF

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 1

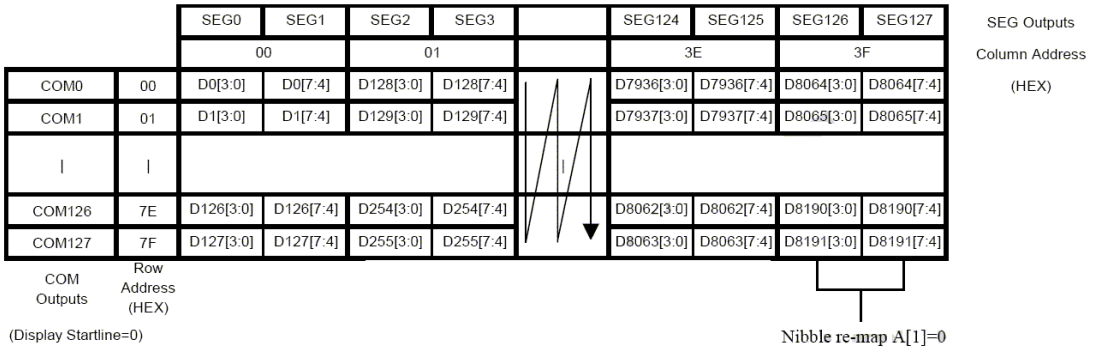
		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	
COM Outputs	Row Address (HEX)										

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

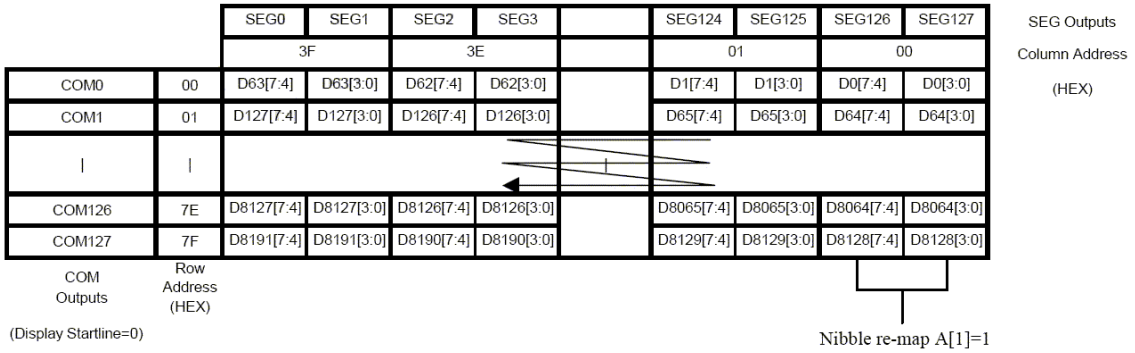
GDDRAM address map 2



The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Enable Column Address Re-map (A[0]=1)
  - Enable Nibble Re-map (A[1]=1)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 3



The example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs (Display Startline=78H)

Row Address (HEX)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

GDDRAM address map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs Column Address (HEX)

COM Outputs (Display Startline=0)

Row Address (HEX)

Nibble re-map A[1]=0