Application 1
Non-linear RC circuits

1.1 Introduction

The main activity for this laboratory is represented by the measurement of the output signal amplitude, delay of low-pass and high-pass *RC* circuits, given an square wave input signal. Several measurements will be performed, with different parameters, such as the value of the resistor *R* , capacitance *C*, as well as the frequency of the input square wave signal.

Working time

2 laboratories - 4 hours

Requirements

- Read the necessary lab documentation.
- Generate the appropriate square wave signals using the signal generator.
- Implement on the breadboard the RC circuits using the appropriate resistors and capacitors
- Scope the output signals of the RC delay.
- Measure using the oscilloscop the amplitude and delays of the output signals
- Draw the waveforms as they appear on the oscilloscope on paper of the output signals.

  Photos of the oscilloscope display are not considered.

Table 1.1 Required Equipment

Equipment	Qty
Signal generator	1
Oscilloscope	1
Scope probe	2
Breadboard	1
Resistors - 300 Ω and 1 $k\Omega$	1 each
Capacitors - 470 pF and 3.3 nF	1 each

1.2 Theoretical background

1.2.1 Square wave signal

The square wave signal represents the most used type of signal in digital circuits. It is a periodic signal, who's waveform is depicted in Fig 1.1. The main characteristics of the square wave signals are:

- Amplitude U difference between the two voltage levels $U1$ and $U2$;
- Frequency F and the corresponding period $T = \frac{1}{F}$;
- Duty factor d represents the ration between $T1$, the period for which the signal has the higher voltage $U1$, and the total period T of the signal - $\frac{T1}{T}$; a du

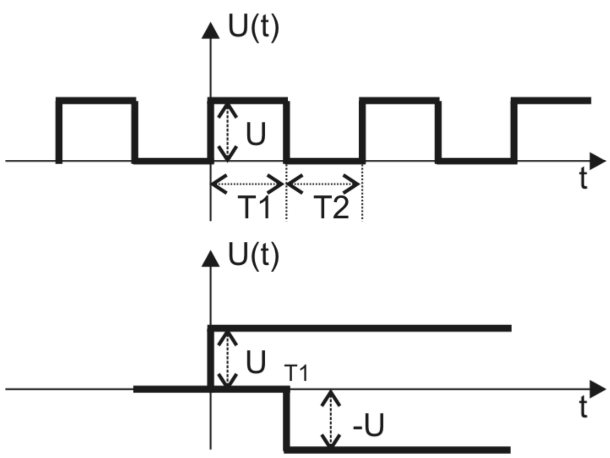

Fig. 1.1 Square-wave signal with its decomposition in step signals

The square wave signal can be represented as of summation of a number of step signals, as depicted in Fig. 1.1. The step signal is defined as follows:

For digital systems using CMOS logic family, the voltage values for logic 0 is $0V$, while for logic 1 is $V_{dd} = U$, with typical values for $U \in (0.6V, 5V)$. The associate square signals can be seen as the summation of two step signals:

$$U_{rise} = \begin{cases} 0, & t < 0 \\ U, & t \geq 0 \end{cases} \tag{1.1}$$

$$U_{fall} = \begin{cases} 0, & t < T1 \\ -U, & t \geq T1 \end{cases} \tag{1.2}$$

1.2.2 Low pass RC circuits

The low pass *RC* circuits is composed of a resistor *R* and a capacitor *C*, with the resistor connected to the input signal and the capacitor connected to the ground - Fig 1.2. The following equations describe the low pass *RC* circuit:

$$U_i = U_R + U_C \tag{1.3}$$

$$U_R = i_R \times R \tag{1.4}$$

$$i_C = C \times \frac{dU_C}{dt} \tag{1.5}$$

$$i_R = i_C \tag{1.6}$$

$$U_o = U_C \tag{1.7}$$

Therefore, in order to determine the output voltage for the low pass *RC* circuit is determined by the following first order differential equation:

$$U_i = RC \times \frac{dU_o}{dt} + U_o \tag{1.8}$$

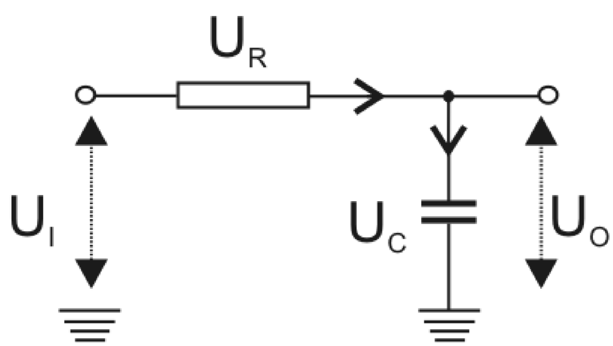

Fig. 1.2 Low pass RC filter

The response of the *RC* low pass circuit to a step signal si given by the following equation:

$$U_o = U2 + (U1 - U2) \times (1 - e^{-\frac{t}{RC}}) \tag{1.9}$$

For the step signal given by equation (1.1), the response of the low pass filter will be:

$$U_o = \begin{cases} 0, & t < 0 \\ U(1 - e^{-\frac{t}{RC}}), & t \geq 0 \end{cases} \tag{1.10}$$

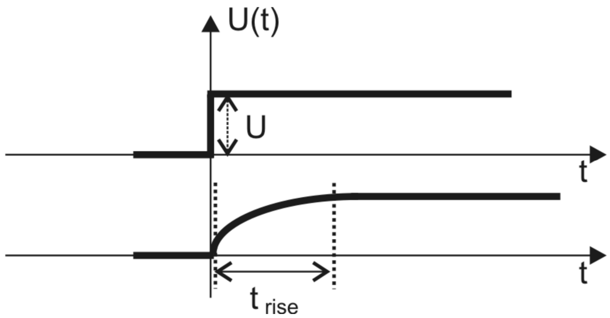

Fig. 1.3 Response of the low pass RC signal to a step signal input

The response of the *RC* low-pass filter is depicted in Fig. 1.3 .The rising time is derived as the difference $t_2 - t_1$, where $U_o(t_2) = 0.9U$ and $U_o(t_1) = 0.1U$. Therefore, the rising time $t_{rise} = RC \times \ln 9 \approx 2.2RC$. Similar approach is used for the fall step signal component in the square wave signal, with $t_{fall} \approx 2.2RC$

Considering a square wave signal used in digital systems composed of CMOS gates, with a period $T = T1 + T2$, with $T1$ the period for which the signal has the value U, and $T2$ the period for which the signal has the value 0, the output response of the low-pass RC circuit will depend on the *RC* constant:

- If $T1 > 2.2RC$, then the output will have enough time to closely reach the amplitude U. Similar, for $T2 > 2.2RC$. In this case the output signal will be delayed with respect to the input.
- If $T1 < 2.2RC$, then the output will reach a voltage $U_{max} = U_o(T1)$.

The response of the low pass RC is depicted in Fig.1.4.

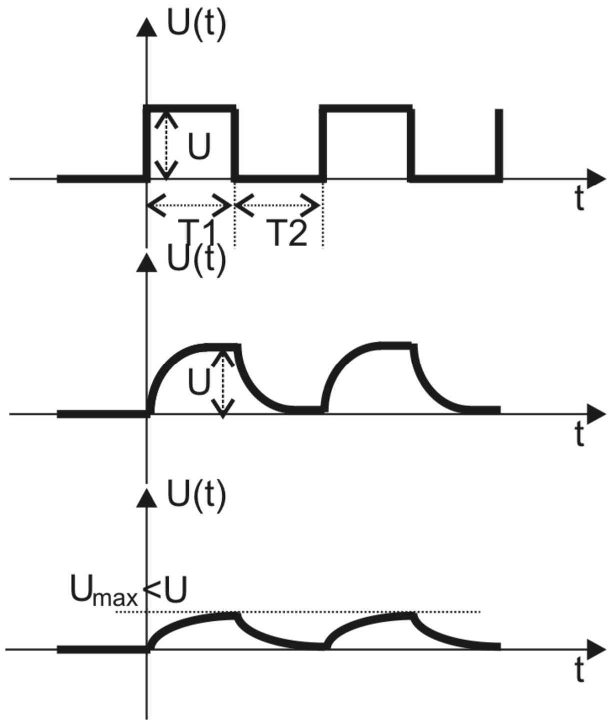

Fig. 1.4 Response of the low pass RC signal to a square wave signal, when $2.2 \times RC < T$, and when $2.2 \times RC > T$

1.2.3 High pass RC circuits

The high pass *RC* circuits is composed of a resistor *R* and a capacitor *C*, with the resistor connected to the ground and the capacitor connected to the input signal 1.5. The following equations describe the low pass *RC* circuit:

$$U_i = U_R + U_C \tag{1.11}$$

$$U_R = i_R \times R \tag{1.12}$$

$$U_C = \frac{1}{C} \times \int i_C dt + U_c(0) \tag{1.13}$$

$$i_R = i_C \tag{1.14}$$

$$U_o = U_R \tag{1.15}$$

Therefore, in order to determine the output voltage for the high pass *RC* circuit, we must solve the following first order differential equation:

$$U_i = \frac{1}{RC} \times \int U_o dt + U_o + U_c(0) \tag{1.16}$$

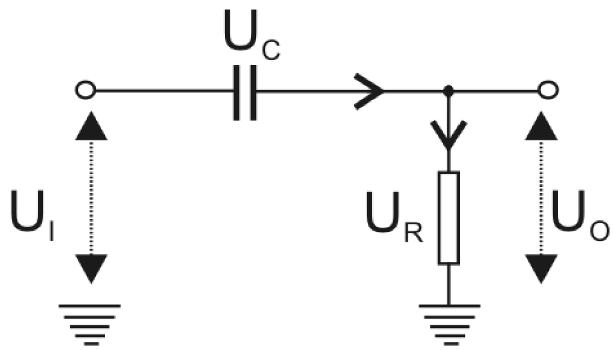

Fig. 1.5 High pass RC filter

For the step signal given by equation (1.1), the response of the high pass filter will be:

$$U_o = \begin{cases} 0, & t < 0 \\ U \times e^{-\frac{t}{RC}}, & t \geq 0 \end{cases} \tag{1.17}$$

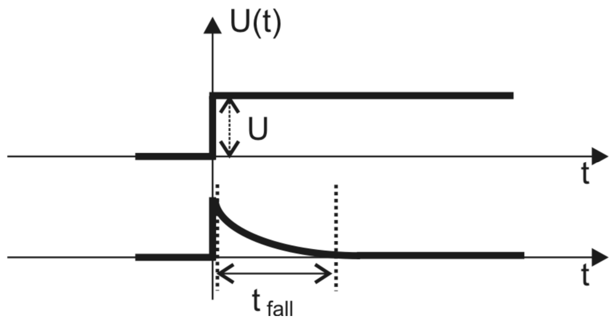

Fig. 1.6 Response of the high pass RC signal to a step signal input

The response of the *RC* high-pass filter is depicted in Fig. .The falling time is derived as the difference $t_2 - t_1$, where $U_o(t_2) = 0.1U$ and $U_o(t_2) = 0.9U$. Therefore, the falling time $t_{fall} = RC \times \ln 9 \approx 2.2RC$. Similar approach is used for the fall step signal component in the square wave signal, with $t_{rise} \approx 2.2RC$

Considering a square wave signal used in digital systems composed of CMOS gates, with a period $T = T1 + T2$, with $T1$ the period for which the signal has the value U, and $T2$ the period for which the signal has the value 0, the output response of the low-pass RC circuit will depend on the *RC* constant:

- If $T1 > 2.2RC$, then the output will have enough time to closely reach the value 0. Similar, for $T2 > 2.2RC$. In this case the output signal will be attenuated with respect to the input signal.

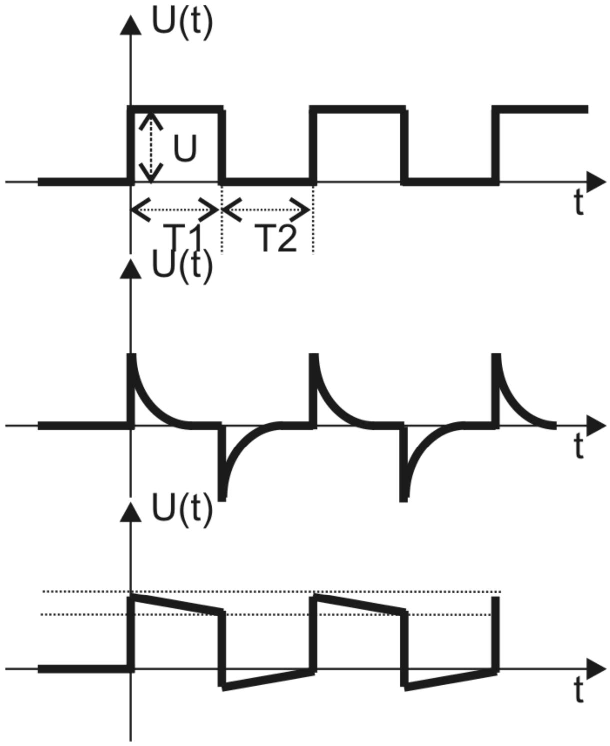

Fig. 1.7 Response of the high pass RC signal to a square wave signal, when $2.2 \times RC > T$, and when $2.2 \times RC < T$

- If $T1 < 2.2RC$, then the output will reach a voltage $U_{max} = U_o(T1)$.

  The response of the high pass RC is depicted in Fig.1.7.

1.3 Lab assignments

1.3.1 Low pass RC circuits

1. Implement the low pass RC circuit on the breadboard using the following values for resistors and capacitors:
   - $R1 = 330\Omega, C1 = 470pF$
   - $R1 = 330\Omega, C1 = 3.3nF$
   - $R1 = 1k\Omega, C1 = 470pF$
   - $R1 = 1k\Omega, C1 = 3.3nF$

2. Generate square wave signals, with amplitude $U = 3V$, duty factor 0.5, and the following frequencies: $F1 = 100KHz$, $F2 = 500KHz$ and $F3 = 1MHz$. Check with one scope probe the amplitude, duty factor and the frequency of the generated square wave signals.
3. Compute the $\tau = RC$ time constant of the low pass *RC* circuit. Compute the response of the four low pass *RC* circuits to the three input signals.
4. Connect the signal output from the signal generator to the low pass *RC* circuit. Scope both the input signal and the output signal. Measure the amplitude and the delay characteristics of the output signal.
5. Draw the waveforms that appear on the oscilloscope screen for both the input and the output signals for the low pass RC.

1.3.2 High pass RC circuits

1. Implement the high pass RC circuit on the breadboard using the following values for resistors and capacitors:
   - $R1 = 330\Omega, C1 = 470pF$
   - $R1 = 330\Omega, C1 = 3.3nF$
   - $R1 = 1k\Omega, C1 = 470pF$
   - $R1 = 1k\Omega, C1 = 3.3nF$
2. Generate square wave signals, with amplitude $U = 3V$, duty factor 0.5, and the following frequencies: $F1 = 100KHz$, $F2 = 500KHz$ and $F3 = 1MHz$. Check with one scope probe the amplitude, duty factor and the frequency of the generated square wave signals.
3. Compute the $\tau = RC$ time constant of the high pass *RC* circuit. Compute the response of the four high pass *RC* circuits to the three input signals.
4. Connect the signal output from the signal generator to the high pass *RC* circuit. Scope both the input signal and the output signal. Measure the amplitude and the delay characteristics of the output signal.
5. Draw the waveforms that appear on the oscilloscope screen for both the input and the output signals for the high pass *RC*.

1.4 References

1. Rabaey, A. Chandrakasan, B. Nikolic ”Digital Integrated Circuits: A Design Perspective”, Prentice-Hall, 2002
2. R. Jacob Baker ”CMOS: Circuit Design, Layout, and Simulation”, IEEE-Wiley Interscience, 2008
3. Mircea Stratulat ”Circuite Digitale” ,Editura Politehnica, 2012