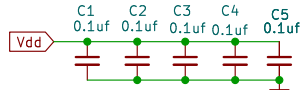
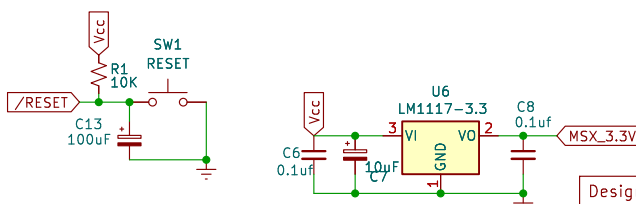
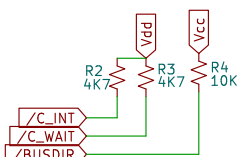
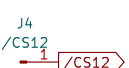
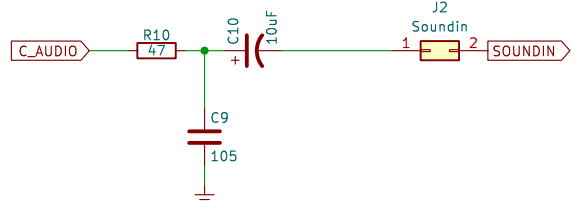
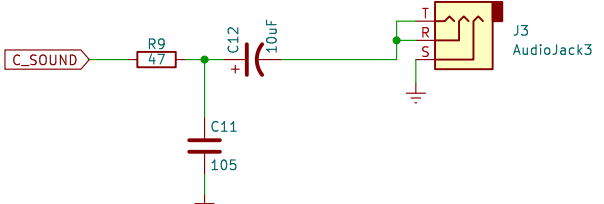
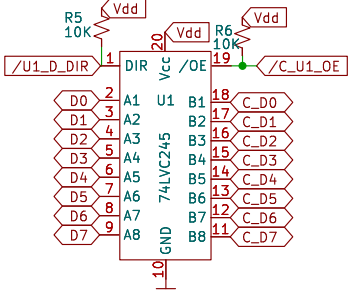
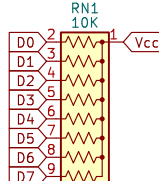
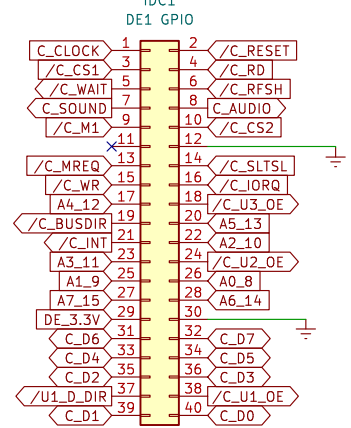
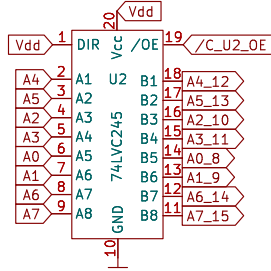
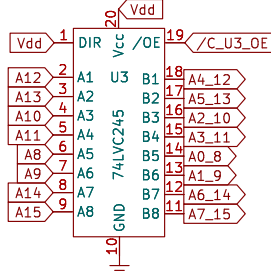
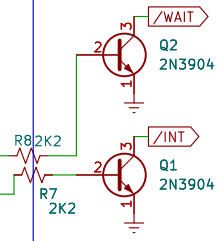
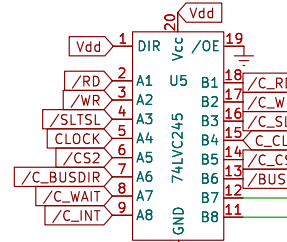
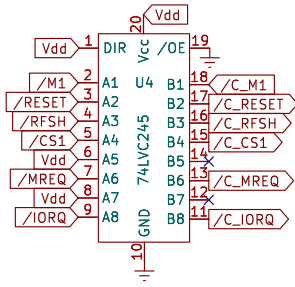
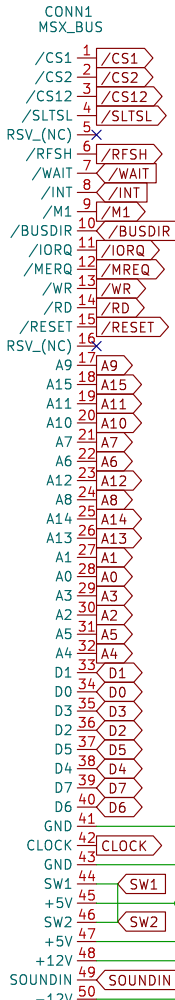


PIN mappings was carefully designed to support both DE0 and DE1 GPIO connector.
DE0 board has 2xCLK_IN (1,3) and 2xCLK_OUT (19,21) pins, which are not present on DE1. These pins cannot operate as bi-directional IO signals, and therefore they were assigned to specific functions in the interface - the direction of their signals must not be changed.

/C_U1_D_OE pin must be asserted for any write and read operation.

v2.0 Bug: CS2 & RFSH sharing same pin but OE is grounded. RFSH should not be wired (soldered) in U4 to avoid issues.



J5 controls the power source for the interface.
If DE0/DE1 is selected, it will be powered directly by DE0/DE1 pin 29
If MSX is selected, it will be powered by the MSX with 3.3v converted from 5V by U6

Designed for MSX and Terasic DE0 & DE1 IDC connector pinout mapped for Altera DE1 FPGA Development Board Cartridge for MSX Computers that expose the MSX BUS to 3.3v systems with voltage conversion	
RCC ● 2024	
Sheet: /	
File: MSX_FPGA_Hat.kicad_sch	
Title: MSX FPGA Hat	
Size: A4	Date: 2024-02-03
KiCad E.D.A. 8.0.8	Rev: 2.01
	Id: 1/1