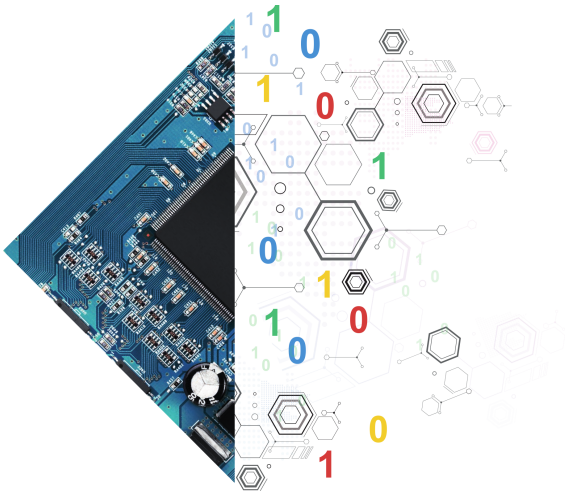


HW/SW Co-Design

SCF 2024

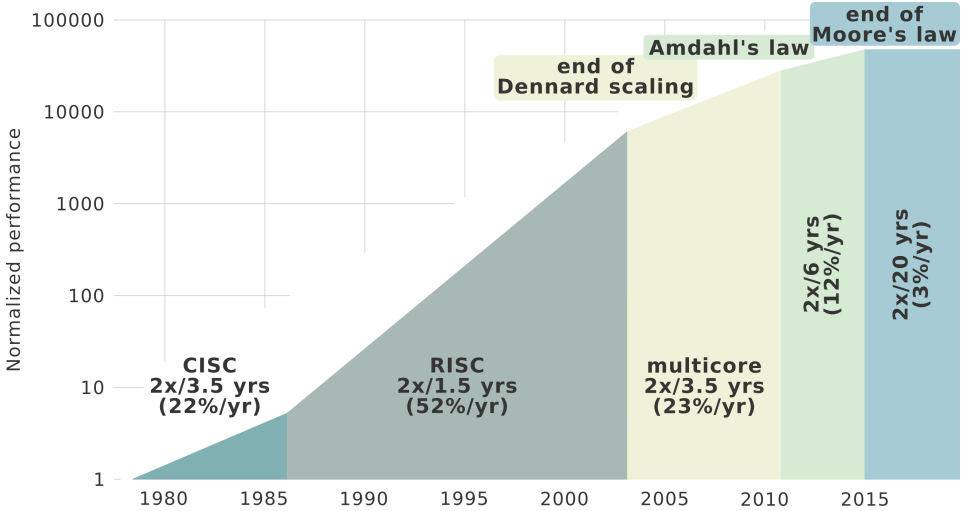
Alberto Dassatti

heig-vd
HAUTE ÉCOLE
D'INGÉNIERIE ET DE GESTION
DU CANTON DE VAUD
www.heig-vd.ch

May 2024

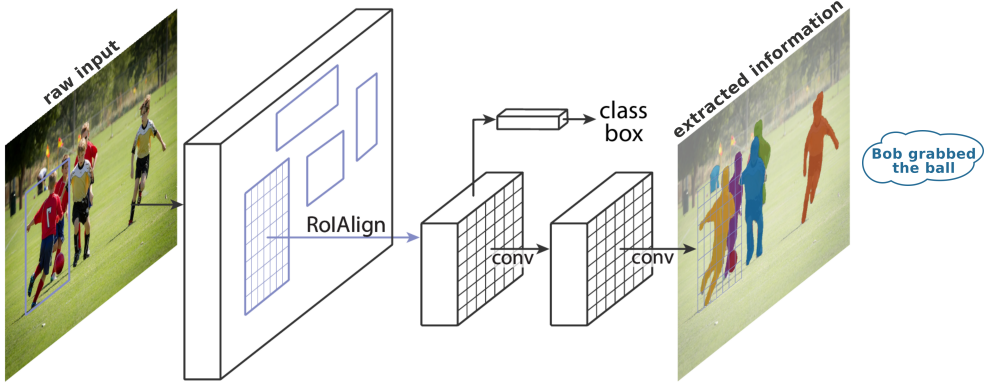
energy efficient
fast
versatile
innovation friendly

CPU PERFORMANCE IS STAGNATING



[Turing Award Lecture Hennessy, Patterson 2018]

Data and processing



500 million tweets

4 million hours of content on YouTube

4.3 billion Facebook entries

3.6 billion Instagram pictures

6 billion Google searches

205 billion e-mails

[He *et al.*, 2018]

COMPUTATIONAL DEMAND IS INCREASING

Processing is Power Hungry

[Jeopardy! quiz show. 2011]

Processing is Power Hungry

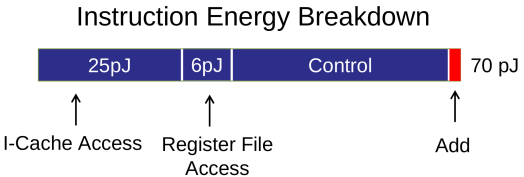
[Jeopardy! quiz show. 2011]

Software: Energy Cost of Computation is Minimal

```
ADD R3 R1 R2 // R3 = R1 + R2
```

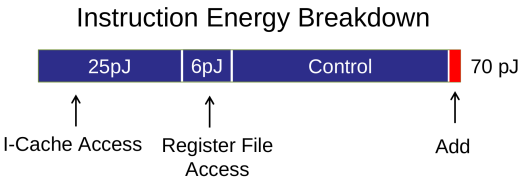
Software: Energy Cost of Computation is Minimal

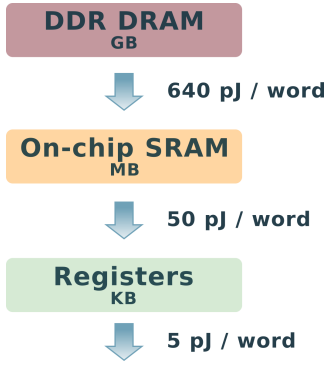
`ADD R3 R1 R2` // R3 = R1 + R2



Software: Energy Cost of Computation is Minimal

```
LOAD R1 MEM_ADDR1
LOAD R2 MEM_ADDR2
ADD R3 R1 R2 // R3 = R1 + R2
STORE R3 MEM_ADDR3
```





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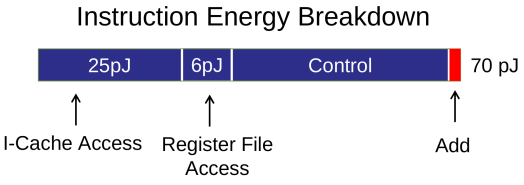
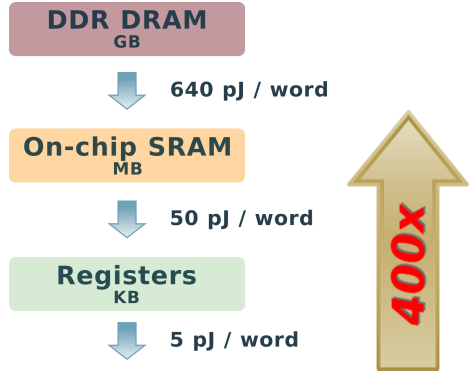
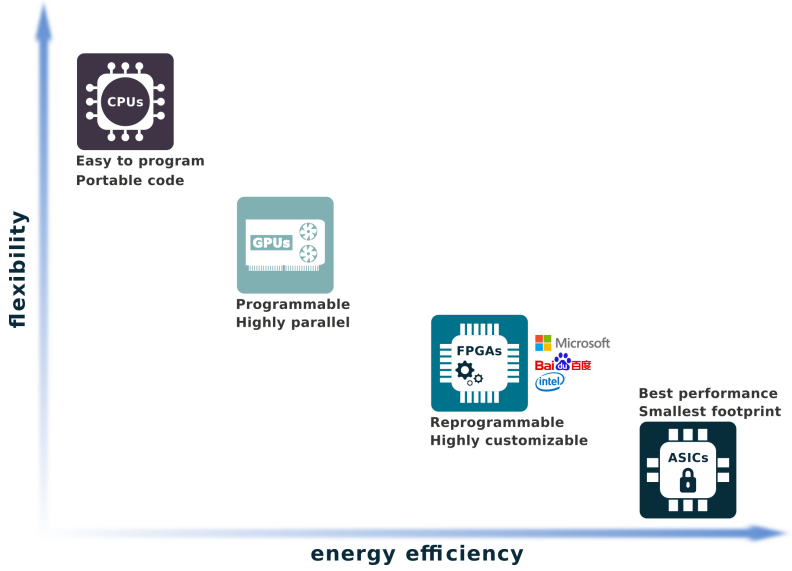




[Horowitz 2014]

TECHNOLOGY VIEW



Classical approach

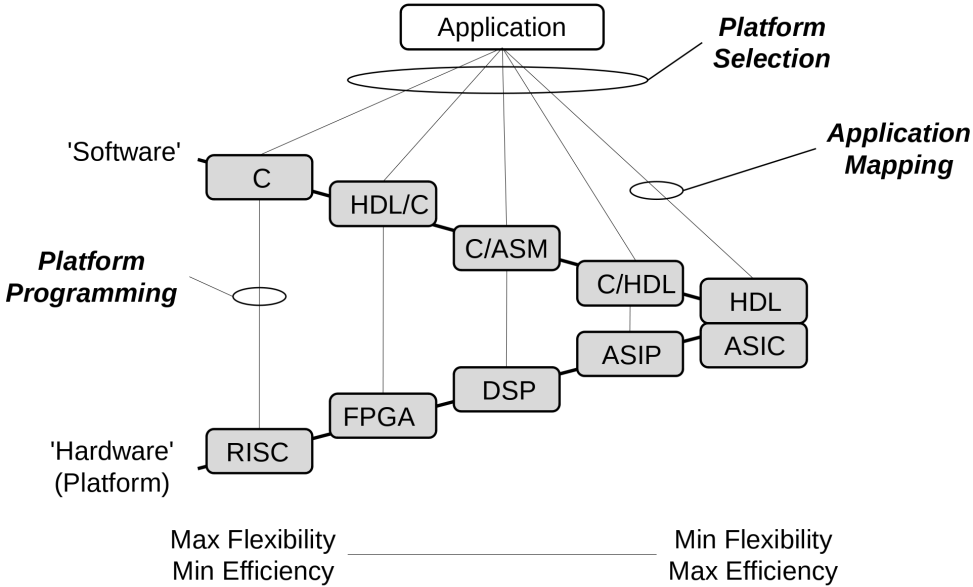
Improve Performance
Improve Energy Efficiency
Reduce Power Density

Implement more in Hardware

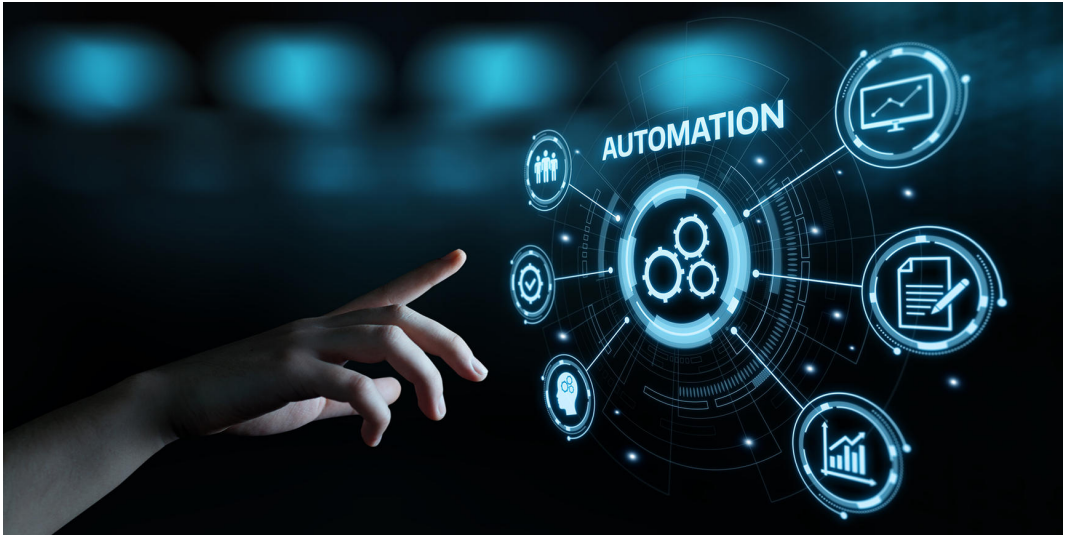
Manage Design Complexity
Reduce Design Cost
Stick to Design Schedule
Handle Deep Submicron

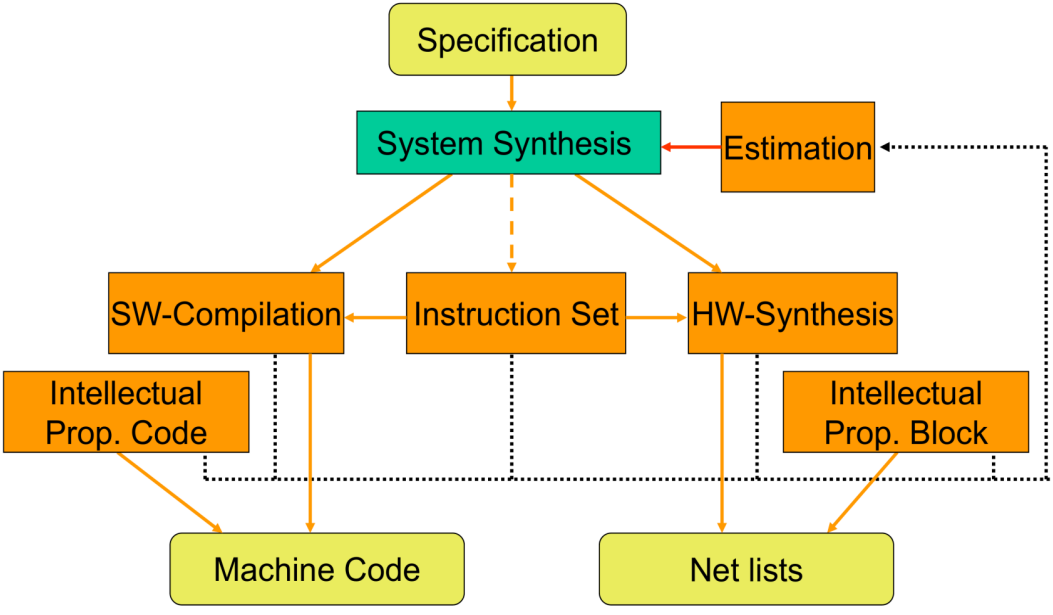
Implement more in Software

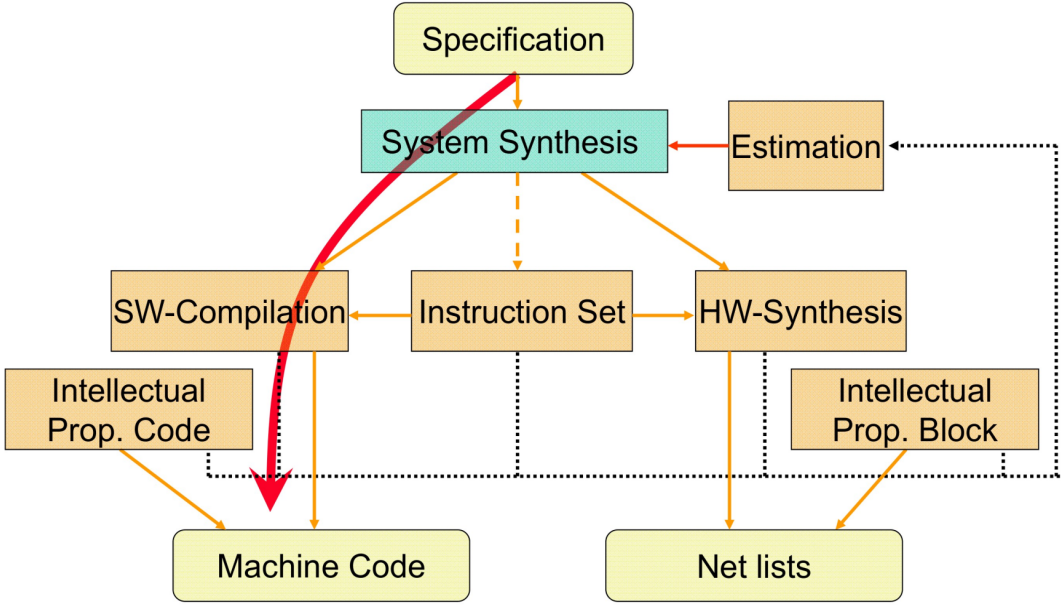
Classical approach




CON
TRACT
Agreement made this ____day of
between
(hereinafter called "First Party"), residing
and
(hereinafter called "Second Party"), residing
WITNESSETH THAT,
1. DESCRIPTION OF WORK.
2. PRICE AND PAYMENT SCHEDULE.
3. DATE OF DELIVERY:
4. WORK TRANSFER.


AUTOMATION


Specification
System Synthesis
Estimation
SW-Compilation
Instruction Set
HW-Synthesis
Intellectual Prop. Code
Intellectual Prop. Block
Machine Code
Net lists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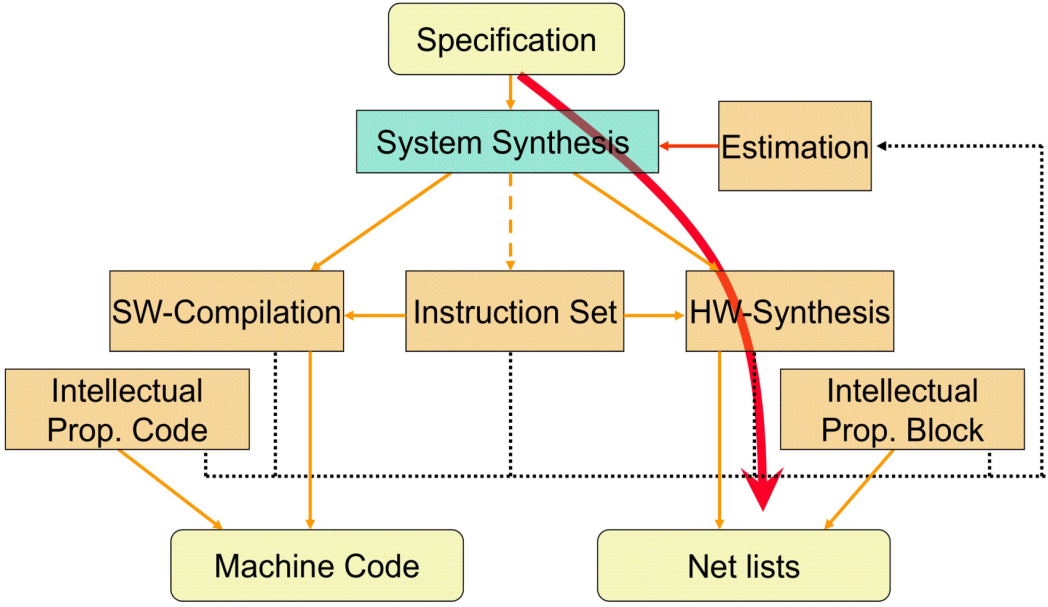
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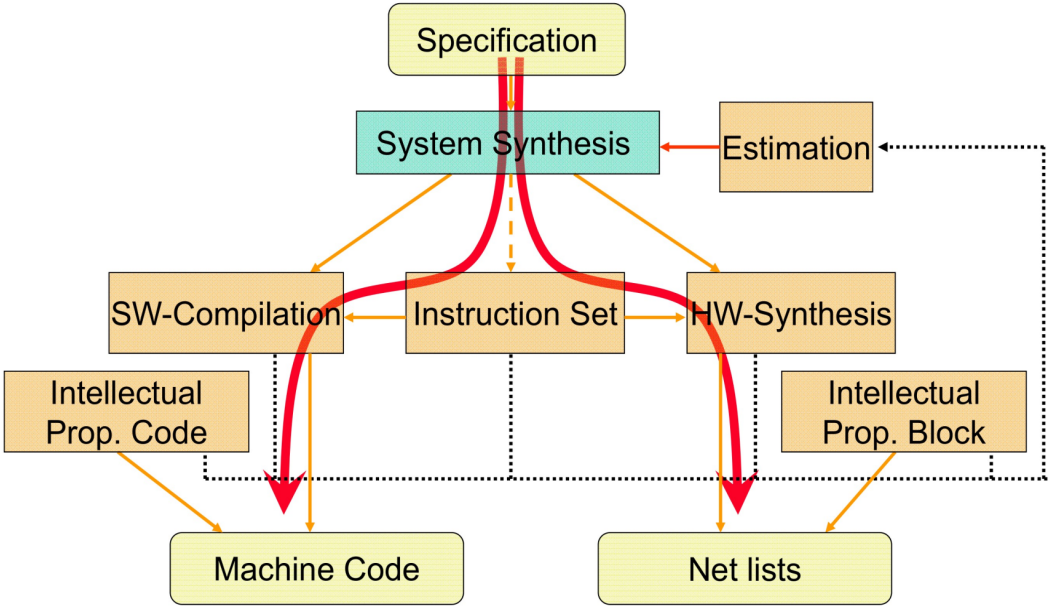
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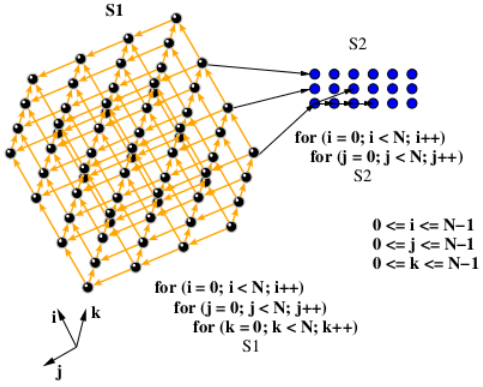
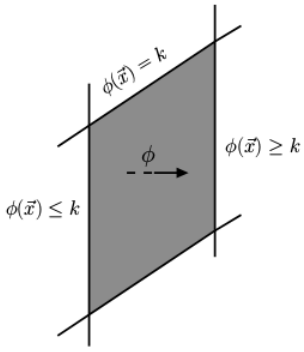
KEY TECHNOLOGIES

- Domain Specific Languages - DSL
- High Level Syntesis - HLS
- Formal methods
- Data oriented Design - DOD
- In-memory computing

DSL

- Capture the Expert's ideas - productivity and abstractions
- Decupling computations and scheduling





HLS

- HDLs are too low level
- Use high level languages (C/C++; SYCL, OpenCL) to capture the computations
- Not fully automated, yet.
- There is a need for a run-time coordination
- Model the CPU-Accelerator paradigm, not much more

- Middle-ground: CGRAs (TFA)

Formal methods

- Math is super useful as abstraction (3k years proven!)
- Remove the need of simulation
- Remove debugging and tooling!
- They can be used for both design and verification
- We need more of them!

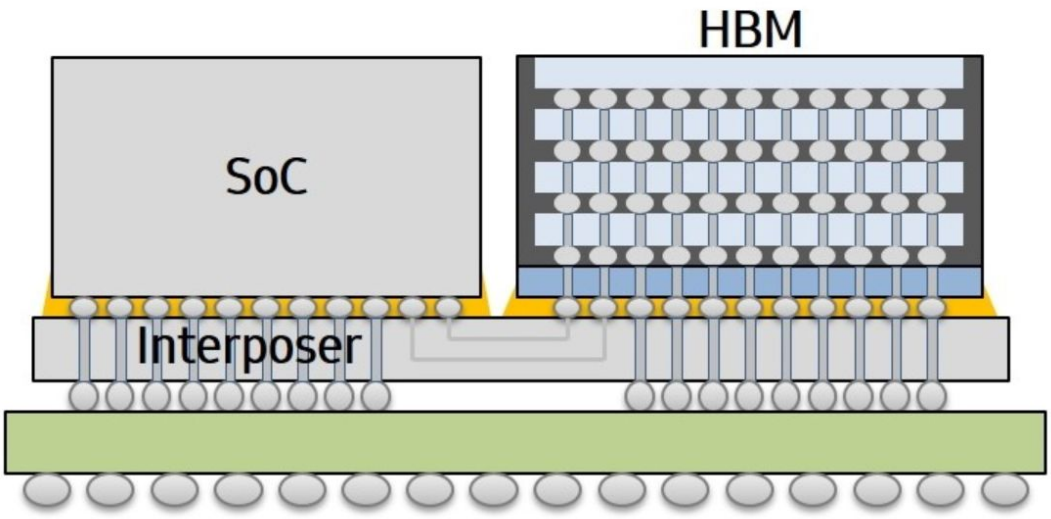
DoD

- Most code is written in OO;
- Programmers are trained to think in OO, but the execution overhead is huge
- DoD pushes to think about data and transformations
- Very popular in Game design
- Great performance
- Adoption requires a mental shift, new tools, and methodologies

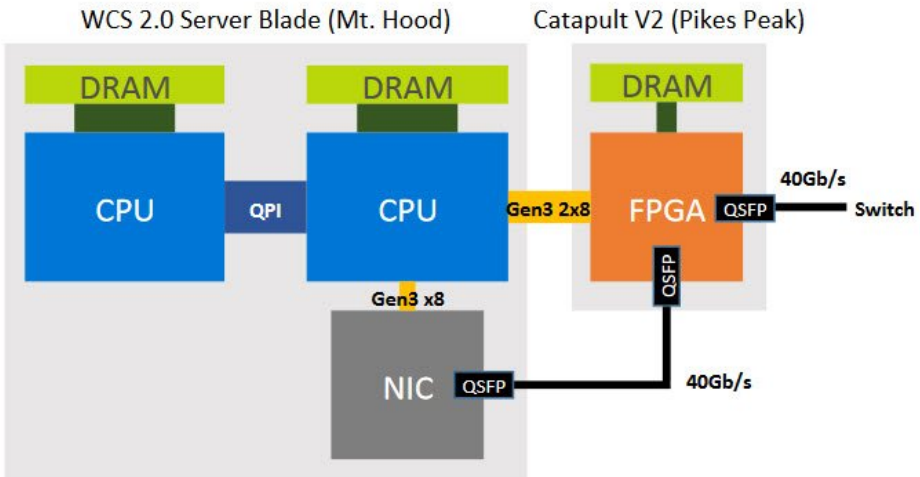
In-Memory Computing

- Instead of moving data, move processing (City center analogy)
- Requires new devices and abstractions (Smart-Drive)
- Requires new technological processes
- The energy gain can be huge
- Poor-man solutions: on-the-wire processing

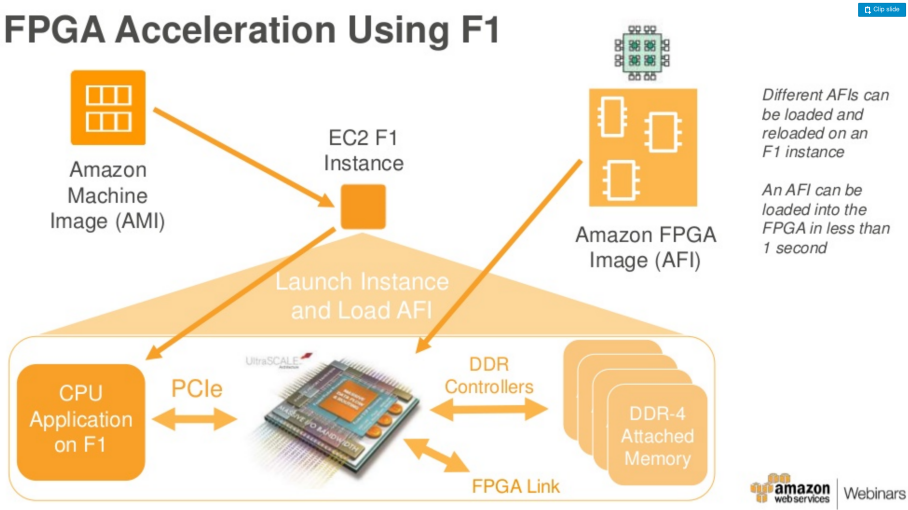
Real world examples: Memory integration



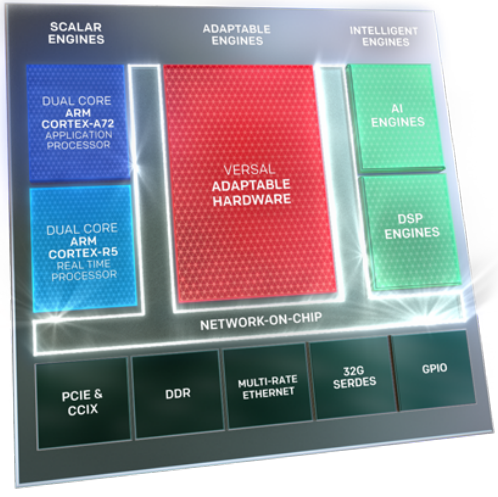
REAL WORLD EXAMPLES: MS CATAPULT



REAL WORLD EXAMPLES: AMAZON F1



Real world examples: Xilinx Versal



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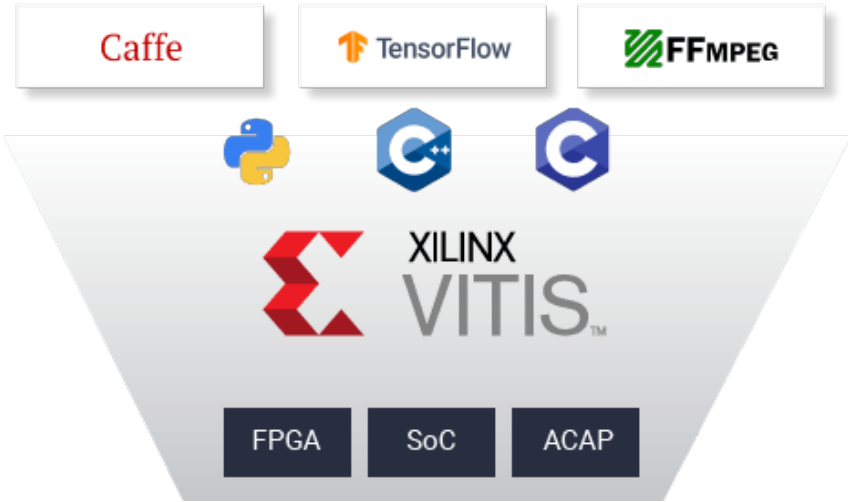

VALUE PROPOSITION

- Innovation friendly
- Energy efficient
- Versatile
- Fast