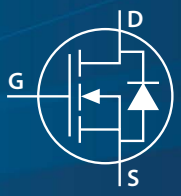
EPC2040 – Enhancement Mode Power Transistor

V_{DS}, 15 V
$R_{DS(on)}$, 30 mΩ
I_D, 3.4 A



EFFICIENT POWER CONVERSION

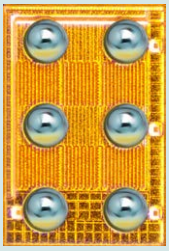
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	15	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	18	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 220°C/W)	3.4	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	28	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	–4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	5.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	39	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	97	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details



EPC2040 eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 0.85 mm x 1.2 mm

Applications

- High Speed DC-DC conversion
- Lidar/Pulsed Power Applications
- Lidar for Augmented Reality Applications

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	15			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 12 V, V_{GS} = 0 V		10	250	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	1.2	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		10	250	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 1.5 A		24	30	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		2.2		V

All measurements were done with substrate connected to source.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 6 V, V_{GS} = 0 V		86	105	pF
C_{RSS}	Reverse Transfer Capacitance			20		
C_{OSS}	Output Capacitance			67	100	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 6 V, V_{GS} = 0 V		106		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			87		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{DS} = 6 V, V_{GS} = 5 V, I_D = 1.5 A		745	925	pC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 6 V, I_D = 1.5 A		230		
Q_{GD}	Gate-to-Drain Charge			140		
$Q_{G(TH)}$	Gate Charge at Threshold			165		
Q_{OSS}	Output Charge	V_{DS} = 6 V, V_{GS} = 0 V		420	630	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 40% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 40% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

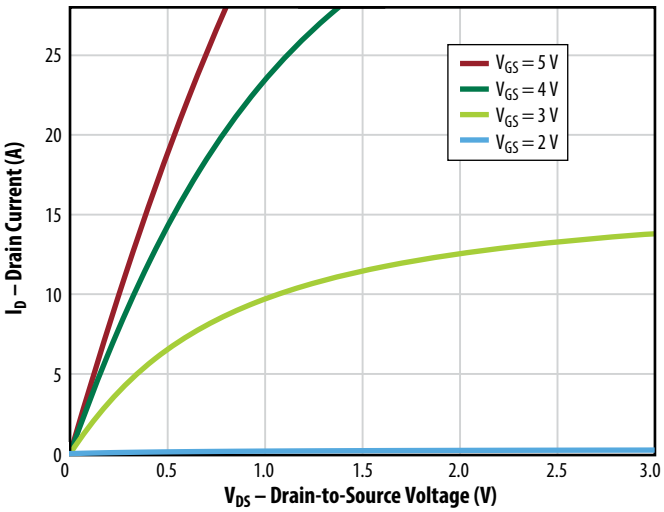


Figure 2: Transfer Characteristics

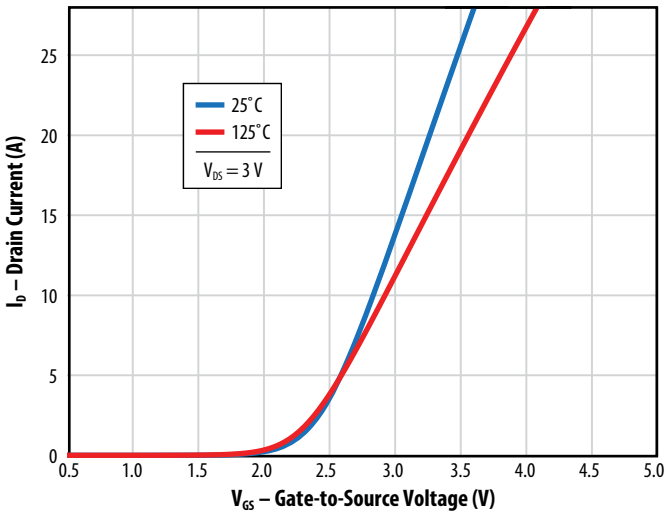


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

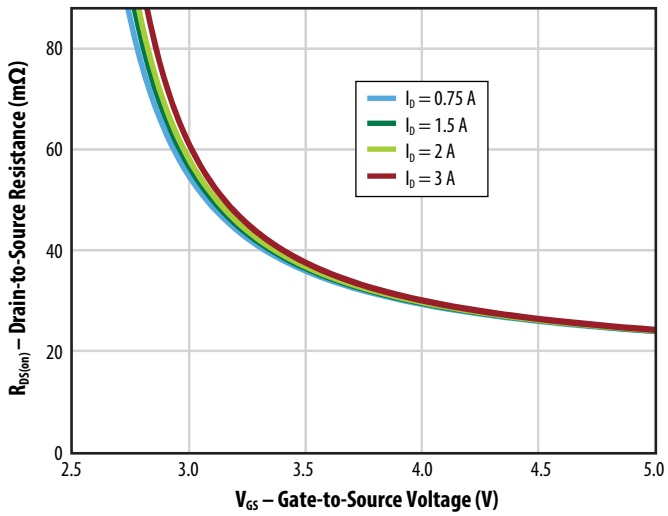


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

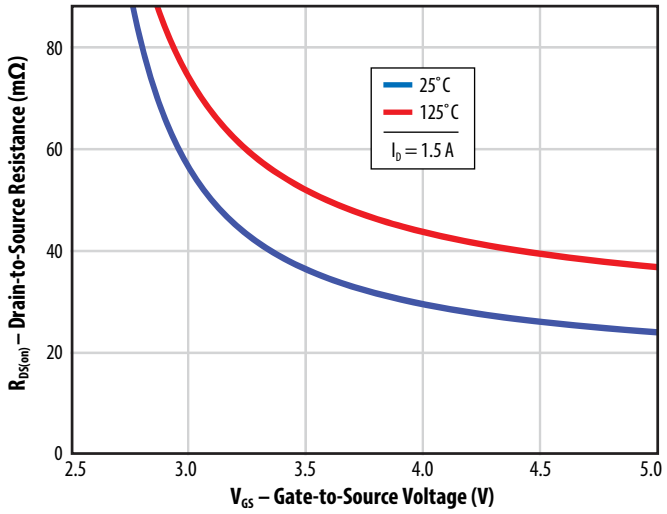


Figure 5a: Capacitance (Linear Scale)

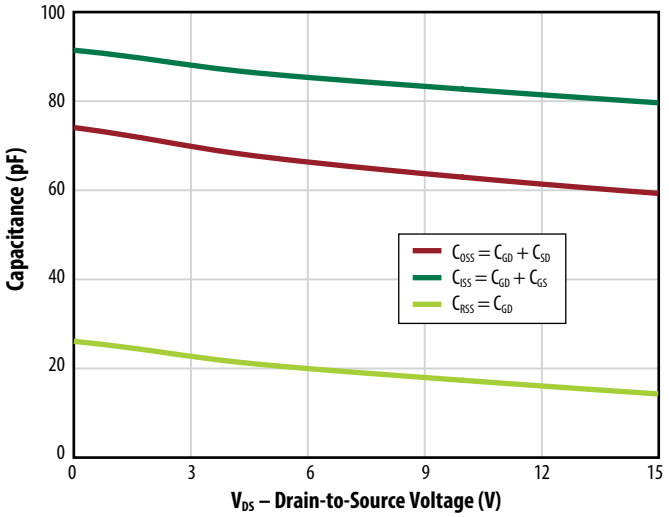


Figure 5b: Capacitance (Log Scale)

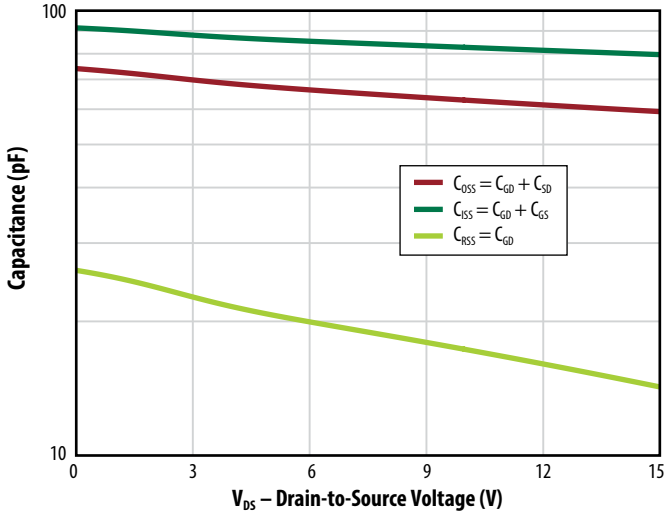


Figure 6: Gate Charge

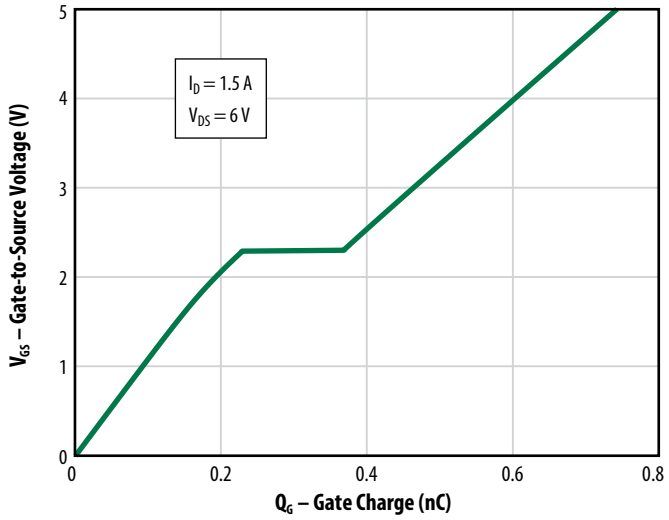


Figure 7: Reverse Drain-Source Characteristics

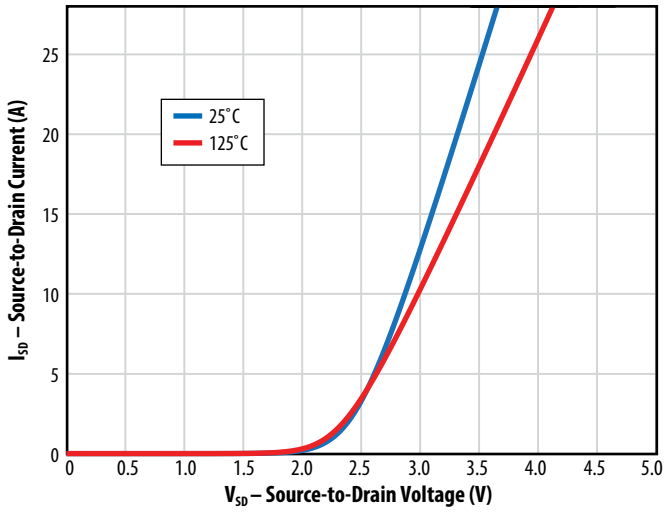


Figure 8: Normalized On-State Resistance vs. Temperature

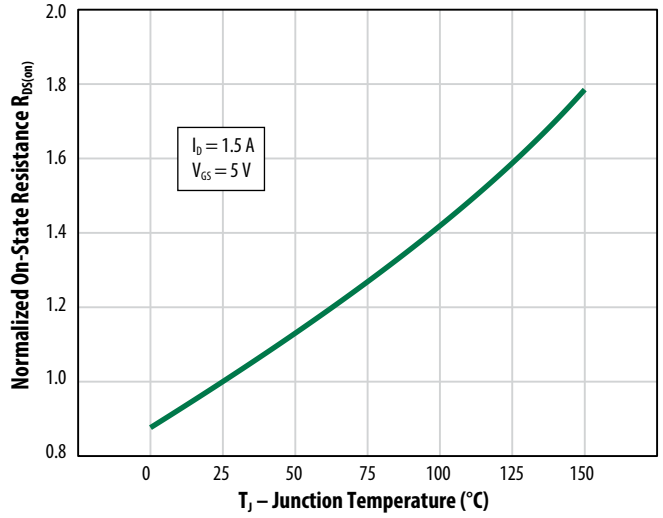
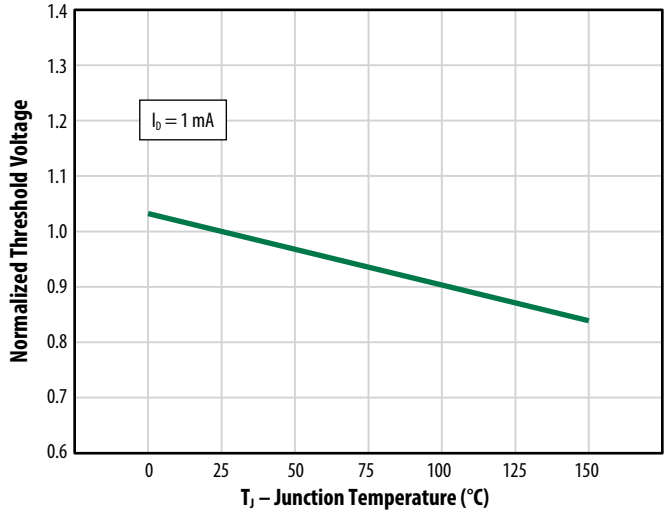


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shortened to source.

Figure 10: Safe Operating Area

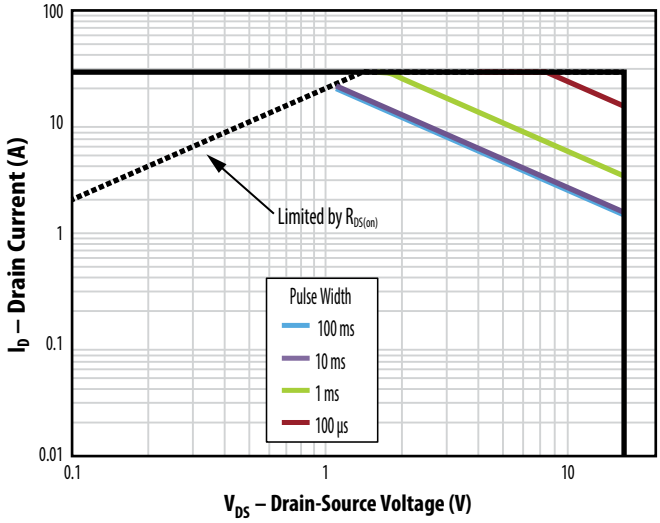
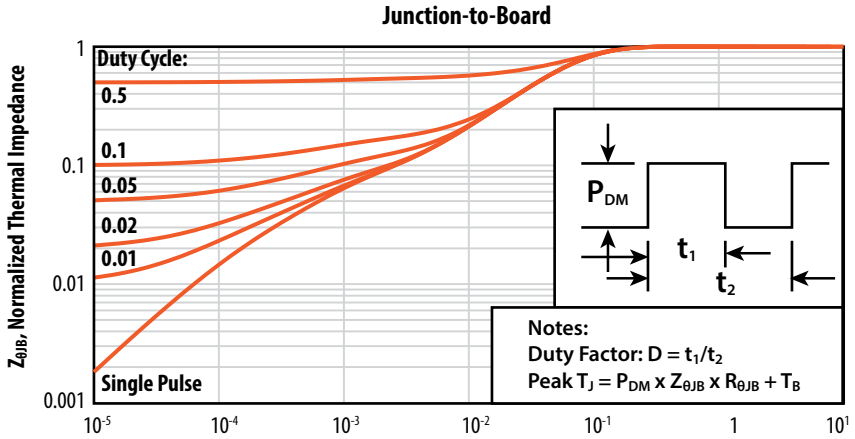
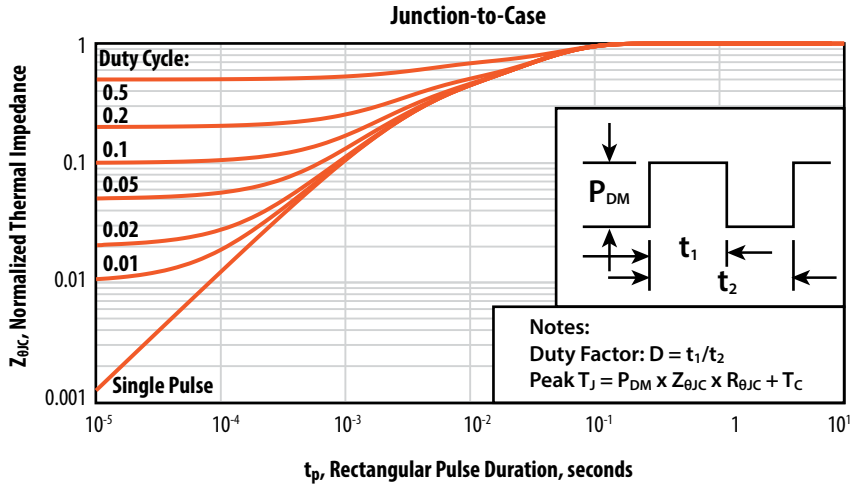


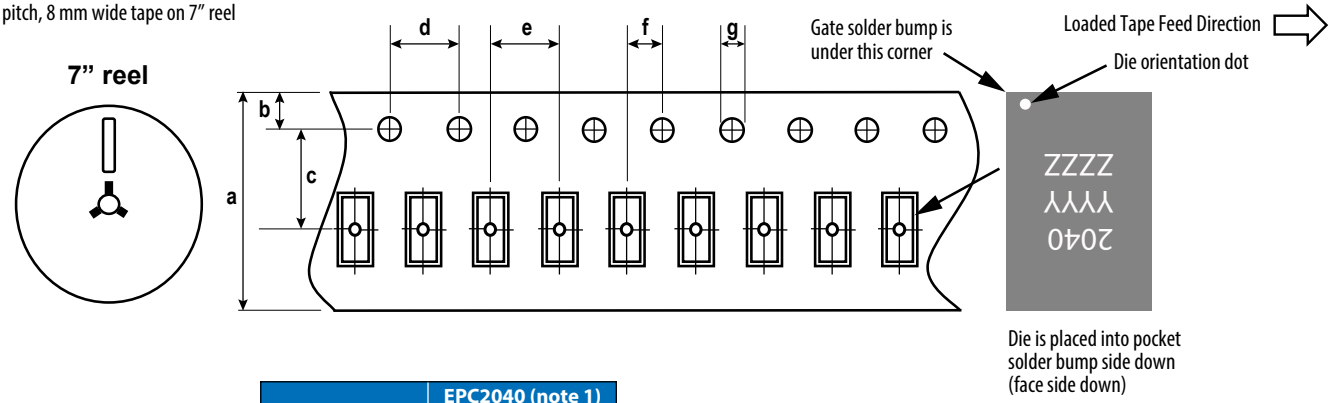
Figure 11: Transient Thermal Response Curves





TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

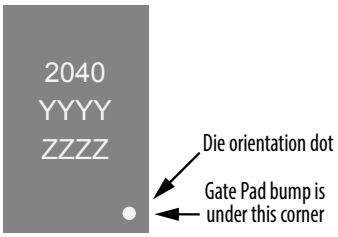


	EPC2040 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

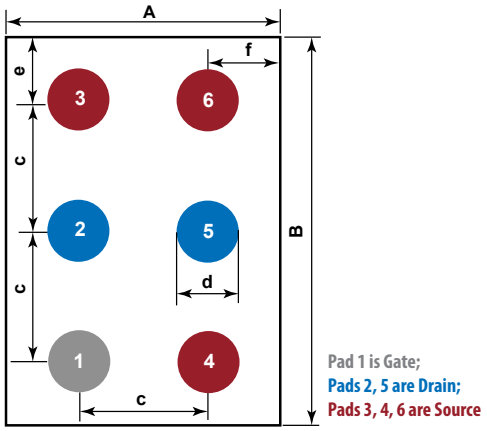
DIE MARKINGS

Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking line 3
EPC2040	2040	YYYY	ZZZZ



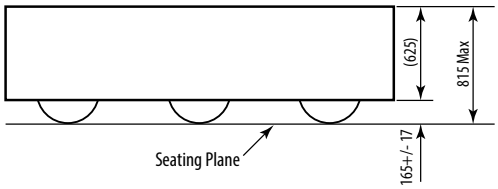
DIE OUTLINE

Solder Bump View



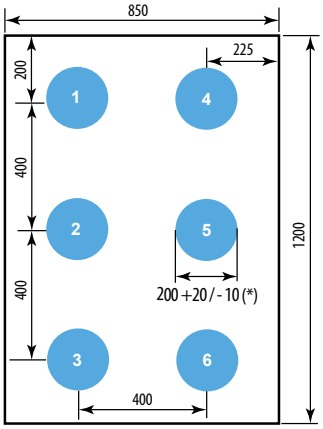
DIM	Micrometers		
	MIN	Nominal	MAX
A	820	850	880
B	1170	1200	1230
c		400	
d	187	208	229
e	185	200	215
f	210	225	240

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



* minimum 190

The land pattern is solder mask defined

Solder mask is 10 µm smaller per side than bump

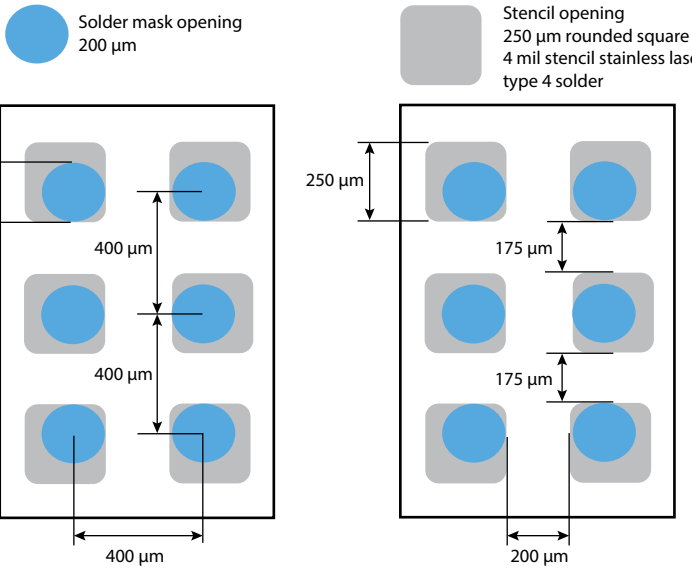
Pad 1 is Gate;

Pads 2 , 5 are Drain;

Pads 3, 4, 6 are Source

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx