



A Report on

BUGBUSTER: 2024

A National Level Contest on

Electronic Circuit Troubleshooting

(Redefining Circuit Troubleshooting, One Bug at a Time)

S.P.I.T. I.E.T.E.

In Association with

S.P.I.T. I.E.E.E. and S.P.I.T. AICTE Idea Lab

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Industry Partners

Cybermotion Pvt. Ltd., Bangalore

Log9 Materials Pvt. Ltd., Bangalore

Duration:

6th April 2024 to 13th April 2024

Faculty Coordinator. Dr. P. V. Kasambe, Assistant Professor

Convenor: Dr. Reena Kumbhare, HoD

Department of Electronics and Telecommunication

Parton: Dr. B. N. Chaudhari, Principal

Venue: Room No. 003 & 001 and Online Google Meet

Bug Buster Phase 1: Orientation and Learning Enrichment Workshop

Date: 6th April 2024.

Organised by: I.E.T.E. S.P.I.T. in association with I.E.E.E. S.P.I.T., Cybermotion Pvt. Ltd. Bangalore and Log9 Materials Pvt. Ltd. Bangalore.

Introduction:

Phase 1 of Bug Busters marked the beginning of a journey enriched with comprehensive learning experiences. Participants engaged in an orientation session to familiarize themselves with the event's structure, rules, and evaluation criteria for Phase 2. Industry experts from Cybermotion Technologies provided illuminating presentations on utilizing Proteus Software, complemented by insights from Mr. Chirag Shah on PCB Schematic and Layout. Dr. Prashant Kasambe orchestrated the workshop, ensuring seamless learning flow.

Event Schedule:

Sr. No.	Speaker	Timing	Matter of Discussion
1.	Dr. Prashant Kasambe	5:00 pm to 5:30 pm	Participants were acquainted with event details, timeline, rules, and the evaluation criteria for Phase 2.
2.	Experts from Cybermotion Technologies	5:30 pm to 6:30 pm	Proteus Software intricacies, enriching participants' understanding on the software to be used for simulation.
3.	Mr. Chirag Shah	6:30 pm to 7:00 pm	Mr. Chirag Shah shared invaluable insights on PCB Schematic and Layout, enhancing participants' knowledge.
4.	Dr. Prashant Kasambe	7:00 pm to 8:00 pm	A brief session about using Keil micro-vision and its integration with Proteus for the specific microcontroller.

Phase 1 laid a solid foundation for participants, equipping them with essential skills and insights for effective electronic circuit design and troubleshooting.

Acknowledgements:

Gratitude extended to Organizers, Industry Experts, and Alumni for their contributions. Special thanks to Dr. Prashant Kasambe for workshop facilitation.

The screenshot shows a Google Meet interface. The main window displays a presentation slide titled "Breadboard Prototype" with a photograph of a breadboard circuit. The circuit includes a microcontroller, various resistors, jumper wires, and a small LCD screen. The slide is presented by Chirag Shah. To the right, a grid of participant avatars is visible, including Prashant Kasambe, Sahil Pisal, Chinmay Udyavar, Prajwal, Sahil Tayde, E21 Yash Singh, Shaurya Rane, and Woodrow Gonsalves. The bottom status bar shows the time as 6:44 PM and the meeting ID as oto-onco-dgv.

The screenshot shows a Google Meet interface with a grid of participant avatars. The participants include Chirag Shah, Saksham Dhagekar, Roshan, MUHAMMAD MUSAB BHALJI, 40 Ankit Tejam, Siddharth Doshi, Varun Nigudkar, Vishal Mutha, Prashant Kasambe, Chinmay Udyavar, Prajwal, Shaurya Rane, Bhavik Desai, Achintya Chavan, and Woodrow Gonsalves. The bottom status bar shows the time as 7:50 PM and the meeting ID as oto-onco-dgv.

BugBuster Phase 2: Online Doubt-Solving Session and Resource Provision

Date: 7th April 2024.

Organised by: I.E.T.E. S.P.I.T. in association with I.E.E.E. S.P.I.T.

Introduction:

Phase 2 of Bug Buster 2024 facilitated an online doubt-solving session via Google Meet, conducted from 6 pm to 8 pm. The technical team of Bug Buster 2024 provided assistance to students throughout this phase. In addition to the interactive session, participants were equipped with valuable resources to enhance their understanding and proficiency.

Event Schedule:

Online Doubt-Solving Session (6:00 pm to 8:00pm):

Participants engaged in an interactive doubt-solving session via Google Meet, receiving assistance from the Bug Buster 2024 technical team.

Resource Provision:

Participants gained access to a designated drive link labeled "Study Material," containing curated resources. These resources were tailored to aid participants in navigating both software and electronics crucial for the final competition. The collection included guides such as 'How to Navigate on Proteus' and datasheets relevant to competition electronics.

Phase 2 served as a foundational stage for Bug Buster 2024, ensuring participants were well-prepared and equipped for the challenges ahead.

Bug-Buster Phase 3: Online Evaluation and Elimination Phase

Date: 9th April 2024

Organized by: I.E.T.E. S.P.I.T. in association with I.E.E.E. S.P.I.T.

Introduction:

Bug-Buster Phase 3 marked a significant milestone in the realm of hardware hackathons, as it transitioned into an online format, adapting to the digital age and the challenges posed by the global situation. With a total of 52 teams participating, each comprising 3 members, the event aimed to provide participants with a platform to showcase their troubleshooting skills in hardware simulations, under the guidance of esteemed professionals in the field.

Event Schedule:

Sr. No.	Brief Idea	Timing	Matter of Discussion
1.	Instruction Session	3:00 pm to 3:15 pm	Dr. Prashant Kasambe led an insightful instruction session, laying down the foundation for the tasks ahead and providing participants with the necessary guidance to navigate through the challenges.
2.	Online Simulation Round on Proteus	3:15 pm to 5:15 pm	Participants engaged in an intense online simulation round using Proteus, a virtual environment that allowed them to troubleshoot hardware issues in real-time. This phase tested their ability to diagnose and resolve problems efficiently.
3.	Presentation of the Simulation to Evaluators	5:15 pm to 7:15 pm	After the simulation round, participants showcased their solutions and findings to a panel of evaluators. Each category had its dedicated time slot for presentation, during which participants explained their approaches, demonstrated their solutions, and answered questions from the evaluators. Presentations were judged not only on the effectiveness of the solutions but also on the clarity of communication and depth of understanding demonstrated by the participants.

4.	Final Online Quiz	7:30 pm to 8:00 pm	This phase concluded with a final online quiz, testing participants' theoretical knowledge and understanding of hardware troubleshooting concepts.
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Participant Categories and Evaluators:

In order to ensure a diverse and competitive environment, participants were divided into five categories based on team compositions and organizational purposes. Each category consisted of a diverse mix of teams, fostering an environment of healthy competition and collaboration. The teams of the respective categories were called upon one by one to the specific category (online) meetings. The categories were as follows:

1) Category 1

- Evaluators: Mr. Shahid Shaikh & Mr. Somesh Srivastava

2) Category 2

- Evaluator: Mr. Aniket Nadkarni

3) Category 3

- Evaluator: Mr. Apoorva Limaye

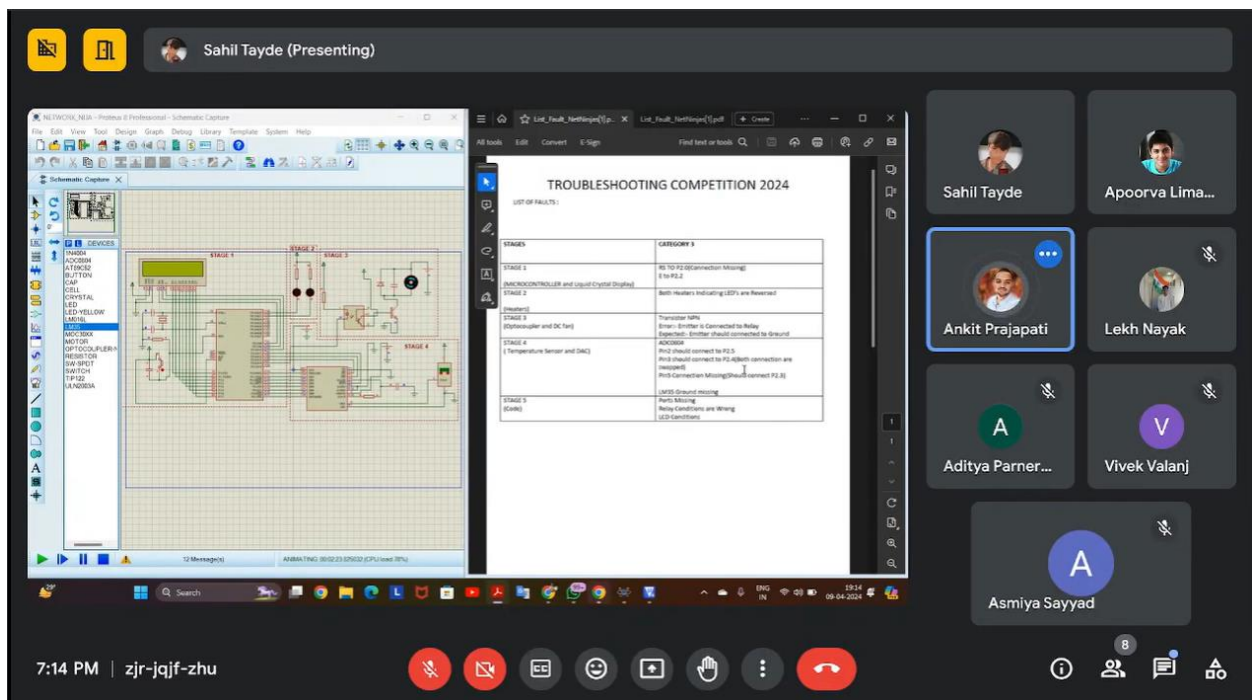
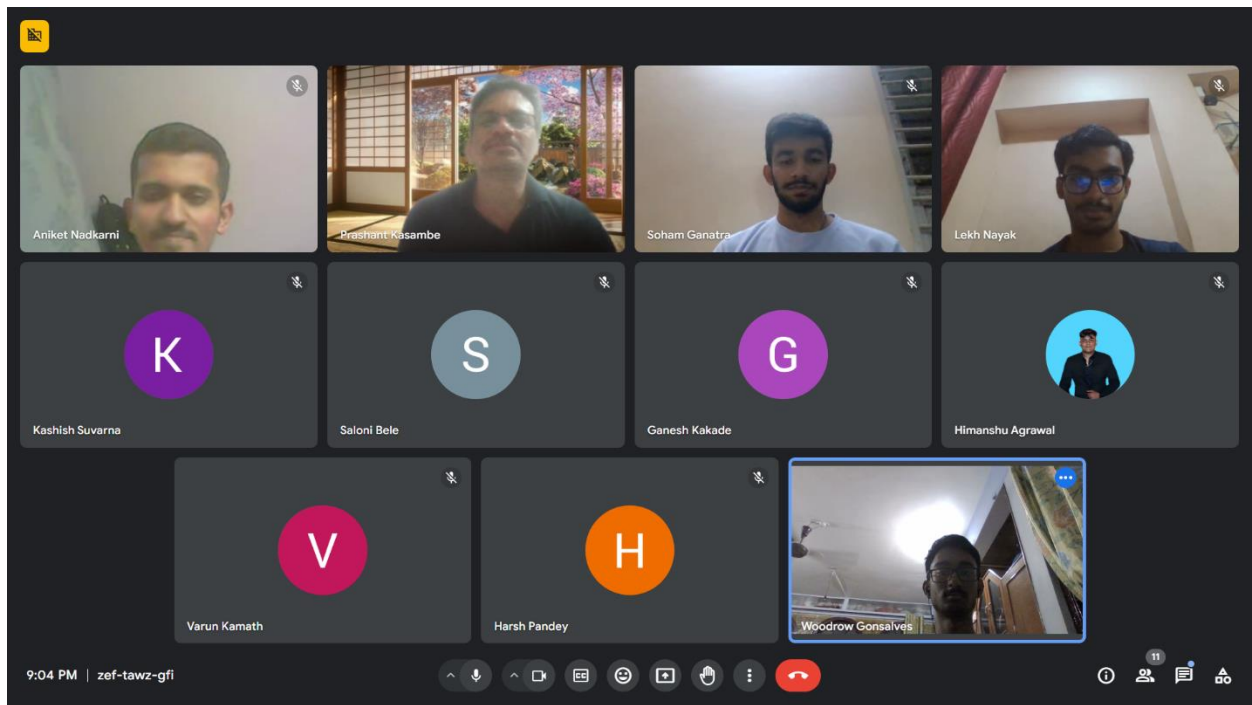
4) Category 4

- Evaluator: Mr. Prabhat Kumar

5) Category 5

- Evaluator: Mr. Varun Mehta

Bug-Buster Phase 3 exemplified resilience and adaptability in the face of challenges, showcasing the potential of online platforms in fostering innovation and collaboration. With a total of 52 teams, each comprising 3 members, the event provided a robust platform for participants to demonstrate their hardware troubleshooting skills.



Bug Busters Phase 4: Final Offline Simulation and Hardware Debugging Round and Declaration of Winners

Date: 13th April 2024

Organised by: I.E.T.E. S.P.I.T. in association with I.E.E.E. S.P.I.T.

Introduction:

Phase 4 was a day full of anticipation and challenges for both the participants and the organisers. As the participants put their knowledge and skills to test, the organizing committees hustled to ensure that every task went by smoothly. The participants had to debug the simulation files, microcontroller codes and faulty PCBs within the time frame, to bag the first prize. The top 18 teams were selected out of 52, who participated in Phase 3.

Phase 4 Schedule:

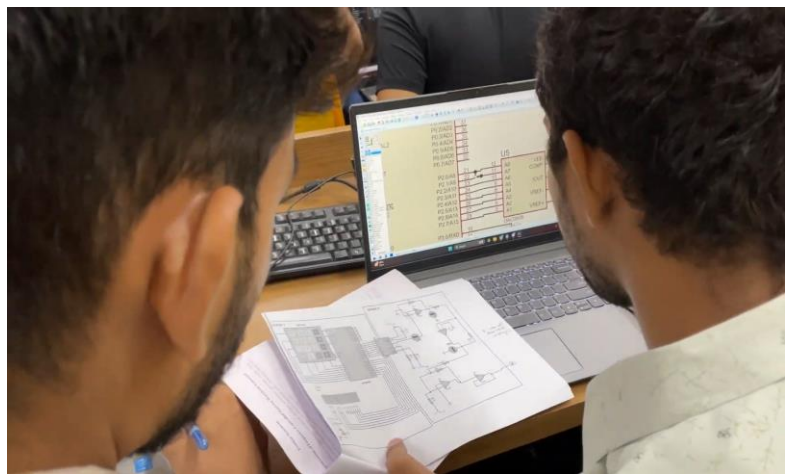
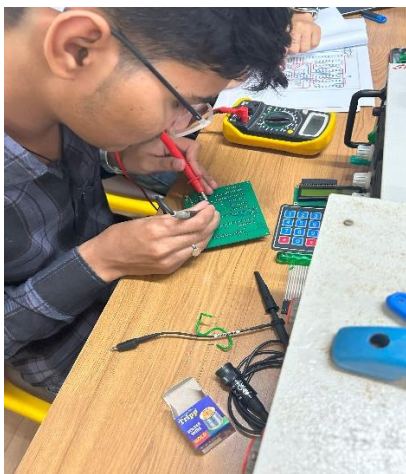
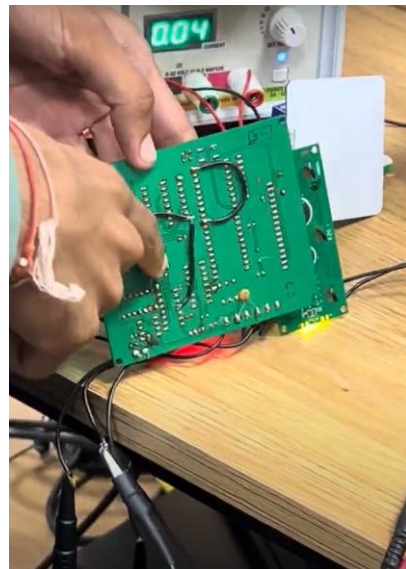
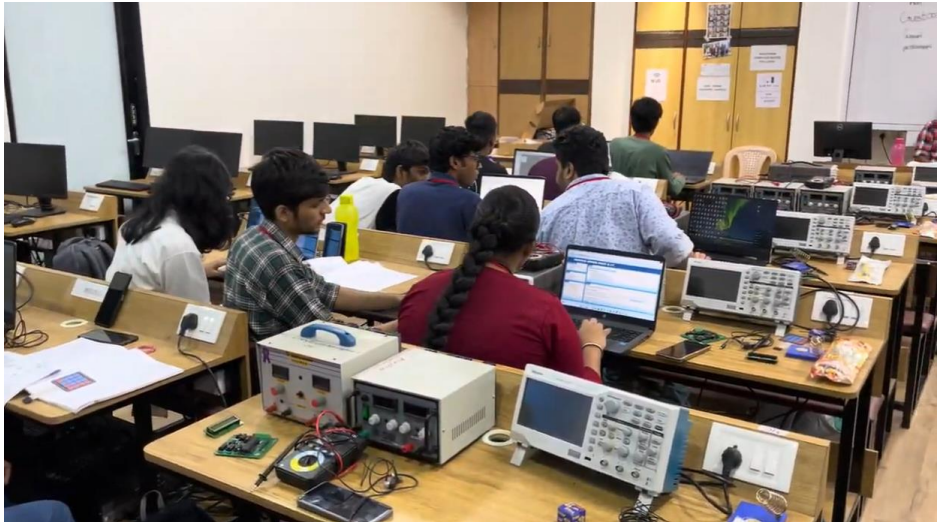
Sr. No.	Brief Idea	Timing	Description
1.	Inauguration	8:45 am to 9:00 am	The inauguration ceremony was a momentous occasion, brimming with anticipation and reverence. As Dr. Prashant Kasambe, Executive Core of I.E.T.E. Soham Ganatra, Woodrow Gonsalves and Prathamesh Mane and the participants lit the diya to honor Goddess Saraswati and invoke her blessings for wisdom, guidance, and success in the endeavors ahead.
2.	Briefing about the event	9:00 am to 9:45 am	The host Prathamesh Mane congratulated the participants for clearing 3 phases before being qualified for the final round. The mic was handed over to Dr. Prashant Kasambe to brief the participants about the schedule to be followed and other technical details. Breakfast was served to everyone after which the teams were allotted rooms and setups for the competition.

Sr. No.	Brief Idea	Timing	Description
1.	Phase 4.1- Debugging of code and simulation files	9:50 am to 1:30 pm	The participants were given the erroneous code files, to code the microcontroller, and simulation codes, which had faults in the display instructions and interchanged port connections, through mail. The expected results and pin layouts were provided to the teams as printouts. Proteus software was used to debug and simulate the results. The participants took great efforts to get the results within the given time. The teams were evaluated by Prof. Priya Deshpande who had joined us through Google Meet.
2.	Lunch Break	1:30 pm to 2:30 pm	The participants were served with complete lunch platter from the college mess and they continued the hardware round with renewed energy.
3.	Phase 4.2 - Debugging of faulty PCBs	2:30 pm to 5:30 pm	The participants referred to the block diagram, pin diagram and layout diagrams to understand the expected connections and get the desired results. Faults like open or shorted pins, missing wires and damaged ICs were deliberately introduced in the circuit. The teams vigorously worked to get the ramp signal as their final output on their DSOs.

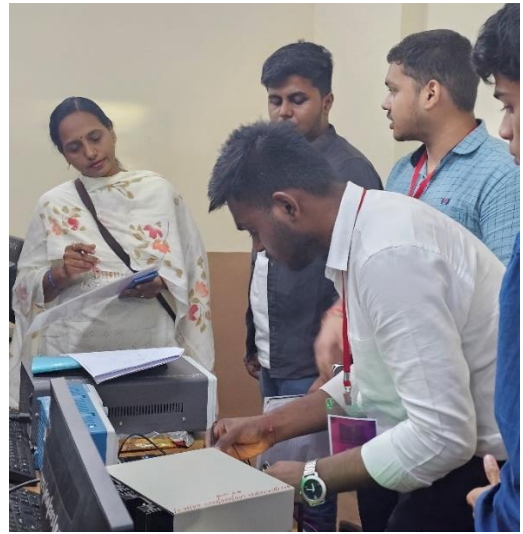
Sr. No.	Brief Idea	Timing	Description
1.	Evaluation Round	5:30 pm to 6:30 pm	Professor Reena Kumbhare questioned the teams and verified the obtained waveforms and graded them for their work. The process was a tough one as everyone had worked hard yet a handful got accurate results, some had got distorted waveforms and some teams could not get the required results. Participants waited in anticipation as Reena ma'am made graded the teams. Everyone was given snacks before the prize distribution ceremony.
2.	Prize Distribution	6:30 pm to 7:30 pm	The much-anticipated moment of the event, the result declaration, had finally arrived. With fingers crossed and hopes high, the host announced the third runners-up, followed by the second, the first, and finally, the winners of the competition. The teams were awarded grand checks for their respective prizes by the judges and professors. The day concluded with heartfelt thanks to the entire staff and team who had supported us throughout the event. Participants shared their invaluable experiences, inspiring us to organize and participate in more hardware hackathons. The teams departed with a sense of accomplishment and joy as the day came to a close.

BugBuster 2024 was successful in bringing out the qualities of persistence, patience and hard work among all participants. The need of being able to debug and troubleshoot a circuit was highlighted. Participants showed great enthusiasm and skillset during the entire course of the event. It brought learnings to everyone associated with the event.

Event Captured through our lens:



Glimpse of Evaluation Round



Glimpse of Winning Teams with Organizing Team and Judges



Rank 1: Electrovation, S.P.I.T., Mumbai.



Rank 2: Downcounters, S.P.I.T., Mumbai & Techtronics, D. J. Sanghavi CoE, Mumbai



Rank 3: Giga MindZ, S.P.I.T., Mumbai & Tech Titans, D. J. Sanghavi CoE, Mumbai



Consolation: Circuit Breakers, S.P.I.T., Mumbai & Vission Makers, Thadomal Shahani CoE, Mumbai

Conclusion

BugBuster 2024 proved to be an enriching and insightful experience for all participants. The event commenced with an auspicious inauguration ceremony led by Dr. Prashant Kasambe, setting a tone of reverence and anticipation. Participants were given a comprehensive briefing about the event schedule and the technical intricacies, followed by engaging sessions that spanned from detailed instructions to hands-on simulations and debugging exercises. Dr. Prashant Kasambe, alongside experts from Cybermotion Technologies and our star alumni, Mr. Chirag Shah, provided invaluable knowledge on various tools and techniques such as Proteus software, PCB schematic and layout, and Keil micro-vision. The rigorous phases included real-time troubleshooting of hardware issues using Proteus, a challenging simulation round, and an intense final quiz, all aimed at testing participants' theoretical and practical understanding.

The final day was marked by high levels of dedication as teams worked through the debugging of erroneous code files and faulty PCBs, evaluated meticulously by professors. The excitement culminated in a nerve-wracking evaluation and the much-anticipated prize distribution ceremony, where the hard work and innovative solutions of the participants were celebrated.

Student Feedback Summarized:

The event was highly praised by many students for its excellent concept, knowledgeable problem statements, and the unique learning experience it provided. Participants appreciated the helpfulness of the teachers and committee, the embedded hardware focus, and the competitive atmosphere that felt like a true hackathon. The event was described as well-executed, with great opportunities for interaction and learning. Many highlighted the fun and educational aspects, expressing eagerness for future events and commending the organizers for their efforts. Overall, the event was seen as a great experience that boosted knowledge and offered significant learning opportunities.

Objectives:

- 1) To provide a common platform for the students of electronics engineering department to exhibit, develop and amplify trouble shooting skills in the field of electronic circuits.
- 2) To appreciate the skills of students for findings and correcting faults in electronics circuits and systems.
- 3) To enhance the outreach of the Institute by technical collaboration.

Based on the positive feedback from the participants, we are pleased to announce that we have successfully achieved the objectives of our event. The event provided a common platform for students of the electronics engineering department to exhibit, develop, and amplify their troubleshooting skills in electronic circuits, as evidenced by the participants' appreciation of the challenging problem statements and the competitive atmosphere. Additionally, the skills of the students in finding and correcting faults in electronic circuits and systems were recognized throughout the event. Furthermore, the event significantly enhanced the outreach of our Institute through technical collaboration, as highlighted by the positive interactions and learning experiences shared by the students. Another important point to note is that the event could be managed in a better way and must be taken offline to increase the seriousness about such rare hardware events.

Acknowledgement's

We extend our heartfelt gratitude to Dr. Prashant Kasambe for his guidance and support throughout the event. Special thanks to the experts from Cybermotion Technologies and Mr. Chirag Shah for their enlightening sessions. We also thank Prof. Priya Deshpande and Dr. Reena Kumbhare for their critical evaluations. We are also thankful to Prof. Manish Parmar, Faculty In-charge S.P.I.T. IETE, Dr. K. T. Talele, Dean Student Affairs & Prof. Sujata Kulkarni, Faculty In-charge S.P.I.T. IEEE as well as Dr. Y. S. Rao, Dean Academics and S.P.I.T. Idea Lab Faculty In-charge for constantly encouraging us and providing support whenever required. We are particularly grateful to our esteemed Industry alumni who served as evaluators: Mr. Shahid Shaikh and Mr. Somesh Srivastava, Mr. Aniket Nadkarni, Mr. Apoorva Limaye, Mr. Prabhat Kumar, and Mr. Varun Mehta.

Additionally, the organizing team wish to sincerely thank Dr. B. N. Chaudhari, Head of the Institute for his vision to train the manpower in developing the skills of PCB Design which is in align with the Program Specific Outcomes of the Department of Electronics and Telecommunication to train manpower in this domain, and giving this unique opportunity to explore the intricacies of the field and gain valuable insights into the world of electronic manufacturing, here at S.P.I.T.

Finally, we thank the entire Organizing team for their tireless efforts in making BugBuster 2024 a grand success. We appreciate the Participants for their enthusiasm and dedication, which made the event truly memorable without which this event was not possible.

**Glimpse of the Participants, Organizing team with the Judges
and the Faculty Co-ordinator of the event**

