# A Report on

# Students Training Programme conducted under

# S.P.I.T. Students Empowerment Scheme

# (AY: 2023-2024)

## Silicon to System Journey

## Conducted by

**Industry Experts: IngotSEMI Technologies LLP., Bangalore**

**&**

**Experts from Academics**

**Duration:**

**23rd December 2023 to 28th December 2023**

**Coordinator. P. V. Kasambe, Assistant Professor**

**Convenor: Dr. Reena Kumbhare, HoD**

**Department of Electronics and Telecommunication**

**Parton: Dr. B. N. Chaudhari, Principal**

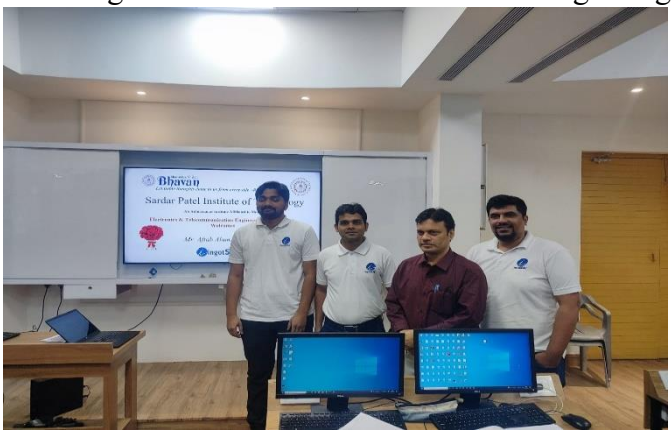
**Venue: VLSI/Embedded Systems Laboratory,**

**Room No. 301**

**DAY 1: Enthusiastic Start!!**

| SR. NO. | TOPIC | SPEAKER |
|---|---|---|
| 1 | History Of Semiconductor Development | Mr. Basant Saini |
| 2 | Basics Of Semiconductor Devices | Dr. Wasi Uddin |
| 3 | Diode Fabrication Process Flow and Electrical Characteristics | Dr. Wasi Uddin |
| 4 | Introduction to Device Modelling: Register and Diode Modelling | Mr. Basant Saini |

The inaugural day of the IngotSEMI Student Training at SPIT marked an enthusiastic beginning for us, a group of Second Year, and Third Year Electronics & Telecommunication Engineering students, eager to delve into a new field and explore a potential career path. Dr. Prashant Kasambe, Co-ordinator of this training programme welcomed the experts from IngotSEMI Technologies. The air buzzed with excitement and anticipation as the participants were warmly greeted and formally introduced to the IngotSEMI team by Director, Mr. Aftab Alam. Their detailed presentation elucidated the agenda for the 6-day workshop, setting the stage for an insightful journey that awaited us.




Left to Right: Mr. Keerthipati Thulasiram, Aftab Alam, Prof. Prashant Kasambe, Mr. Basant Saini

**Inauguration of the workshop**

**Day 1 - Lecture 1**

**History Of Semiconductor Development - Basant Saini**

The first session was an introductory session and instructor Basant Saini briefed us about the history of semiconductor development. The diodes and transistors we use today are a result of vigorous efforts of many scientists over the decades. The journey began when it was realized that relays, being mechanical switches, are slow and prone to wear and tear. Then evolved the vacuum diodes, triodes and vacuum tubes.

**Making of first transistor**

It is a common misconception that the first transistor was invented by William Shockley alone, the first transistor, the point contact transistor was invented by Bell Labs and was a work of three scientists John Bardeen, Walter Brattain and William Shockley. However, Sir William Schockley must receive the due credit for the invention of the junction transistor. The participants were told about the processes of Photolithography and the Moore's Law as well.

**Day 1 - Lecture 2**

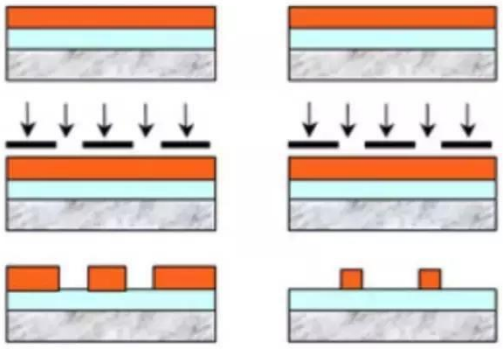
**Basics Of Semiconductor Devices - Wasi Uddin**

The next session was conducted by instructor Wasi Uddin. Our knowledge about the semiconductors was refined and key concepts such as Band Theory, Pauli's Exclusion Principle, Fermi Levels and their distribution on applying biasing were discussed. The ideality factor and input and output characteristics of the diode were revised as well. It was done in such a skilful and interactive manner that even the new learners could gras the concepts easily without much efforts.

**Day 1 - Lecture 3**

**Diode Fabrication Process Flow and Electrical Characteristics - Wasi Uddin**

In this session, following a lunch break, we were told about the manufacturing of the semiconductor wafers. Detailed discussion on making, grinding and slicing of ingot, rounding, polishing, etching and cleaning of the wafer was held. A thorough understanding of the process of depositing the photoresist, etching of oxide, doping, and deposition of metal was given.



Positive Photoresist Negative Photoresist

**Day 1 - Lecture 4**

**Introduction to Device Modelling: Register and Diode Modelling - Basant Saini**

The day was concluded with a session on device modelling. We were given insights on process of modelling and analyzing of models, simulation and verification. Various TCAD tools such as Silvaco and Synopsis were introduced. We gained in-depth knowledge on analytical modelling.

**DAY 2: Lessons Learnt and Opportunities Explored!**

| SR. NO. | TOPIC | SPEAKER |
|---|---|---|
| 1 | Basic of semiconductor devices (MOSCAP) | Dr. Ajay Agrawal |
| 2 | MOSCAP Fabrication Process flow and Electrical Characterization | Dr. Ajay Agrawal |
| 3 | Semiconductor modelling | Dr. Wasi Uddin |
| 4 | Semiconductor Ecosystem and Manufacturing | Dr. Wasi Uddin |
| 5 | Opportunities in Semi-conductor/VLSI Domain With Detailed QnA and doubt clearing session | Basant Saini |

After gaining enthralling insights into some of the industry processes on the first day, anticipation fueled our excitement for what awaited the student participants on the following day. The day kicked off with a captivating session on Basics of MOSCAPs that set the tone for another day of immersive learning and explorations into the intricacies of semiconductor technology.

**Day 2 - Lecture 1**

**Basic of semiconductor devices (MOSCAP) – Dr. Ajay Agrawal**

In the first session, conducted by Dr. Ajay Agrawal, students understood the need of MOS Capacitors in place of regular Capacitors and learnt the characteristics and operating modes of the MOSCAPs.

Accumulation Mode: In this mode, the majority carriers (electrons for n-type and holes for p-type) accumulate near the semiconductor-oxide interface when a positive voltage is applied to the gate. The electric field created enhances the carrier concentration, creating a conducting channel between the source and drain terminals. The energy bands bend upwards and no current flows regardless of the voltage applied. Surface potential is less than zero.

Depletion Mode: Depletion mode occurs when a negative voltage is applied to the gate, causing an electric field that repels majority carriers away from the semiconductor-oxide interface. This results in a depletion region near the surface, reducing the carrier concentration and leading to a decrease in conductivity. Unlike accumulation mode, a depletion-mode MOSCAP typically starts with a conducting channel and the gate voltage controls the depletion region. The energy bands bend downwards and thee surface potential is between zero and the difference between the fermi level and intrinsic fermi level.

Inversion Mode: In inversion mode, a sufficiently high positive voltage is applied to the gate, attracting free carriers of the opposite type to the semiconductor surface. This leads to the formation of an inverted layer or channel with carriers opposite to the majority carriers in the bulk semiconductor. For an n-type MOSCAP, holes are attracted, and for a p-type MOSCAP, electrons are attracted. This inversion layer allows current flow between the source and drain, representing the ON state of the device. The energy bands bend downwards and thee surface potential is between the difference between the fermi level and intrinsic fermi level and twice of that value for weak inversion and its twice of that value for strong inversion.

Students also learnt about C/Co vs Voltage graph.

**Day 2 - Lecture 2**

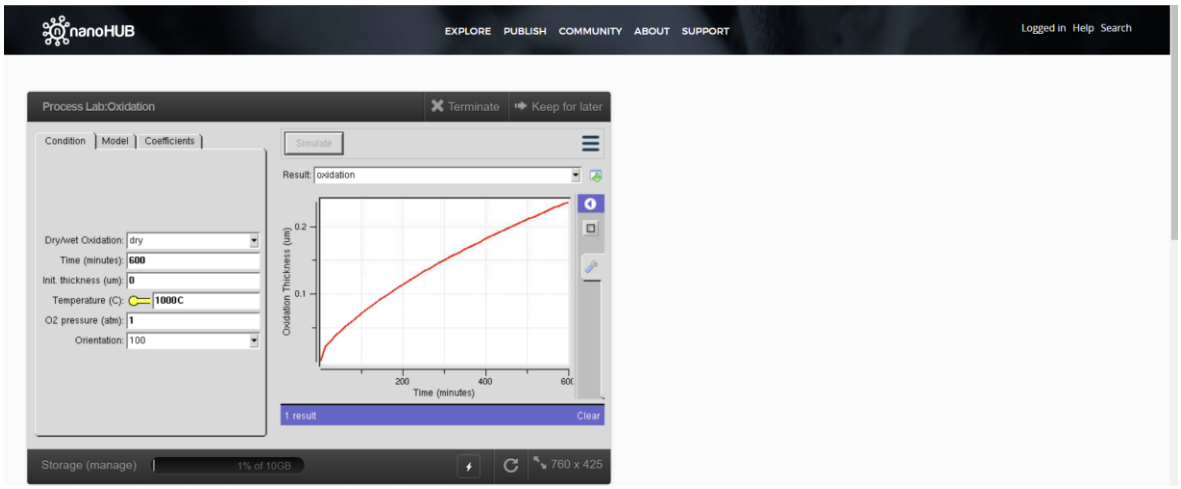
**MOSCAP Fabrication Process flow and Electrical Characterization – Dr. Ajay Agrawal**

In the following session, Dr. Ajay spoke about modelling a capacitor. Various parameters such as permittivity, area of plates and distance between the plates decide the capacitance of the capacitor. The permittivity of the medium is a property of the oxide layer and cannot be changed after deposition. The area of the plates is to be precisely maintained and hence processes such as masking and etching are to be followed instead of manual cutting. This is followed by electrical testing using a probe station.

## Day 2 - Lecture 3

### Semiconductor modelling – Dr. Wasi Uddin

The next session was held after lunch and Dr. Wasi Uddin explained the Basics of Semiconductor Devices (MOSFET) & Introduction to CMOS process flow (Semiconductor modelling). We primarily discussed the oxidation processes. Dr. Wasi taught how to use NanoHub, an online simulator, to simulate the oxidation processes and analyse them graphically.

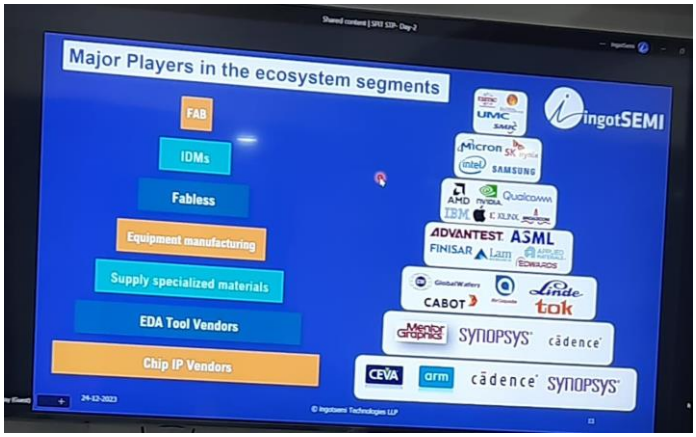



**Simulation on NanoHub**

## Day 2 - Lecture 4

### Semiconductor Ecosystem and Manufacturing – Mr. Basant Saini

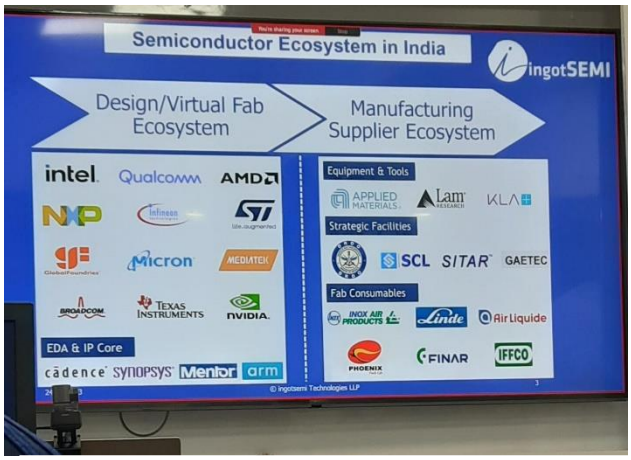
The next session was the one which grabbed everyone's interest. Instructor Mr. Basant Saini introduced us to Semiconductor Ecosystem and Manufacturing Industry. Every process and all the services that take an idea of a product from the parent company to the market were explained in detail. The roles offered by such companies and their potentials were discussed. We gained insights about IP Vendors like ARM and Synopsis, EDA Tool Vendors like Synopsis and Cadence and also about Supply Material Vendors, Equipment Manufacturers, Fabless and IDMs. The Fab processes were discussed in detailed.




Major Players in Semiconductor Industries

**Day 2 - Lecture 5**

**Opportunities in Semi-conductor/VLSI Domain – Mr. Basant Saini**



Opportunities in India

The next session on Opportunities in the Semiconductor Industry, conducted by Mr. Basant Saini, provided with a bird's eye view of the opportunities and roles that will be in demand in the semiconductor industry in the coming years, promising lucrative packages. The opportunities will be doubled over the decade. Leading companies in the semiconductor industries such as ST, Global Foundries, Synopsis, Applied Materials, LAM Research and AMD offer various roles in the manufacturing chain. New labs and training programs are being set up under "India Semiconductor Mission". Options for higher education and projects that will help secure these roles were suggested. Chip design roles, manufacturing roles and packaging and assembly roles were also elaborated upon. The session also delved into details about chip design roles, manufacturing roles, and packaging and assembly roles.

The day ended with fellow students asking endless doubts about the new career paths they had discovered and the instructors patiently guiding them.

**DAY 3: Introduction to FPGAs and using one for the first time!**

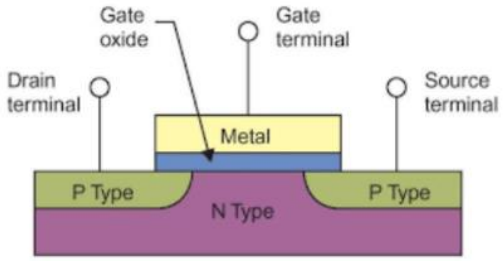
| SR. NO. | TOPIC | SPEAKER |
|---|---|---|
| 1 | Basics of Semiconductor Devices (MOSFET) | Dr. Wasi Uddin |
| 2 | Introduction to CMOS Process Flow (Semiconductor modelling) | Dr. Wasi Uddin |
| 3 | Introduction to FPGAs and its's components | Mr. Jeevan Urs |
| 4 | Architecture overview of Artix – 7 FPGA | Mr. Jeevan Urs |
| 5 | Hands-On session on Hardware Using Vivado | Mr. Jeevan Urs |

**Day 3 - Lecture 1**

**Basics of Semiconductor Devices (MOSFET) – Mr. Wasi Uddin**

As students were on a slight backlog due to the technical issues, students had faced on days 1 and 2, the morning of Christmas began with a deep dive into the world of MOSFETs, that rest at the heart of semiconductor technology. Dr. Wasi Uddin had delved into the heart of MOS technology the previous day, and he built upon it that morning with much aplomb -- explaining what it was that made MOSFETs so beautiful and versatile, and then elaborating on advancements over the years. The Bulk MOSFET, the workhouse of the semiconductor world, was deceptively simple a first glance.

At the heart, Dr. Wasi explained, lay the channel, a thin layer of heavily doped semiconductor. This channel is flanked by two regions of opposite doping. The gate, it turned out, acted as a magic switch. When a voltage is applied, it would create an electric field that either attracted or repelled charge carriers within the channel, effectively turning the MOSFET on or off.




The participants scribbled furiously, their minds grappling with the elegant interplay of physics and engineering that gave life to these microscopic marvels. Dr. Wasi pressed on, delving into the different operating regions of the Bulk MOSFET – linear, saturation, and cut-off. He explained how these regions dictated the device's behavior, allowing it to amplify weak signals, switch high currents, and form the building blocks of complex digital circuits.

He moved onto FinFETs, an improvement on the traditional MOSFET, that rendered gate length less relevant in the grand scheme of things and improved on the voltage gain of the planar MOSFET. The global switching standards, logic-based questions regarding such standards, and the concept of DIBL was covered in this session. Dr. Wasi's lecture was so crucial in unraveling the intricate tapestry of semiconductor technology that it left an indelible mark on students understanding. It laid the foundation for everything else we would learn. The concepts of doping, junctions, depletion regions, channel formation, and voltage thresholds underpinned all semiconductor devices. His lucid explanation of the physics behind MOSFET operation gave us an intuition for how switching, amplification, power control, and digital logic could be engineered starting from fundamental principles.

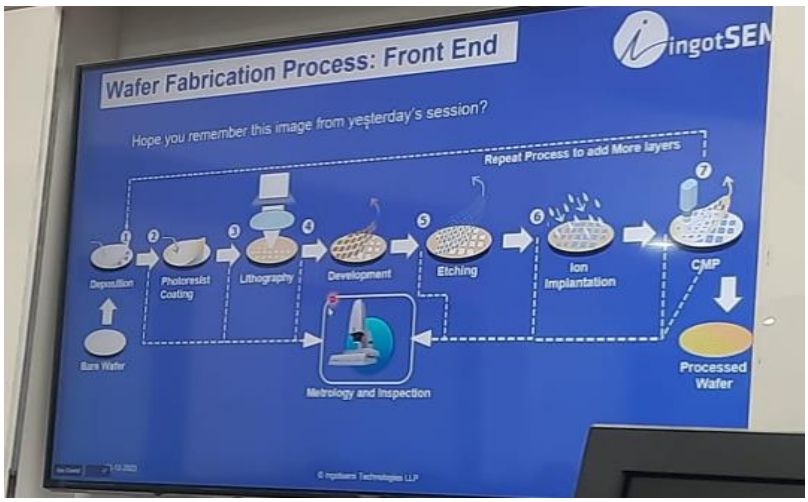
**Day 3 - Lecture 2**

**Introduction to CMOS Process Flow (Semiconductor modelling) – Dr. Wasi Uddin**

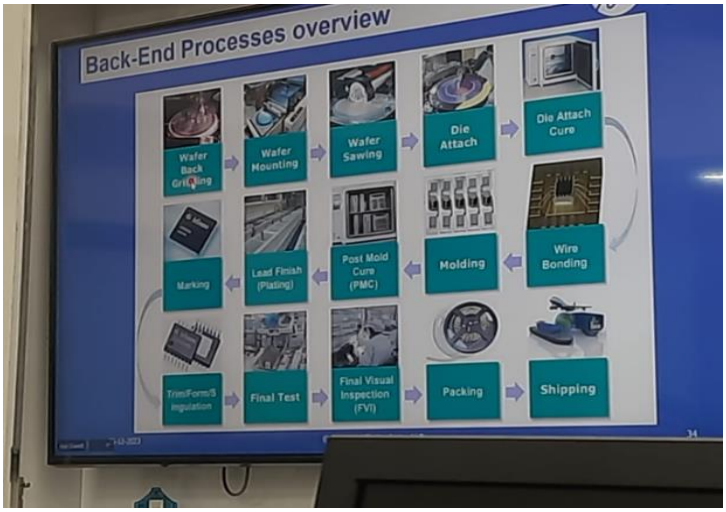
But if theory was fun, explanation of real-life fabrication was even more so. A lot of it was an elaboration on the previous day's lecture on Semiconductor Manufacturing in FabLabs, but all of us were spellbound regardless. A lot of the things described by Dr. Wasi seemed impossible, beyond the realm of mortal conception --- rooms so clean they set an operating theatre to shame, devices so perfect and exact that the slightest of errors meant tragedy. Above all, what seemed most inconceivable was perhaps the thought behind every step, the sheer amount of human resourcefulness and creative power it must have taken to conceive such marvels.

One of the students in reply said "I will admit I spent most of all Process related lectures in stunned disbelief." The meticulous intricacy of fabricating integrated circuits sounded more akin to performing magic than science. As Dr. Wasi described the dizzying array of ultra-specialized processes, my mind struggled to comprehend how humanity had devised such advanced techniques.

Oxidation, photolithography, etching, doping, CMP – each process by itself pushed the absolute limits of physics and engineering. And yet they had all been woven together into a precisely choreographed manufacturing process that reliably yielded billions of transistors on slivers of silicon. As image after mind-boggling image flashed by of fab plants that spanned football fields, robotic arms spinning wafers with uncanny precision, and containers of toxic chemicals being handled with nonchalant ease, students could only sit wide-eyed in rapt attention. The fact that such an unfathomably complex manufacturing pipeline had been constructed just to satisfy humanity's quest for faster, smaller, denser computing seemed nothing short of miraculous to all the participants.




In the span of an hour, learners had gained immense respect for an entire ecosystem of brilliance that students had previously been oblivious too. The very screens and processors students took for granted represent the life's work of generations of geniuses. As students parted for lunch, they knew they would never look at my phone or laptop the same way again. Microscopic transistors were taking on an aura of magic for me now – the promise of progress incarnate.



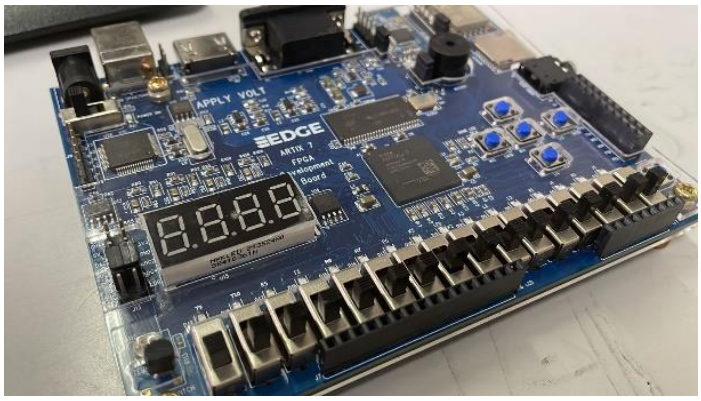

**Day 3 - Lecture 3**

**Introduction to FPGAs and its's components – Mr. Jeevan Urs**

One of the learners expressed "I will be the first to admit to knowing absolutely nothing about FPGAs when I walked into the lecture hall that afternoon after a delicious, Christmas-worthy lunch. Sure, I'd done my research -- FPGA stood for Field Programmable Gate Arrays, words that apart, made perfect sense, but together, seemed like something I couldn't begin to process."

Mr. Jeevan was gentle with his introduction -- he began with its history. A few of the students had spent a few hours the previous day trying to download _Vivado_ on our devices. _Vivado_ belonged to _Xilinx._ These were things we knew. He built on that, and explained that in 1984, after some fundraising, Ross Freeman, Bernard Vonderschmitt, and James V. Barnett II founded

Xilinx. Freeman speculated that transistors would experience a fall in price and eventually invented the FPGA.




The original FPGA was 74 series of Chips using only NAND and some people would design their own chips based on Gate Arrays (*array of NAND Gates*) The first programmable chips were PLAs (Programmable Logic Arrays) They were two level structures of AND and OR gates with user programmable connections. PAL (Programmable Array Logic) came after, and had a programmable AND array followed by a fixed OR array.

Eventually, this evolved into FPGAs which had a more flexible architecture consisting of configurable logic blocks (CLBs), I/O blocks, and programmable interconnects that let signals route between logic blocks. Unlike their predecessors, FPGAs were made up of logic cells that could be configured to perform complex functions beyond just AND/OR logic.

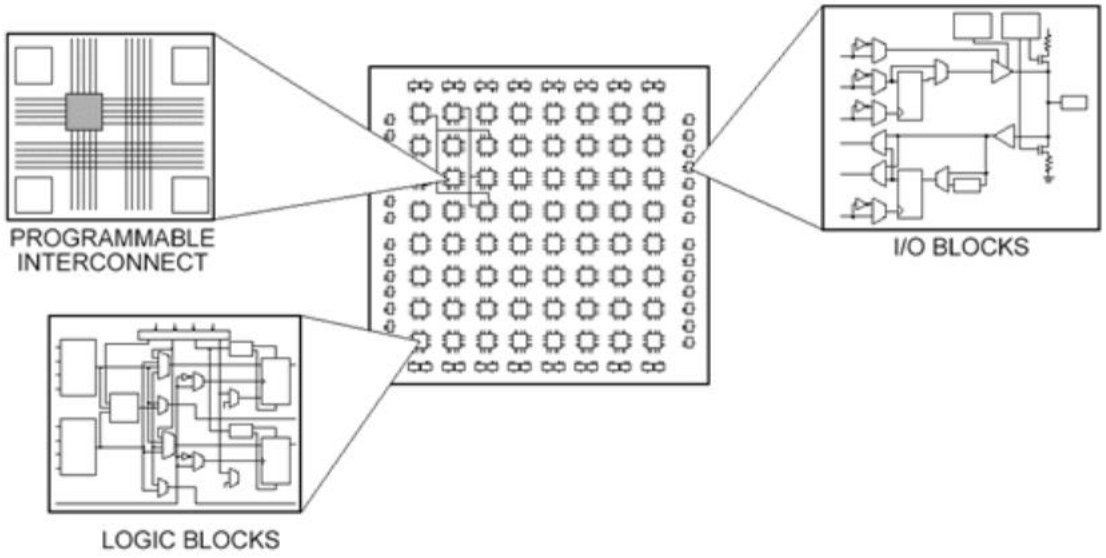
The first commercial FPGA was the XC2064 which came out in 1985 from Xilinx, offering just 64 configurable logic blocks. But the flexibility and potential were clear, and rapid innovation followed over the next decades. FPGA density and capabilities skyrocketed manifolds as fabrication processes enabled cramming in more transistors per chip. Soon millions of system gates were possible, with embedded RAM, DSP blocks, CPU cores and more.

Mr. Jeevan then elaborated on FPGA architectures and showed how logic, routing and I/O blocks could be programmed using HDL languages like Verilog and VHDL. Students realised that with FPGAs, they had the ultimate playground - a silicon canvas to imagine and create any digital circuit we desired! FPGAs could be used to make the blueprint for circuits that could be implemented via ASIC --- which was far more suited to mass production.

**Day 3 - Lecture 4**

**Architecture overview of Artix – 7 FPGA – Mr. Jeevan Urs**

In response to Mr. Jeevan's delivery about FPGA, one of the students admitted "I tried my best to keep up as Mr. Jeevan rapidly introduced us to the world of Field Programmable Gate Arrays. He started by breaking down the logic blocks that serve as the building blocks of FPGAs - the lookup tables (LUTs), flip flops, multiplexers and carry logic. Using examples, he showed how LUTs can implement basic logic functions by storing truth table outputs in memory cells. I frantically noted down points as he covered LUT types, FPGA interconnect architectures, and the Configurable Logic Blocks (CLBs) made up of grouped LUT slices."




When he touched upon the different Xilinx FPGA varieties like Artix 7 and Virtex 7, their intended applications and the resources they offered, students could faintly begin to envision the flexibility these chips offered. His brief overview of the RTL design flow - from HDL to synthesis, placement, routing and finally FPGA programming - provided the basic framework for what students were about to do hands-on.

When things got too heavy, Mr. Tulsi come in, with interesting, common-world analogies to simplify complex concepts! As someone with barely any hardware or EDA background, most of the terminology had sounded unfamiliar. But the sheer enthusiasm and energy with which Mr. Jeevan and Mr. Tulsi explained such esoteric concepts in simple terms was infectious. Students might only have grasped the tip of the iceberg, but for the first time, FPGAs now seemed approachable and packed with endless creative potential instead of something daunting and impossible to understand.

Students took a short break to catch our breath and grab some snacks before the Vivado session. Their mindswas abuzz thinking of what we might design and implement on the FPGA boards ourselves within the next couple weeks! The students had been given just a tiny peek, but the world of hardware design already seemed marvelous.

**Day 3 - Lecture 5**

**Hands-On session on Hardware Using Vivado – Mr. Jeevan Urs**

Then came the crowning jewel of the day, the most awaited part --- actually working with FPGAs and Vivado!

One of the group was given the ARTIX A7 FPGA to work with. Mr. Jeevan patiently explained the workflow on his own device. This team was able to follow without facing too many issues, but all the teachers including Dr. Prashant Kasambe went around the class helping out students where there needed it. From the basic writing of the program right down to the generation of the bitstream, we had help and handy explanations every step of the way.

The joy all students felt when the output of the LEDs matched the truth table is difficult to put in words. After hours of struggling through the intricacies of Vivado, watching our basic logic function light up the development board with the correct result felt like sweet vindication.

The process had seemed so complicated - crafting Verilog code, running endless syntheses and implementations, ironing out errors and timing constraints. Yet suddenly, all that effort crystallized physically before our eyes. The satisfaction was sublime.

The day ended on an even brighter note. It was both Chrismas and Class Representative's birthday, and so it was decided to have a treat with cake and some snacks. We sang him a happy birthday song with great vigour, and left the college premises when the sky was dark, our minds full, and our hearts fuller.

**DAY4: Introduction to Vitis HLS**

| SR. NO. | TOPIC | SPEAKER |
|---|---|---|
| 1 | Introduction to Vitis HLS, Validation and Verification | Mr. Jeevan Urs |
| 2 | Embedded System Design Flow on ZYNQ | Mr. Jeevan Urs |

On Day 4 students were mainly guided by Mr. Jeevan. He has experience in handling Vivado, Vitis HLS and many such allied software. This day consisted of briefly two sessions, an introduction to FPGA's, IP's, ASIC and a hands-on workshop. Mr. Jeevan helped in setting up all the PC's with the required applications. Mr. Jeevan also provided the necessary codes required to run an example on the application.

A day before this, Jeevan sir was very helpful and kind in sharing and downloading the software along with its license on the computers of the microprocessor lab of S.P.I.T.

**Day 4 - Lecture 1**

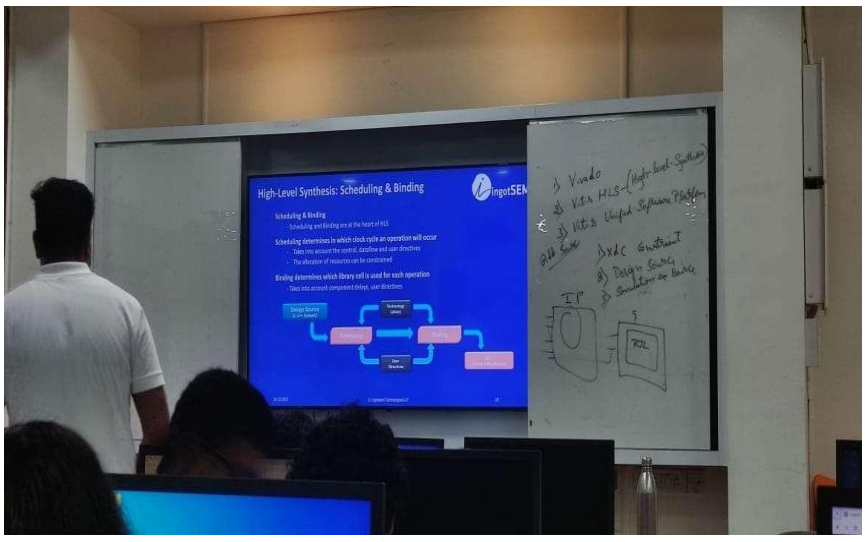
**Introduction to Vitis HLS, Validation and Verification– Jeevan Urs**

The first session of day 4 consisted of a small introduction to various topics related to the software's use. The students had to understand what the applications can accomplish to finally accomplish the given taskon the software. The students were taught about IP, what is stored in it, how and where it is used, how do companies and people use it to make money. The students learnt about LUT's (Look up tables) and black boxes. Steps that areinvolved in the Vitis HLS Design were also told. The main steps include:

1) Write a C++ code.
2) Debug the code.
3) RTL Conversion.
4) Creation of an IP.

Students were told that this is for low level design and for high level design we would require Vitis HLSsoftware, where HLS stands for High Level Synthesis.

In C simulation, we write the C code to be performed. The students performed the C synthesis where one can schedule steps, optimize available resources and finally convert to RTL. The C synthesis code is then converted to VHDL/Verilog. If the RTL simulation output and the output of the C code is the same then the RTL is packed inside the IP and a black box is created in the end. The black box is created sothat no one can copy the RTL logic inside it. To use the IP (Intellectual Property), we will have to pay the owner of the IP. We also learnt how to write Verilog/VHDL codes in a way. The session ended with a small talk on Scheduling and Binding.




**Day 4 - Lecture 2**

**Embedded System Design Flow on ZYNQ – Mr. Jeevan Urs**

After everyone returned from lunch break, we sat in the coldness of 301, as Jeevan sir explained about how to begin with Vitis HLS. Mr. Jeevan gave a brief introduction to the FPGA (Field Programmable Gate Array) boards available (like Nexys A7-100T, Pynq Z2, Edge)

Students first wrote a code for matrix multiplication in C language. The students successfully completed the steps instructed by Mr. Jeevan and made sure that every step was performed successfully using the flow navigator. The steps to perform the IP creation are as mentioned above. Students had to be careful inlistening to the Mr. Jeevan as missing one step would cause an effect in completion of the step but would result in no IP creation.

Participants were told about the two types of modelling namely gate level modelling and behavioural modelling. Additionally, students also had to pick up resources from the internet like the constraints andthe XDC master file. Participants coded the FPGA's to work as an AND Gate, OR Gate, and used it to turn ondifferent colour LED's. The participants learnt to connect


the FPGA with the Computer/Laptop and write codes along with generating the Bitstream. Below is a photo of the hand-on session.

**Day 5 : All About PYNQ!!**

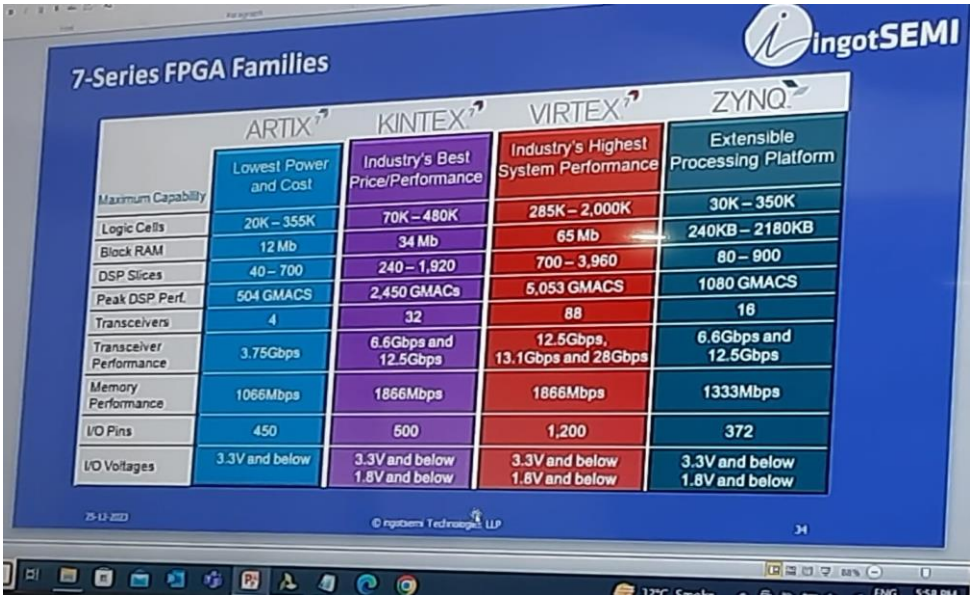
| SR. NO. | TOPIC | SPEAKER |
|---|---|---|
| 1 | Python Productivity using PYNQ-72 and PYNQ Framework | Mr. Jeevan Urs |
| 2 | Demonstration on ML Based Application using PYNQ and Hands-On session on Hardware | Jeevan Urs |

**Day 5 - Lecture 1**

**Python Productivity using PYNQ-72 and PYNQ Framework – Jeevan Urs**

The Fifth day of the VLSI course had a theory session in the Morning followed by LAB practice on FPGAs. In the beginning, the session on FPGAs was addressed by Mr. Jeevan in presence and guidance of Prof. P.V.Kasambe and ingotSEMI Team in which he briefed about FPGA structure and the background of the entire process from programming the FPGA to its detailed working and also about the 7 series FPGA families.This session was quite interactive and students gained a deep understanding about the working of the boards and their applications. Mr. Jeevan had an

immense variety of techniques to communicate and interact with students and clarify all doubts and queries arising in our minds.



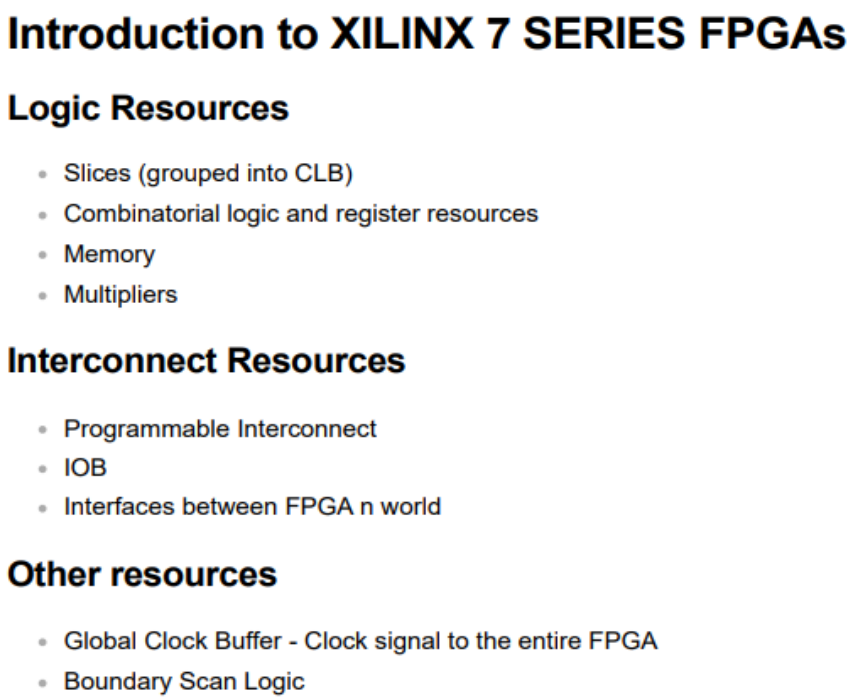

**Day 5 - Lecture 2**

**Demonstration on ML Based Application using PYNQ and Hands-On session on Hardware – Mr. Jeevan Urs**

After the session, In the next Lab session , students were assembled in the lab dividing them all in the group of 4 students .This lab session was taken by Prof.Jeevan with the presence and guidance of Prof. P.V.Kasambe and ingotSEMI team . All students were now given an exact hands-on experience on programming the FPGA boards like Artix-7,ZYBO,PYNQ etc with a code on jupiter platform.This gave students a real advantage of experiencing and understanding the working of FPGAs and their diversity. During this lab session, Students were given The PYNQ board and the board was connected to the PC with the USB connection and also the LAN was connected which is available on the board. After waiting for 3 mins the yellow led's turned on indicating the completion of connection. After that we set the IP address by going to the Network properties of IP4 in the Control panel of the P.C we edit the IP address. Now moving to Chrome, we open Jupiter and put the IP address. Then we put the password.

After entering the JUPITER platform, we open the file as mentioned by Prof.Jeevan. The located file contains a code of controlling of LED with the help of buttons of the board. In the experiment we had a button to Turn on and change the LED colour to RED, BLUE, GREEN. We also had a button to continuously change these led colours in series, students had a button to turn of the functioning of the code. When we write that code on The JUPITER software, we run the code by the run directory available on the top of the control panel. Prof. Jeevan also told students the versatility of the platform since it allows us to write multiple blocks of the code and Run only the block which we want.This was Enhancing the functionality of the platform .

Here during this lab session students got the entire experience of working on FPGA boards and programming them with the help of jupiter. On the Privious days they did this using vivado and vitis HLS in verilog language. Hence concluding that Day 5 was a deep learning and practicing process for all.




**DAY6: Verification in VLSI – Prof. Surendra Rathod, Principal, Fr. Rodrigues College of Engineering, Bandra**

| SR. NO. | TOPIC | SPEAKER |
|---|---|---|
| 1 | Verification in VLSI | Prof. Surendra Singh Rathod |

The participants had the privilege of hosting Prof. Surendra Singh Rathod, a distinguished academician with a Ph.D. from IIT Roorkee, for a guest lecture on day 6. Currently the Principal at Fr. Conceicao Rodrigues College of Engineering, Prof. Rathod has over 25 years of rich experience spanning across teaching, research and leadership roles in academia.

He has an outstanding research record that includes 40+ papers in international journals, 60+ papers in conferences, guiding 3 doctoral students to completion and 8 published patents. A recipient of prestigious honors like the ISTE Best Teacher Award (Maharashtra) and the CSI Distinguished Professor Award, he has also successfully obtained competitive research grants worth over Rs. 28 lakhs.

It was undoubtedly an honor for our institution to host such an accomplished expert and researcher. His lecture and interactions with our students proved to be extremely inspiring. The organizing team is grateful that Prof. Rathod Sir took the time to visit our college and share his invaluable insights with our budding engineers. His words of wisdom will surely motivate young minds at our institute to aim for excellence in engineering education and research.

**Day 6 - Lecture 1**

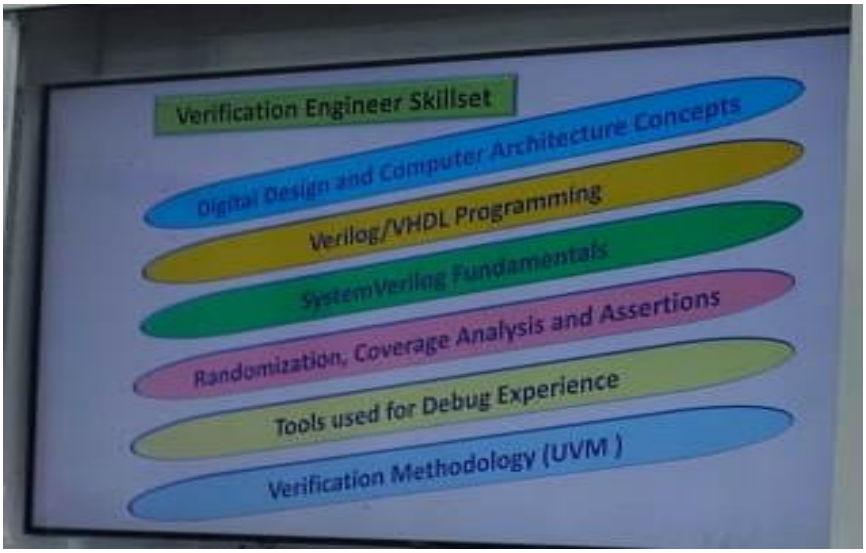
**Verification In VLSI – Prof. Surendra Rathod, Principal, Fr. Rodrigues College of Engineering, Bandra**

The topic of the guest lecture was about 'Verification in VLSI'. In his lecture, sir first explained the concept of SoC (System on Chip) which is an integrated circuit that integrates most or all components of a computer or electronic system onto a single chip.

He also showed us different advertisements of a mobile brand 'Lava' to showcase that before launching any product in the market, a company has to test it millions of times to ensure excellent quality and reliability, which was highlighted in the ads to build customer trust.

After that, he elaborated on the significant demand for verification engineers in the industry. He mentioned that 70% of engineers are recruited for verification roles and the remaining 30% are for design roles.

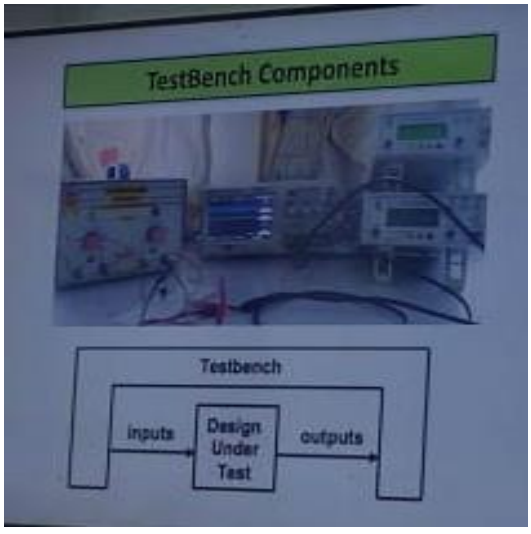
Then he explained the key skill sets required to become a proficient verification engineer, as shown in the image. The lecture was very informative in shedding light on the critical but often less understood area of verification and the promising career opportunities it presents for VLSI engineers. Dr. Rathod insights into the nuances of verification were valuable for all our students.

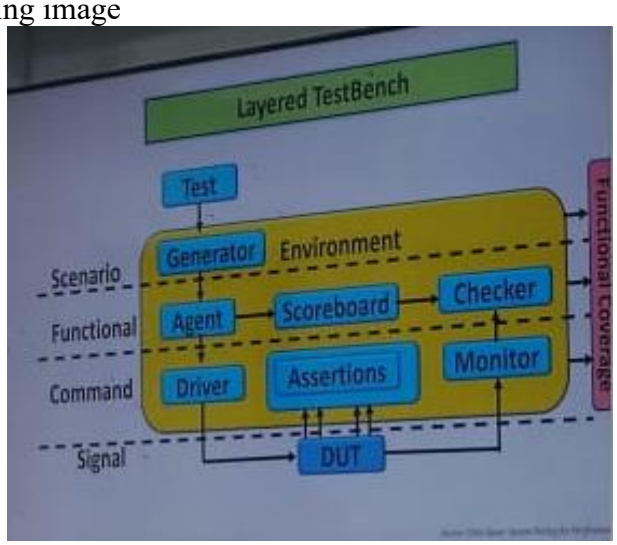



Through his discussion, then Dr. Rathod elucidated the differences between testing and verification. Verification ensures that the intended functionality of a part or product works as expected with respect to a “golden” reference dataset of outputs. Manufacturers perform verification prior to fabrication to reduce costs by catching errors early. Conversely, testing involves evaluating a fabricated product from an end-user perspective, typically through prototypes. He then illustrated the verification process via a block diagram.

Next, he covered the concept of a DUT (Design Under Test) - the phase when product design is still actively progressing before implementation manufacturing. This includes conceptualizing, planning and refining various design elements. To verify DUT functionality, test benches serve as simulation environments. To help us visualize test benches, he drew an analogy with the experimental setups used to test circuits in an electronics laboratory. The images below showcase such a setup versus a typical test bench block diagram.

Through easy practical examples, Prof. Rathod provided invaluable perspectives into intricate verification methodologies. The lecture enabled students to grasp complex VLSI verification principles. After explanation of simple test bench sir explained layered test bench, the block diagram of layered test bench is shown in following image

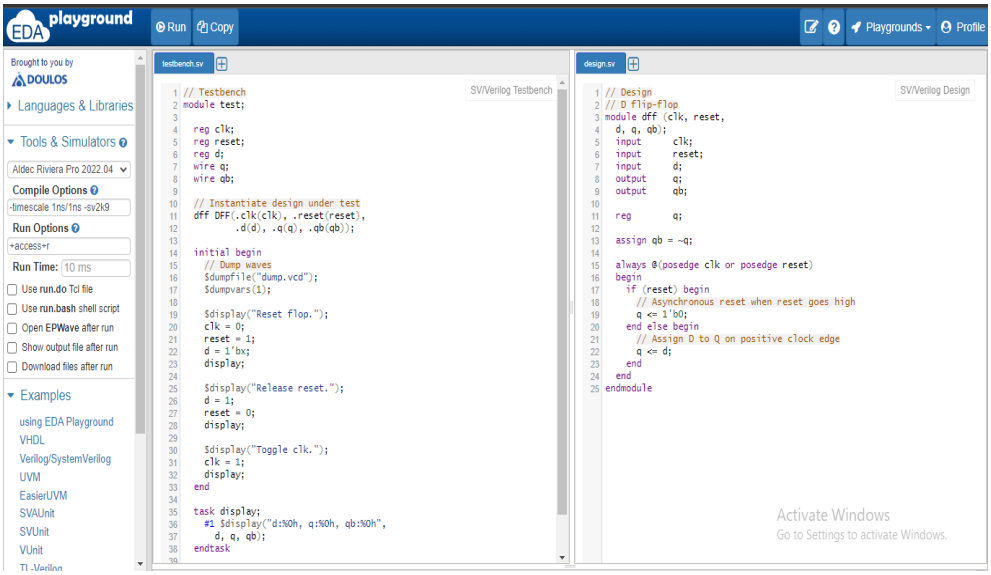


In the following block diagram Scoreboard Block contains expected model, Assertions Block gives the warning/errors in testing of DUT. The fuctional coverage checks if all intended functions are executed. In short testbench initiates the variables i.e. basically it connects all the components of DUT

Dr. Rathod then introduced us to EDA (Electronic Design Automation) Playground, a free online tool. EDA Playground provides a web-based environment for learning, testing, and sharing electronic designs and simulations. It is a virtual space where engineers and students can experiment with hardware description languages (HDLs) like VHDL and Verilog to run simulations without needing to install complex EDA tools locally. EDA Playground serves as a valuable platform for the electronic design community by offering a user-friendly and accessible web interface for coding, simulating and sharing digital designs. It also contains a variety of code examples for different HDL languages including VHDL, Verilog, Python, C++ etc. We first explored a sample Verilog program of a D Flip-Flop circuit from the examples section to gain hands-on experience with the tool. In summary, EDA Playground is an excellent gateway for students to get started with HDL programming and circuit simulations through the convenience of a web browser. He provided a great overview of leveraging this platform for our VLSI design and verification learnings.

All the participants also observed the output in form of Waveform by just enabling the 'Open **EPWave** after run' option, in following image the output of D flip-flop is shown. In similar manner sir shared 2 more project just by sharing link of the project on Whatsapp. EDA playground is very useful online tool for small projects and it's free unlike vitis and vivado software.




Dr. Rathod then explained the two types of assignment operators in Verilog:

1. Blocking: Here, the RHS is evaluated first and then the value is assigned to the LHS. Sequence matters in blocking assignments.
2. Non-Blocking: Unlike blocking, all statements are executed in parallel. The RHS is evaluated first but the values get assigned to LHS only after the always block ends. Sequence does not matter in non-blocking assignments.

He also gave a brief introduction to inter-processor communication and the evolution of System Verilog. He highlighted that Verilog has integrated features of high-level programming languages like object-oriented programming in its recent updates. Regarding soft-core processors, he asked us to further explore the VEGA processor developed by IIT Madras.

In summary, the lecture provided critical perspectives on key aspects of Hardware Description Languages like blocking vs non-blocking assignments. Sir also gave us an overview of emerging concepts like System Verilog and soft processors. His guidance on relevant areas for us to explore more will surely aid our VLSI learning journey.

**CONCLUSION**: The SPIT Student Training Program organized by Department of Electronics and Telecommunication and conducted by ingotSEMI Technologies LLP, under the mentorship of Mr. Aftab Khan, Director ingotSEMI and Team, covered a wide array of topics, with each day building upon the previous to provide students with a good understanding of semiconductor devices and designing. The initial sessions delved into the history of semiconductor development and introduced diode devices, their fabrication, characterization, and modeling. This basic knowledge set the stage for the subsequent exploration of MOS capacitors and MOSFET devices on the second day. As the program progressed, students transitioned into programmable logic devices, specifically FPGAs, during the third day. Hands-on sessions with the Artix-7 FPGA allowed for practical application of the learned concepts. Next, we extended this knowledge by introducing additional design tools, including Vitis HLS for high-level synthesis, further enhancing students' skills in FPGA-based design. The program's fifth day focused on tying together these concepts through the embedded system design flow on the Zynq platform. Students also gained insights into deploying machine learning applications using the Pynq framework. The program's final day saw Dr. Surendra Rathod as the guest speaker, who guided the students about career prospects in system verification industries, as well as provide a hands-on experience in Verilog code using simulation software. Overall, the program provided students with a holistic understanding of the VLSI industry, equipping them with valuable knowledge for their future endeavors.

The co-ordinator of the Training Programme Dr. Prashant Kasambe would like to extent the sincere thanks to the industry expert team of ingotSEMI Technologies, expert from academics, Dr. S. S. Rathod for sharing their valuable insights into the VLSI domain. It was possible due to the efforts of Technical Staff of Electronics and Telecommunication Department namely Mrs. Deepali Thombare, Mrs. Sujata Gavas and Mrs. Aditi Adhav who helped in setting up the Laboratory resources by installing Vivado Software under the technical assistantship of CoreEL Technologies Pvt. Ltd., Banglore. The co-ordinator would like to extend the sincere thanks to IT team of S.P.I.T. namely Prof. D. D. Ambavade, and Mrs. Karuna Bhikru who assured complete internet connectivity to almost 100 PCs at Room No. 003 and 301 in spite of the fact that it was a vacation time for them. Sincere thanks to Mr. Hemant Murkutkar for arranging the manpower for major civil work at Room No. 301 on urgent request. The co-ordinator of the Training Programme wish to thank a team of students Mr.Keshav Jha, Ms. Saloni Zargad, Mr. Woodrow G, Mr. Shashvat Sangale, Mr. Prathamesh Mane, Ms. Tanvi Wani, Ms. Aditi Rao, Mr. Aditya Nagane for their timely help. Sincere thanks to Dr. Reena Sonkusare, HoD, Electronics and Telecommunication for the entire support during the smooth execution of the programme.

Finally, the organizing team wish to sincerely thank Dr. B. N. Chaudhari, Head of the Institute for his vision to train the manpower in VLSI domain which is in align with the country's Semiconductor Mission to train manpower in this domain, and giving this unique opportunity to explore the intricacies of the field and gain valuable insights into the world of semiconductor manufacturing, here at S.P.I.T.

The objectives of the training programme were:

1. To have an industry training to students under student's empowerment scheme of S.P.I.T.
2. To effectively utilize the resources developed in the VLSI Laboratory under the AICTE MODROB Scheme
3. To train students in the domain of their interest and carrier path.

So, looking at the feedback of the students, it is observed that the training programme was successful to meet all the objectives and the Department of Electronics and Telecommunication would witness fruitful outcomes of such activities. However, this path is little long and students and faculty need more dedication and such advanced training.