ELECTRICAL ENGINEERING DEPARTMENT
COLORADO SCHOOL OF MINES

EENG 385 - Electronic Devices and Circuits
BJT Curve Tracer: Deboo Integrator
Lab Document

Outcome and Objectives

The outcome of this lab is to analyze, simulate and assemble a circuit that generates a staircase waveform using an integrator circuit and compare the expected behavior of the circuit from each mode of analysis. Through this process you will achieve the following learning objectives:

- Use a software tool to perform time and frequency domain analysis of an electronic circuit.
- Analyze and design a circuit containing resistors and op amps.
- Analyze and design a circuit consisting of several building blocks.
- Assemble a circuit on a PCB using the equipment in the laboratory.
- Use laboratory test and measurement equipment to analyze electronic circuits.

System Architecture

In this third lab of the BJT Curve Tracer, shown in Figure 1, you will explore the Deboo Integrator, a circuit that takes the integral of its input.

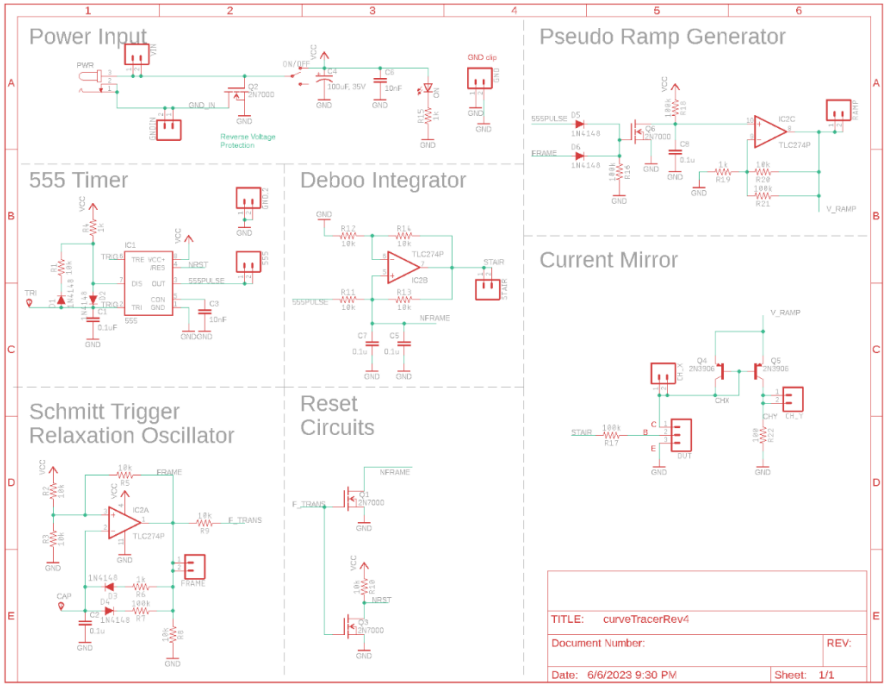


Figure 1: The complete BJT curve tracer. Note we will only populate 1 of the C5 or C7 0.1uF capacitors in our circuit. The other capacitor position is in case the Deboo Integrator needs trimmed.

Look carefully at the schematic and locate the Deboo Integrator subsystem. Notice the two signals "555PULSE" and "NFRAME" in this subsystem originate in the 555 Timer and the Schmitt Trigger Relaxation Oscillator (via Reset Circuits) subsystems. In order to understand the behavior of the Deboo Integrator, you should review the behavior of these two subsystems. Do this by retrieving the simulation information you found in the previous two labs and put the information into Table 1. We will come back to this table through the course of the lab.

Table 1: The output of the 555 Timer and Schmitt Trigger Oscillator simulations from the prior two labs.

Quantity	555 Timer Simulation	Schmitt Trigger Relax Osc Simulation
Time high (µs)		
Time low (µs)		
Period (µs)		8091 us
Frequency (kHz)		
Duty Cycle	8.7%	

Analysis: Deboo Integrator

The construction of a working BJT curve tracer requires we create a staircase-shaped voltage waveform. A staircase waveform looks like, you guess it, a staircase when viewed from the side – you will see it later in the lab. The circuit to do this is a Howland Current Source with a capacitive load, called a Deboo Integrator. The Deboo Integrator to be built is shown in Figure 2. Note, in this circuit all the resistors have the same value, denoted as *R*.

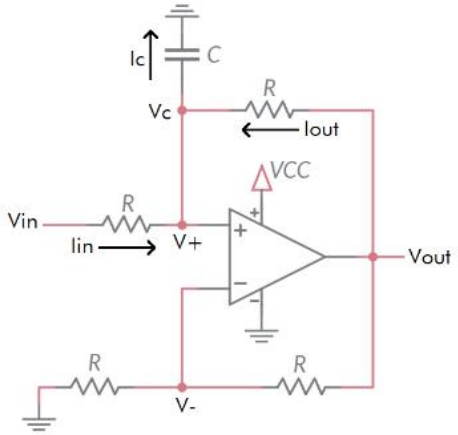


Figure 2: A Deboo Integrator integrates the input voltage over time.

To understand how the Deboo Integrator computes the integral of the input voltage, let's walk through the following analysis together.

1. Write an equation relating *V-* and V_{out}. Solve in terms of V_{out}. *(Hint: Voltage divider.)*
2. Write an equation for Iout in terms of V+, V_{out} and *R*. *(Hint: Use Ohm's law.)*
3. Replace the V_{out} term in the Step 2 equation with the value for V_{out} found in the Step 1 equation.
4. Since the circuit has (circle one) positive/negative feedback the inverting and non-inverting inputs of the op amp are the same. Let's call this common voltage V_c. So, $V- = V+ = V_c$.
5. Replace *V+* and *V-* in the Step 3 equation with V_c and simplify.

6. Write an equation for I_{in} in terms of V_{in}, V_c, and R. *(Hint: Ohm's law.)*
7. Write a KCL equation for the *V+* node.
8. Replace the I_{out} and I_{in} terms in the Step 7 equation with the value for I_{out} / I_{in} found in the Steps 5/6 equation. Simplify. *(Hint: The simplified equation has three terms.)*
9. Write the equation for the current (called I_c) in a capacitor in terms of the voltage (called V_c) and capacitance.
10. Replace the I_c term in the Step 9 equation with the value for I_c found in the Step 8 equation.
11. Replace the V_c term in the Step 10 equation with the value of V_c found in the Step 1 equation (remember that V- equals V_c).
12. Multiply both side of the Step 10 equation by *dt/C* and then integrate both sides.

This is pretty cool; we have a circuit computing the integral of the input voltage, multiplied by *2/RC*, and placed the result on its output. Let's now look at how this capability is used to create a staircase voltage.

Analysis: Deboo Integrator in BJT Curve Tracer

The Deboo Integrator in the BJT Curve Tracer in Figure 1 gets its input from the 555 Timer output pulses (555PULSE in Figure 1). The next set of questions seeks to understand how the Deboo Integrator output will look like when it receives these pulses.

1. Using the values of resistance and capacitance in Figure 1, compute the weighting factor *2/RC* for the Deboo Integrator output. Note, I created the PCB with a parallel combination of 0.1uF capacitors C5 and C7. I did this when I designed the PCB in case the capacitance value needed to be increased above 0.1uF. After a lot of testing, a single 0.1uF works just fine. **So only populate one of C5/C7 positions with a single 0.1uF capacitor!**

2. Assume $V_{cc} = 9V$. Apply a single 555 Timer pulse from Table 1 to the V_{in} terminal of the Deboo Integrator. How much will V_{out} increase? Remember an integral is the area under the curve and for the 555 Timer pulse, this amount is just the area of the rectangle formed by the pulse. Put this value in the **Analysis** column of Table 2 in the Analysis section at the end of the lab. Hint, you need to multiply by the amplitude of the input.

3. Assume that the V_{out} of the Deboo Integrator is initially at 0V as shown in the upper graph of Figure 3. The lower graph shows a sequence of pulses from the 555 Timer being applied to the input of the Deboo Integrator. Draw the resulting voltage vs. time graph of the V_{out} .

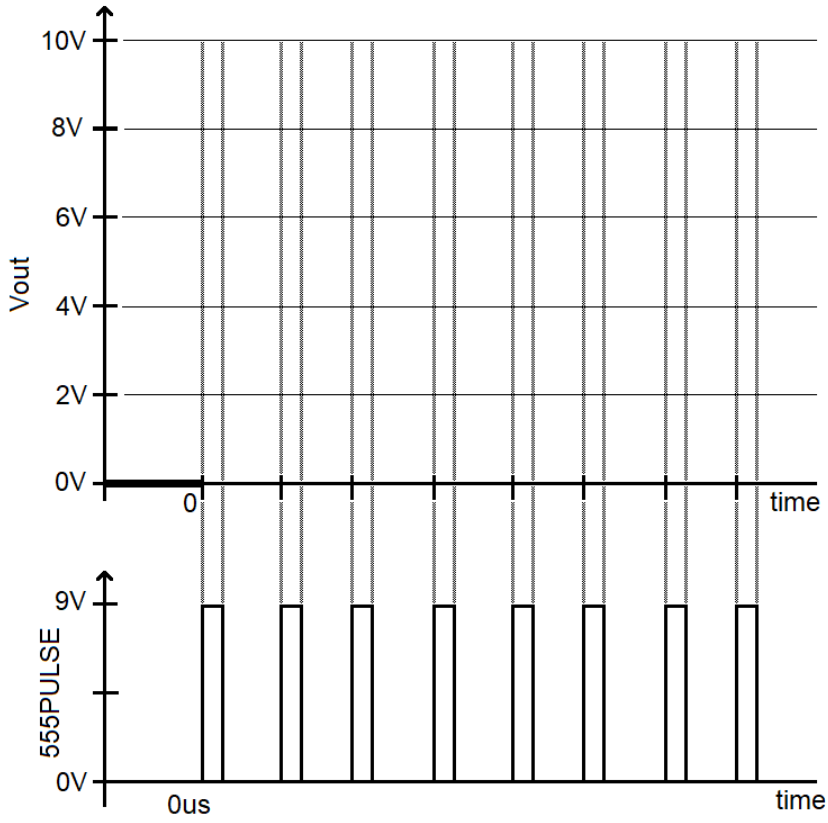


Figure 3: Complete the V_{out} curve generated by the Deboo Integrator circuit when the 555 pulse train is applied.

You would be right in concluding the staircase function will only increase as more-and-more 555 timer pulses are applied to its input. To prevent this, we will need a way to periodically remove the charge from the capacitor. We will accomplish this using the frame signal from the Schmitt Trigger Relaxation Oscillator and the Q1 MOSFET shown in Figure 1.

Resetting the Deboo Integrator Capacitor

Before diving into the interactions between these modules, let's take a moment to understand the behavior and purpose of the MOSFET. The 3-terminals of a MOSFET are called the drain (D), gate (G), and source (S). The left side of Figure 4 shows the schematic view of a MOSFET with these terminals labeled.

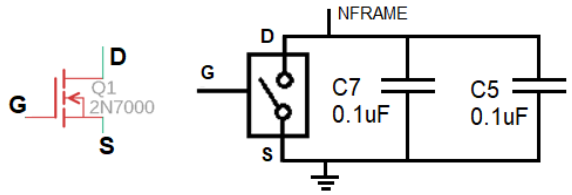


Figure 4: (Left) The schematic of a MOSFET. (Right) The equivalent circuit of the MOSFET in the Deboo Integrator.

We will remove the accumulated charge on the Deboo Integrator's pair of capacitors C7 and C5 by using the MOSFET as a voltage-controlled switch, shown on the right side of Figure 4. The behavior of this switch is given by:

- When the gate is driven towards 9V, the switch is closed. In other words, the drain and source are connected.
- When the gate is driven towards 0V, the switch is open. In other words, the drain is disconnected from the source.

Take a moment and look for the Q1 MOSFET in Figure 1.

4. What circuit (subsystem name) is supplying the signal applied to the gate of Q1?
5. During one period, how long is the FRAME signal at 0V and how long is FRAME at 9V? Use the data from Table 1.
6. How many (integer)555 Timer pulses arrive at the input of the Deboo Integrator while the gate of MOSFET, FRAME, is at 0V? Provide two answers, the fractional answer and this answer rounded down to the nearest integer.

Now consider how this signal will affect the charge on the capacitor C5 or C7.

7. When the gate of Q1 is driven towards 9V, what will happen to the capacitor C5 or C7? Will it be discharged or allowed to accumulate charge?
8. When the gate of Q1 is driven towards 0V, what will happen to the capacitor C5 or C7? Will it be discharged or allowed to accumulate charge?

Now let's put these ideas together into a picture of how the staircase waveform generated by the Deboo Integrator will look like in the simulator and when assembled.

9. Using the information, calculated in this section, estimate the height of the highest step in the Deboo Integrator output (before the Deboo is reset by the Schmitt Trigger Relaxation Oscillator).

Now, with a good understanding of how the Deboo Integrator works, let's turn to simulating this circuit to check the analysis.

Simulation: Deboo Integrator

Log into your MultiSim Live account and take a moment to verify you have a premium account. If you do not, go to the **Setup a MultiSim Live premium account** instructions in Lab 00 and do this now.

In order to more quickly build the circuit shown Figure 5, you should start by opening the Schmitt Trigger Relaxation Oscillator lab. **Immediately rename the circuit so that you do not accidently overwrite your previous work**. First, spend a few minutes adding in the other circuit elements. You may want to check that the Schmitt Trigger Relaxation Oscillator capacitor has an initial value and that your simulation uses this initial condition. Note, I provided the three probes with their respective test point with names and changed their color in order to make the simulation output more readable – make the 555TIMER test point a light color. Be mindful where you put the probes, their location is important.

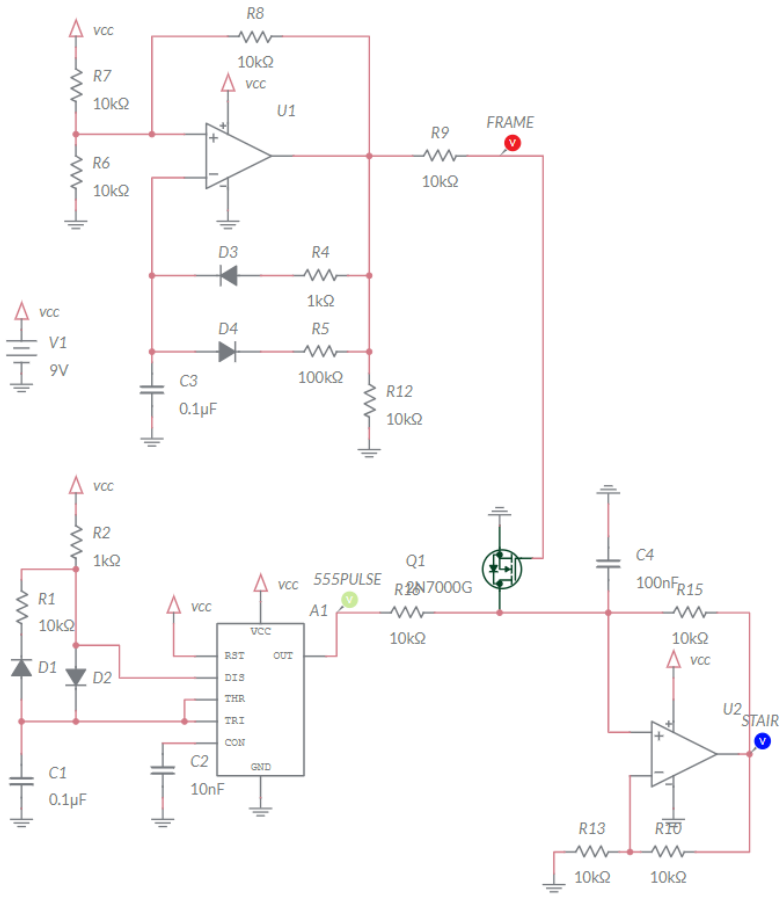
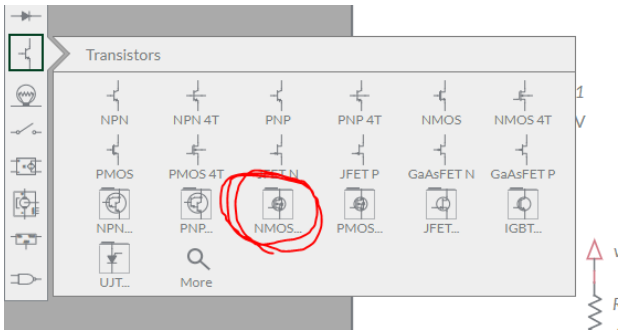
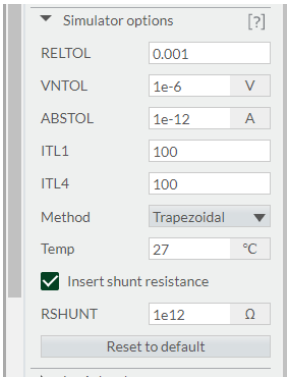


Figure 5: The Deboo Integrator together with the 555 Timer. Note the single 0.1uF capacitor C4.

The parts list for the Deboo Integrator is the same as for the Schmitt Trigger Relaxation Oscillator with the exception of the 2N7000 MOSFET. You will find this MOSFET in the NMOS submenu in the Transistors part selector.



After building the circuit and before running the circuit, you will need to make an unusual change to get the simulator to work. Go to the Document options (double click on the schematic) and find the Simulator options subwindow to the right of the screen. Change the ABSTOL parameter to 1e-8.



Now run the simulation for 5ms and include the simulated waveform with in your answers. To do this, make sure to select Zoom All and use the Export -> Grapher image from the main menu to produce an output graphic.

Use the simulated staircase waveform to determine the step height. The step height is the amount each 555 Timer pulse increases the voltage on the Deboo Integrator output. Put this value in the *Simulation* column of Table 2 in the Analysis section at the end of the lab.

Empirical: Deboo Integrator

Assemble the Deboo Integrator subsystem using the instructions in the Assembly Guide. After you have everything soldered in place and working perform the following test.

1) Power up an oscilloscope Attach a probe to Channel 1 and configure it as follows.

Ch1 probe	555PULSE test point
Ch1 ground clip	GND test point
Horizontal (scale)	100 µs
Ch1 (scale)	1V or 2V (whatever fits better)
Ch2 probe	STAIR test point
Ch2 (scale)	Same as Channel 1
Trigger mode	Auto
Trigger source	Ch2
Trigger slope	↓
Trigger level	4.5V

2) Set the GND reference of Ch1 and Ch2 to the lowest visible reticule. The waveforms will overlap the same as they did in the MultiSim simulation. Set the horizontal position of the trigger to the left most visible reticule. Take a screen shot of this output and include it in your lab report.

3) Take a screen shot of the of the 555PULSE and STAIR waveforms and include them in your lab report. Screen shot the oscilloscope traces on USB. Cell phone pictures will lose points. [Save] → Save → Format → 24-bit Bit... (*.bmp) [Save] → Save → Press to Save

Note, the STAIR waveform may be noisy if you use an 110VAC/9VDC converter. For best results, use a lab power supply.

Use the data collected from the oscilloscope to fill out the **Empirical** columns in Table 2. Determine the step size, that is, the amount each 555 Timer pulse increases the voltage on the Deboo Integrator output. All the step size, after the first step, should be the same.

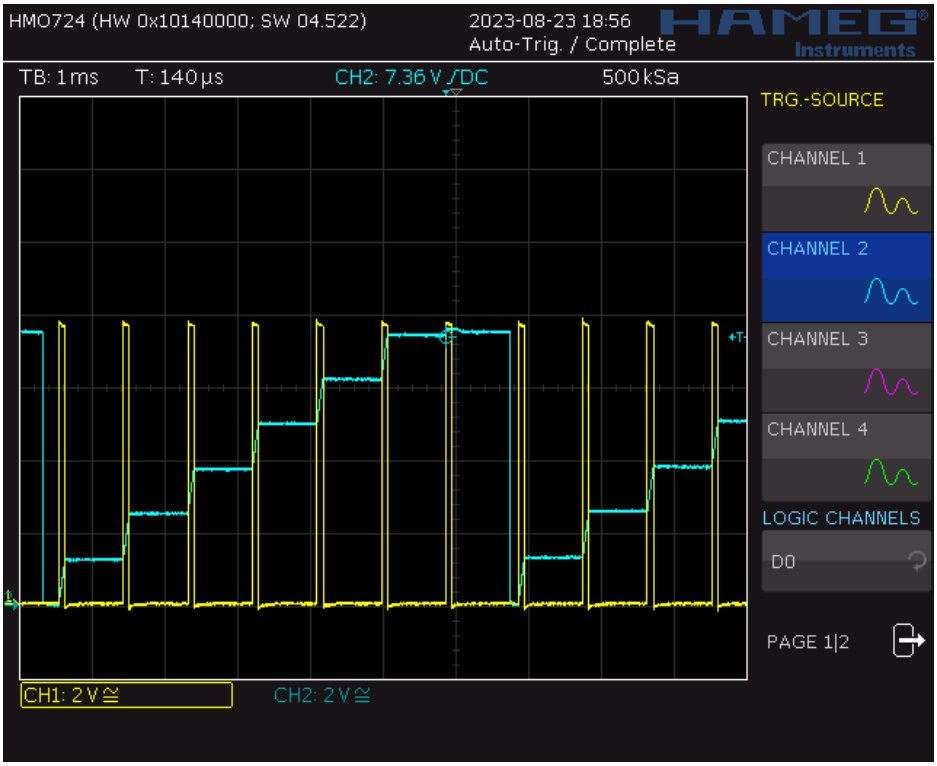


Figure 6: An oscilloscope trace showing the two output you need to capture. Note that this image was captured on a Rhode&Schwarz HMO724.

Comparison: Deboo Integrator

Complete the **Analysis, Simulation** and **Empirical** columns of the following tables using the information you found throughout this lab. Represent your answer to 3 significant figures using the units given in parenthesis in the **Quantity** column. You will need this table in later labs, so keep it handy.

Table 2: Summary of the step size calculations made for the Deboo Integrator. If your Deboo Integrators has fewer than 7 steps, leave those rows blank.

Quantity	Analysis	Simulation	Empirical
Step size			

Steps	Analysis	Simulation	Empirical
7	Leave blank		
6	9.18		
5			
4			
3		4.5	
2			
1			
0	0	0	0

Turn In: Deboo Integrator

1) Make a record of your response to numbered items below and turn in a single copy as your team's solution on Canvas using the instructions posted there.
2) Include the names of both team members at the top of your solutions.
3) Use complete English sentences to introduce what each of the items listed below is and how it was derived.

Hint, use Ctrl+click to follow links. This also works for all the Figures and Tables in these labs.

Analysis: Deboo Integrator
Steps 1-12 of analysis
Analysis: Deboo Integrator in BJT Curve Tracer
Steps 1-9 of analysis
Simulation: Deboo Integrator
Schematic (use Export -> Schematic Image)
Timing diagram (use Export -> Grapher Image)
Empirical: Deboo Integrator
Screen shot oscilloscope output for 555PULSE and STAIR.
Comparison: Deboo Integrator
Table 2 Compare Deboo Integrator output in different models.