EENG 385 - Electronic Devices and Circuits
BJT Curve Tracer: Schmitt Trigger Relaxation Oscillator
Lab Document

Objective

The objective of this lab is to introduce the use of positive feedback in the construction of an oscillator.

Analysis Schmitt Trigger Relaxation Oscillator

During today's lab you will build the circuit shown in Figure 1, a Schmitt Trigger Relaxation Oscillator. At the outset, I need to be clear, the engineering objectives of this lab could be accomplished with a 555 Timer. However, the education objective of this lab is to explore the use of positive feedback in an op amp to generator oscillatory behavior.

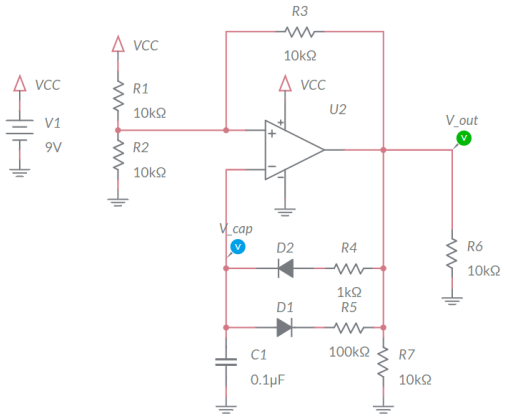


Figure 1: The Schmitt Trigger Relaxation Oscillator. The output is taken from the op amp output.

In order to analyze the circuit in Figure 1, you need to understand the behavior of a Schmitt Trigger – a circuit with one input, V_{in}, and one output, V_{out}. The Schmitt Trigger compares V_{in} against two voltage levels, V_{high} and V_{low} and assigns the output as follows:

- If ($V_{in} > V_{high}$), then V_{out} = VCC
- If ($V_{in} < V_{low}$), then V_{out} = 0V
- If ($V_{low} < V_{in} < V_{high}$), then V_{out} remains unchanged

The behavior is captured in Figure 2, a graph of V_{in} vs. V_{out}.

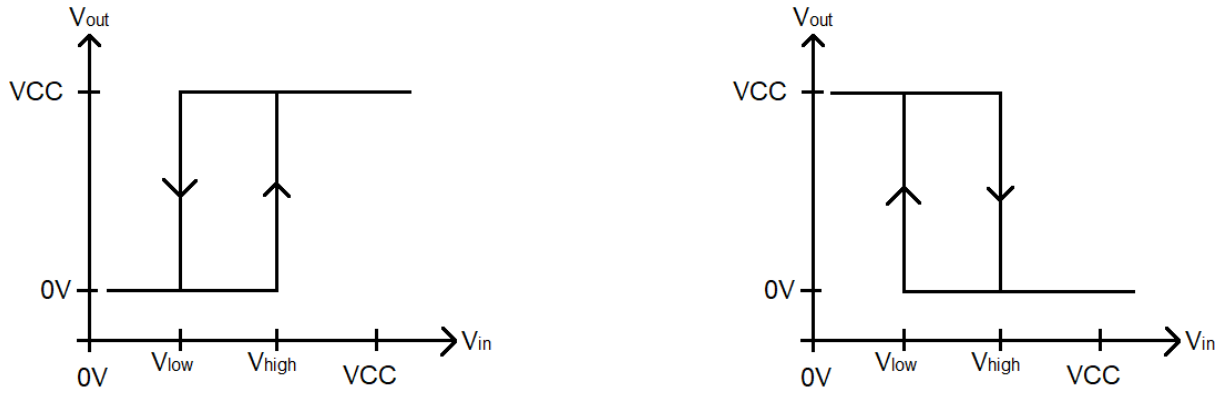


Figure 2: Input, output relationship for a Schmitt Trigger is characteristic of a system with hysteresis. Left a normal Schmitt Trigger and right, an inverting Schmitt trigger.

Let's focus on the curve to the left in Figure 2. To understand this figure, use your finger to point to the region of the horizontal axis (the V_{in} axis) which corresponds to $V_{in} > V_{high}$. Look above this region and you will see a horizontal line corresponding to V_{out} = VCC. Likewise for $V_{in} < V_{low}$ you should see that V_{out} = 0V. The tricky part of the graph is when V_{in} is between V_{low} and V_{high}. In this region, V_{out} holds on to the value it had before V_{in} entered the region between V_{low} and V_{high}.

For example, let's say V_{in} = VCC, so we know for sure that V_{out} = VCC. Now, let V_{in} decrease slowly, all the while V_{out} will stay at VCC. At some point V_{in} will become equal to and then just a smidge lower than V_{high}. At this point, V_{high} will remain unchanged at stay at VCC. As V_{in} decreases towards V_{low}, V_{out} will remain at VCC. Only when V_{in} decreases, just a smidge, below V_{low} will V_{out} switch its value to 0V. This transition is represented in Figure 2 by the downward arrow on the line connecting VCC to 0V at $V_{in} = V_{low}$.

Similarly, as V_{in} increases from 0V towards V_{high}, the output, V_{out}, will stay at 0V. Only when V_{in} increases above V_{high} will the output change to VCC. This transition is represented in Figure 2 by the upward arrow on the line connecting 0V to VCC at $V_{in} = V_{high}$.

Systems with hysteresis are well suited to reject noise from signals. Consider the example shown in Figure 3 where the top analog signal (red line) is converted into digital signal. The middle signal shows how the analog is converted when a single threshold (the grey line between V_{high} and V_{low}) is used to classify the analog signal as 1 when it is above the grey line and 0 when the analog signal is below the grey line. Any noise on the analog signal will cause this scheme to make several digital transitions.

The bottom graph in Figure 3 shows how the analog signal is converted when two thresholds, V_{high} and V_{low}, and hysteresis are used to classify the analog signal. In this scheme, the signal is classified as 0 when the analog signal is below V_{low} and classified as 1 when the analog signal is above V_{high}. When the analog signal is between the two thresholds, it retains its previous value. The resulting digital signal is much more immune to noise on the analog signal.

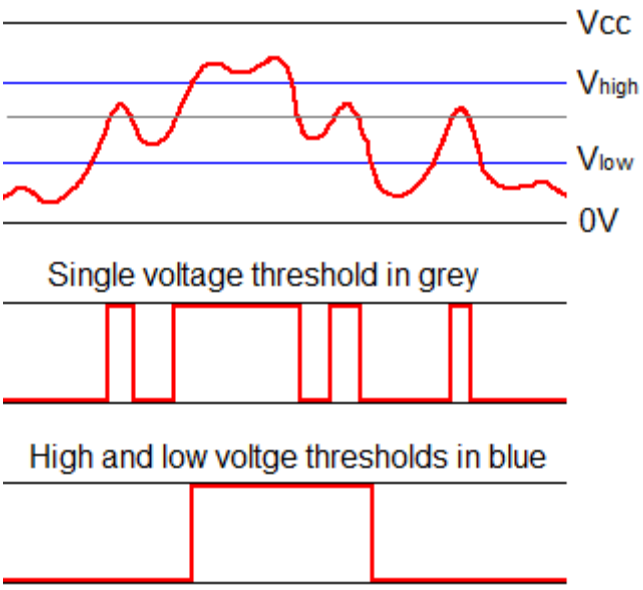


Figure 3: The top signal (in red) is converted into a digital signal using the single grey threshold (middle) and the 2 blue thresholds (lower).

Figure 4 shows a Schmitt Trigger built using an op amp and resistors. Can you identify the parts of this circuit used in the circuit shown in Figure 1? Note, the resistors are the same in both figures.

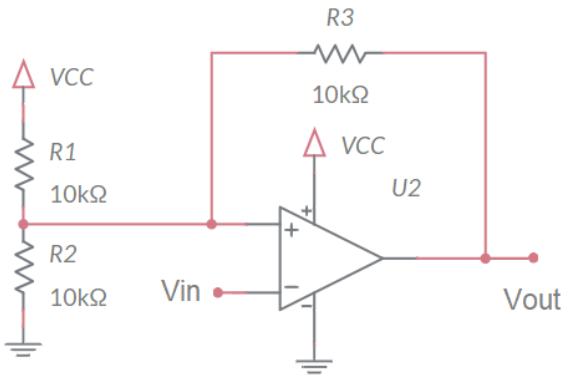


Figure 4: A Schmitt Trigger built using an op amp. Don't forget to add a 9V power supply!

Answer the following questions to understand the behavior of the circuit in Figure 4.

1. Assume V_{out} = 9V. What is the voltage at the non-inverting input of the op amp? Call this voltage V_{high}. *(Hint: Combine the parallel resistors then use Ohm's law.)*

2. Assume V_{out} = 0V. What is the voltage at the non-inverting input of the op amp? Call this voltage V_{low}. *(Hint: Combine the parallel resistors then use Ohm's law.)*

3. Imagine V_{in} is at 0V. What is V_{out}? *(Hint: The voltage on the non-inverting input of the op amp is greater than V_{low}.)*

4. Imagine increasing V_{in} from 0V to just below V_{high}. What is V_{out}? *(Hint: Use V_{out} from the Q3, since you are starting at 0V, to determine the value of non-inverting op amp input from Q1.)*

5. Imagine V_{in} continues to increase and goes just above V_{high}. What is V_{out}?

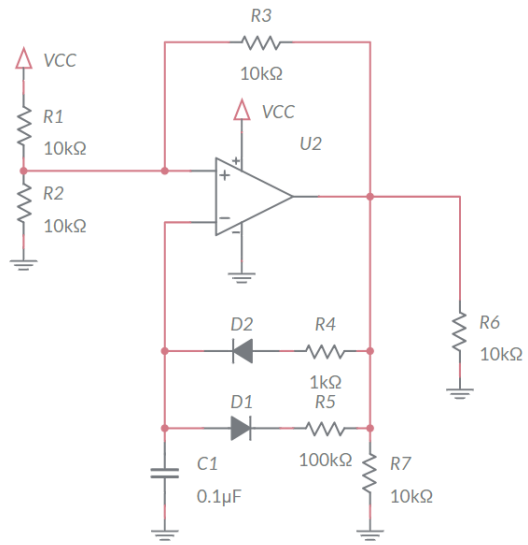
6. Imagine V_{in} is at 9V. What is V_{out}? *(Hint: The voltage on the non-inverting input of the op amp is at least V_{high}.)*

7. Imagine decreasing V_{in} from 9V to just above V_{low}. What is V_{out}? *(Hint: Use V_{out} from the Q6, since you are starting at 9V, to determine the value of non-inverting op amp input from Q2.)*

8. Imagine V_{in} continues to decrease and goes just below V_{low}. What is V_{out}?

9. Use this information to draw V_{in} vs. V_{out} hysteresis diagram similar to Figure 2. Label the V_{in}-axis with the voltage values for V_{low} and V_{out} found in Q1 and Q2.

Now with your solid understanding of the Schmitt Trigger circuit in Figure 4, it is time to apply your understanding to the operation of the larger circuit in Figure 1. Do this by working through the following questions.



10. Assume V_{out} = 9V. In this case, there is a path for electrical flow from V_{out} through R4, through the (forward biased) diode D2, to the capacitor C1 to ground. Diode D1 is reverse biased so it eliminates the 100kΩ resistor from the circuit. What is the time constant for this charging? *Hint: You can replace the forward biased diode D2 with a wire.*

11. Use this time constant to write an equation describing the voltage on capacitor C1.

12. Compute the time required for capacitor C1 to charge from V_{low} to V_{high}
    - Set the equation derived in Q11 equal to V_{high} and solve for t. Represent your answer in microseconds and round to the nearest integer.

- Set the equation you derived in Q11 equal to V_{low} and solve for *t*. Represent your answer in microseconds and round to the nearest integer.
- To derive the time to charge C1 from V_{low} to V_{high}, subtract the time to get to V_{high} from the time to get to V_{low}.

13. Assume V_{out} = 0V. In this case, there is a path for electrical flow from the charged plate of the capacitor C1 through the (forward biased) diode D1, through resistor R5 to V_{out} = 0V. Diode D2 is reverse biased so eliminates the 1kΩ resistor from the circuit. What is the time constant for this discharging? *(Hint: You can replace the forward biased diode D1 with a wire.)*

14. Use this time constant to write an equation describing the voltage on capacitor C1.

15. Compute the time required for the capacitor C1 to discharge from V_{high} to V_{low} as follows.
    - Set the $V_t(t)$ equation equal to V_{high} and solve for *t*. This equation gives the time to discharge from 9V to V_{high}. Represent your answer in milliseconds and round to three significant figures.
    - Set the $V_t(t)$ equation equal to V_{low} and solve for *t*. This equation gives the time to discharge from 9V to V_{low}. Represent your answer in milliseconds and round to three significant figures.
    - To derive the time to discharge C1 from V_{high} to V_{low}, subtract the time to get to V_{high} from the time to get to V_{low}.

Note, the capacitor C1 is connected to the inverting input of the op amp in Figure 1. Thus, the charge on this capacitor plays the role of V_{in} in Figure 4 and in the graph produced in Q9. Use your answers to these and other questions to answer the following two questions. Make sure to fill in the blanks and choose an option when a pair of **items** are separated by a "**/**".

16. When V_{out} = 9V, then the capacitor C1 is **charging/discharging** from V_{low} to V_{high}. The capacitor takes ____μs to go from V_{low} to V_{high}. When the charging/discharging capacitor's voltage exceeds $\boldsymbol{V_{low}/V_{high}}$ then V_{out} = 0V. When V_{out} = 0V, the capacitor will start to **charge/discharge** .

17. When V_{out} = 0V, then the capacitor C1 is **charging/discharging** from V_{high} to V_{low}. Now the capacitor takes ____ms to go from V_{high} to V_{low}. When the charging/discharging capacitor's voltage drops below $\boldsymbol{V_{low}/V_{high}}$, then V_{out} = 9V. When V_{out} = 9V, the capacitor will start to **charge/ discharge**.

Thus, V_{out} oscillates between 9V and 0V with the characteristics of the waveform determined by the time required to charge and discharge the capacitor C1. Use the information from this section to fill in the **Analysis** columns of Table 4 and Table 5.

Simulation Schmitt Trigger Relaxation Oscillator

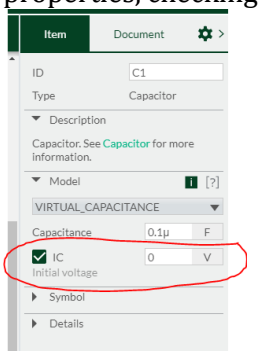
Build the circuit in Figure 1 using MultiSim Live. Make sure to attach probes to the output of the op amp and the inverting input of the op amp. The parts list is similar to last weeks; just in case, the bill of materials is given in Table 1.

Table 1: The parts list for the Schmitt Trigger Relaxation Oscillator.

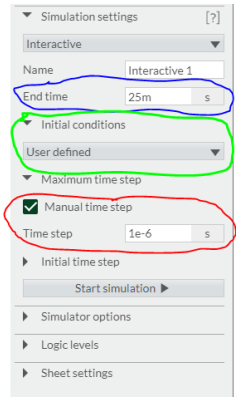
Component	Tool	Name
DC Voltage Supply	Sources	DC Voltage
Ground	Schematic connectors	Ground
VCC	Schematic connectors	Connector
Resistor	Passive	Resistor
Capacitor	Passive	Capacitor
Diode	Diodes	Diode
Op amp	Analog	5 Terminal Op amp

Once you have completed the schematic, use the export option in the main menu to output a PNG file of the schematic. Then, make some important changes in order for the simulation to run correctly.

- Set the initial voltage on the 0.1 µF capacitor to 0V. Do this by opening the 0.1 µF capacitor's properties, checking the box next to IC and entering the value "0" in the text box.



- Set the simulation time step to 1 µs. Do this by opening the document properties menu, expanding the **Maximum time step** option, checking the "Manual time step" checkbox and filling "1e-7" in the "Time step" text box.
- In this same menu, change the simulation End time to 25ms by filling "25m" in the "End time" text box.
- In this same menu, change the Initial Conditions to "User defined" by selecting this option from the pull-down menu.



Include one wavelength of the output and capacitor voltage in your answers. You can use the export option in the main menu to output a PNG file.

Figure 5: Simulation output of the circuit shown in Figure 1.

Use the V_{out} waveform to fill in the **Simulation** column in Table 4. You may want to use the cursors function available in the Item tab. If you do not see this tab, double click on a blank area of the timing diagram to make it appear.

Use the V_{cap} waveform to fill in the **Simulation** column in Table 5. Fill in the V_{high} row with the highest voltage appearing on the V_{cap} waveform. Fill in the V_{low} row with the lowest voltage appearing on the V_{cap} waveform.

Assemble Schmitt Trigger Relaxation Oscillator

This week, you will be soldering in the components associated with the SCHMITT TRIGGER RELAXATION OSCILLIATOR subsystems. This subsystem is named in Figure 6. You should solder in all the components associated with this subsystem and the resistor R10 for the RESET CIRCUIT. Table 2 lists the parts to be soldered in this week.

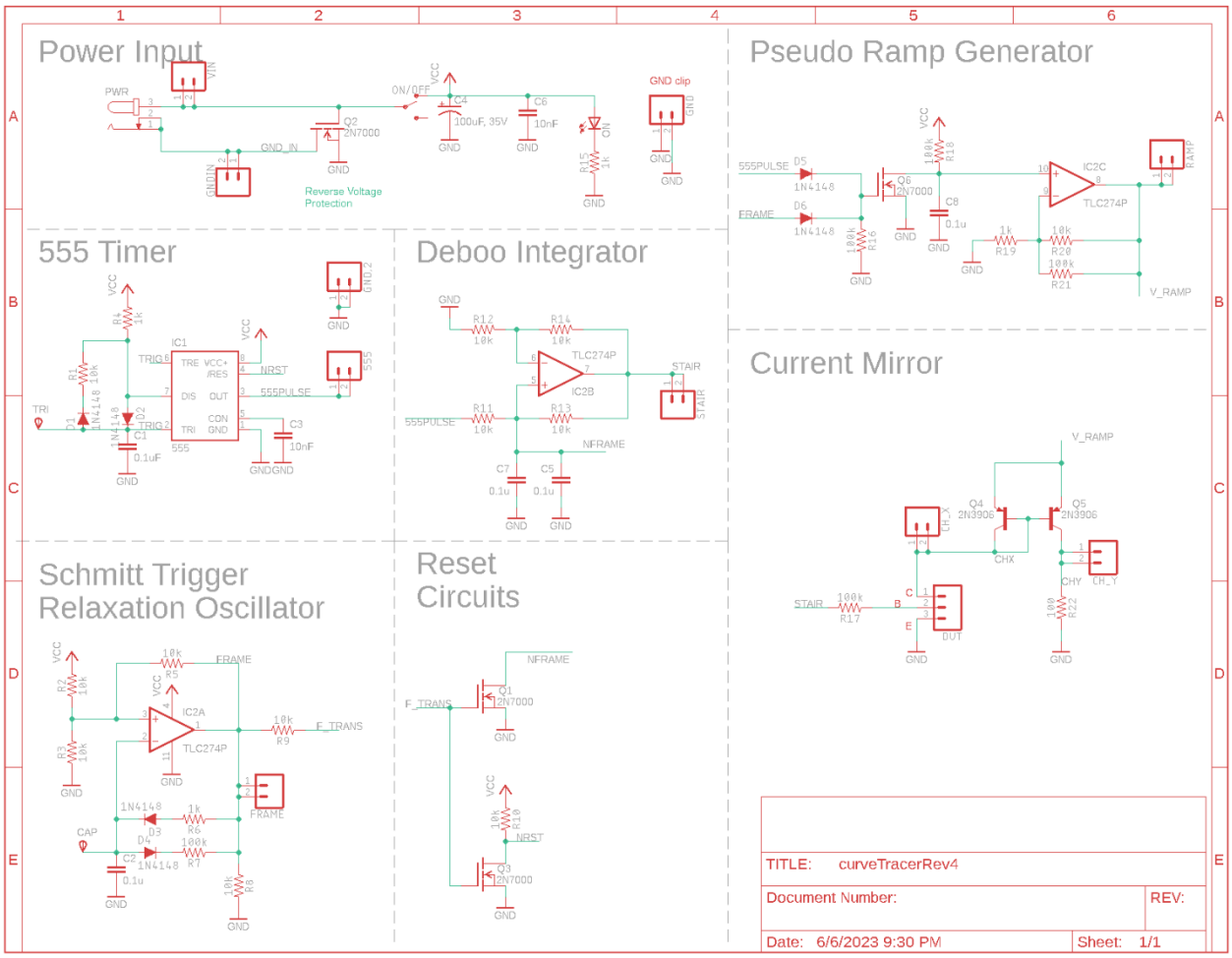


Figure 6: The schematic for the overall BJT curve tracer.

Make note of the following when assembling the Schmitt Trigger Relaxation Oscillator:

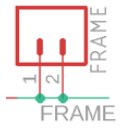
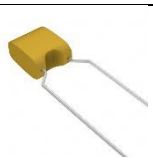
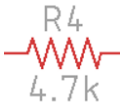
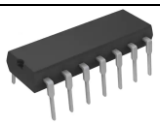
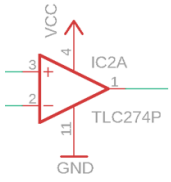
- Consider using a component tester to verify the capacitance values.
- Use a trimmed resistor lead to form the FRAME test point loop.
- This circuit has three polarized parts – the pair of diodes and the TLC274. Since you are installing a socket for the TLC274, the polarity of the op amp can easily be corrected.

Table 2: List of parts to be soldered into the PCB this week. Shaded cells are polarized components. Watch their orientation.

R2 / 10kΩ	TLC274 socket
R3 / 10kΩ	R7 / 100kΩ
R5 / 10kΩ	C2 / 0.1 µF
R9 / 10kΩ	R8 / 10 kΩ
D3 / 1N4148	R6 / 1k Ω
D4 / 1N4148	R10/10 kΩ

To make sure you can positively identify all the elements in the schematic, complete Table 3 by filling in the **Match** column with the letter corresponding to the **Schematic Symbol** for a **Physical Part**.

Table 3: Match the schematic symbol with the corresponding part.

Schematic Symbol	Match	Physical Part
A 		
B 		
C 		
D 		
E 	A	

Soldering Tips

Work on being patient with the heat from the solder iron soaking into the PCB pad and the part leads. Use a small dab of liquid solder on the tip of the iron to facilitate heat transfer. When everything is nice and hot, the small dab of solder will wick onto the PCB pad and component lead. When this happens, start to melt a small length (less than the join will need) into the interface between the iron tip and the component and PCB pad. Remove the solder while leaving the soldering iron tip in place to make a quick appraisal: Can the joint can take a little more solder? If so, add another little dab of solder. When done, remove the solder first, then the iron. When you get the knack of it, this should take about 5 seconds. Work on improving your work from last week – take your time.

When complete, your BJT Curve Tracer board should look like Figure 7. Note, I have installed the op amp into the socket.

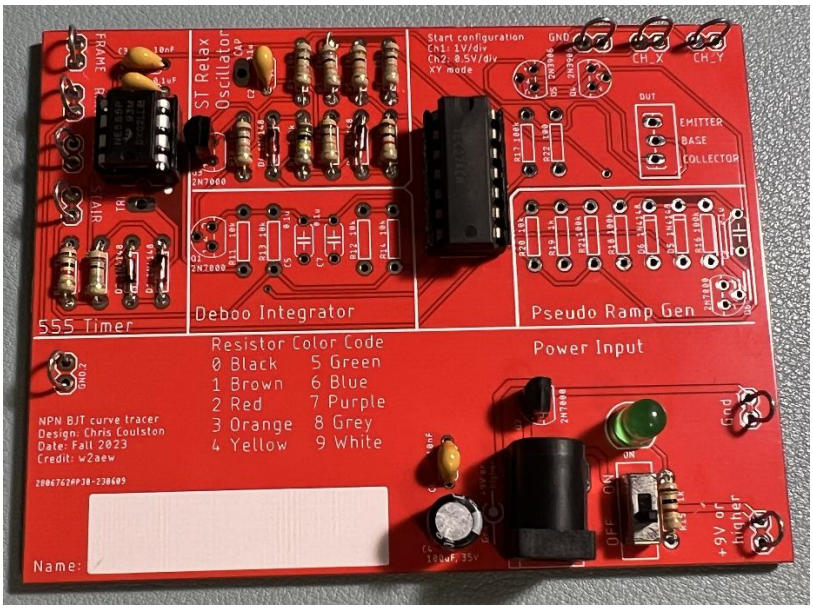


Figure 7: The completed (for Lab 2) BJT curve tracer board. Note, this board is an older version of the board with a 47 kΩ resistor in the place where you should install the 33 kΩ resistor.

After you solder in all the components, you should test and correct any problems.

Test ST RELAX OSCILLATOR Subsystem

1) Check the resistance between the "+9V or higher" and "Gnd" test points with the ON/OFF switch in the OFF position. You should get an overload condition on the DMM – there is essentially infinite resistance with the switch in the OFF position.
2) Check the resistance between the "+9V or higher" and "Gnd" test points with the ON/OFF switch in the ON position. This measurement jumps around and may show negative resistance. The value displayed is not meaningful.
3) Power up the BJT curve tracer:
    - Put the ON/OFF switch in the OFF position,
    - Apply power to the board either through your AC/DC converter or using the lab power supply. If you are using the lab power supply, set the voltage to 9V and the current to 100 mA.
    - Put the ON/OFF switch to the ON position.
    - The green LED should illuminate.
4) Power up an oscilloscope. Attach a probe to Channel 1 and configure it as follows.

Ch 1 probe	FRAME test point
Ch 1 ground clip	GND test point
Horizontal (scale)	1 ms
Ch 1 (scale)	1 V or 2 V (whatever fits better)
Ch 2 probe	Inverting input of op amp
Ch 2 (scale)	Same as Channel 1
Trigger mode	Auto
Trigger source	Ch1
Trigger slope	↑

Trigger level	4.5V

Set the GND reference of Ch 1 and Ch 2 to the lowest visible reticule – the waveforms will overlap the same as they did in the MultiSim simulation. Set the horizontal position of the trigger to the left most visible reticule. Note, the op amp output is sent to the FRAME test point. The capacitor charge is available by attaching an oscilloscope probe to the CAP test point shown in Figure 8.

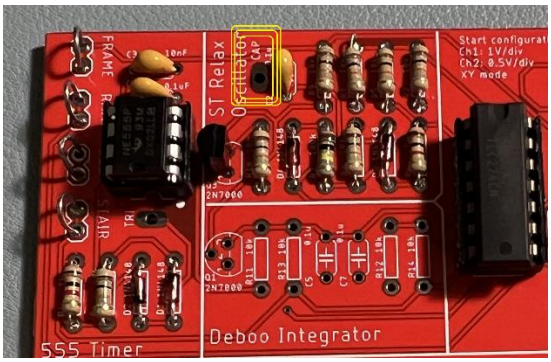
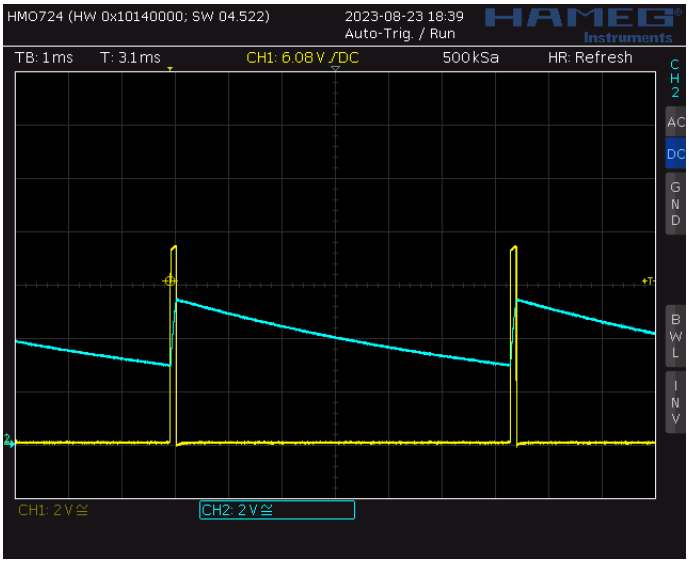


Figure 8:You can probe the capacitor voltage at the yellow circled test point.

After you get everything setup, take a screen shot of the V_{out} and $_{Vcap}$ waveforms to include in your lab report. You may want to apply the Acquire function to average 32 waveforms together to smooth the waveforms. Use the data collected from the oscilloscope to fill out the **Assemble** columns in Table 4, and Table 5.



Note, this oscilloscope trace was captured on a Rhode&Schwarz HMO724.

Debugging ST RELAX OSCILLATOR Subsystem

I would expect most problems with this subsystem to be the result of:

- Bad solder connection

- Diodes soldered in backwards
- Wrong component (resistor or capacitor)

If your BJT curve tracer board fails one of the test steps in the previous section, here is some guidance on what may have happened and how to correct it.

1) If you are getting low resistance with the ON/OFF switch in the OFF position:
    - Make sure the ON/OFF switch is in the OFF position.
    - Check for solder bridges on the rear of your PCB.
    - Make sure you are reading the DMM correctly. The reading when the ON/OFF switch in the OFF position should be the same as when you hold the probes apart in air.
2) If you are getting a different resistance with the ON/OFF switch in the ON position:
    - Make sure the ON/OFF switch is in the ON position.
    - Make sure you are reading the DMM correctly. The reading when the ON/OFF switch in the ON position will jump around a lot and probably be negative.
3) If the green LED does not illuminate when power is applied to the ON/OFF and the switch is in the ON position:
    - Test power is supplied. Put a DMM in voltage mode and check the +9V and Gnd test points.
    - Check for solder bridges on the rear of the PCB.
4) If you are not getting waveforms resembling the MultiSim Live simulation:
    - Test that the board is powered up.
    - Check the oscilloscope leads are fully inserted.
    - Press the "Default Setup'" button to undo any weird configuration the last user may have left the oscilloscope in.
    - Check solder connections by trying to wiggle each component. No visible movement should be possible.
    - Check all pins of the TLC274 are firmly engaged into the IC socket.

Turn In:

1) Make a record of your response to numbered items below and turn in a single copy as your team's solution on Canvas using the instructions posted there.
2) Include the names of both team members at the top of your solutions.
3) Use complete English sentences to introduce what each of the items listed below is and how it was derived.

Analysis Schmitt Trigger Relaxation Oscillator

Steps 1 – 17.
Fill in **Analysis** column of Table 4.
Fill in **Analysis** column of Table 5.

Simulation Schmitt Trigger Relaxation Oscillator

Schematic (use Export -> Schematic Image).
Timing diagram (use Export -> Grapher Image).
Fill in **Simulation** column of Table 4.
Fill in **Simulation** column of Table 5.

Assemble Schmitt Trigger Relaxation Oscillator

Complete Table 3**.**
Fill in **Assemble** column of Table 4.
Fill in **Assemble** column of Table 5.

Analysis

Complete the following table using the information you found in the following sections. Represent your answer in 2 or 3 significant figures using the units given in parenthesis in the **Quantity** column.

Table 4: Summary of V_{out} behavior in the Schmitt Trigger Relaxation Oscillator.

Quantity	Analysis	Simulation	Assemble
Time high (us)	89 us		
Time low (us)			
Period (us)		8091 us	
Frequency (Hz)			
Duty Cycle			

Table 5: Summary of the 0.1µF capacitor voltage in the Schmitt Trigger Relaxation Oscillator.

Quantity	Analysis	Simulation	Assemble
V_{high}	6.7 V		
V_{low}			