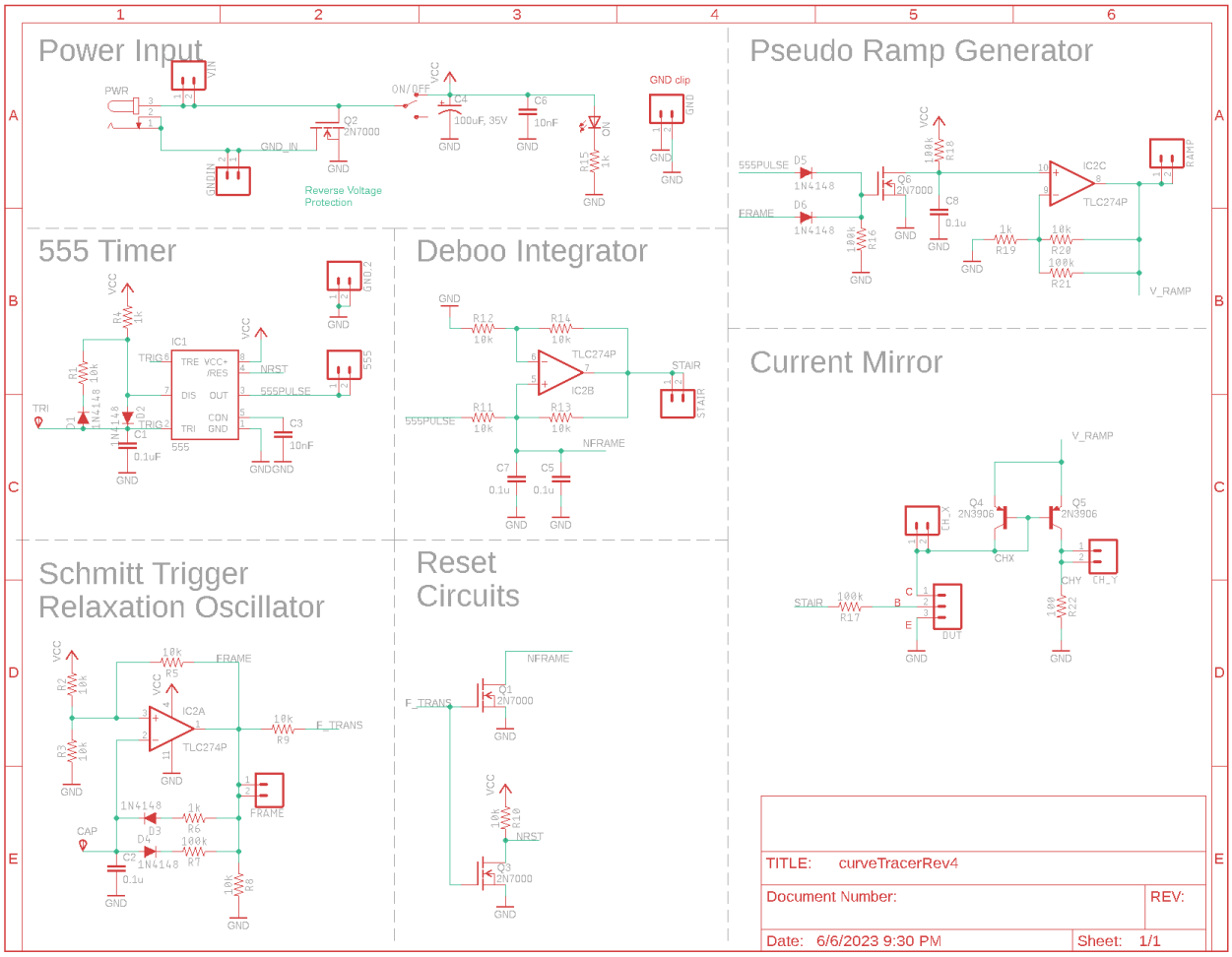
ELECTRICAL ENGINEERING DEPARTMENT
COLORADO SCHOOL OF MINES

EENG 385 Workbook

Created by Dr. Christopher Coulston

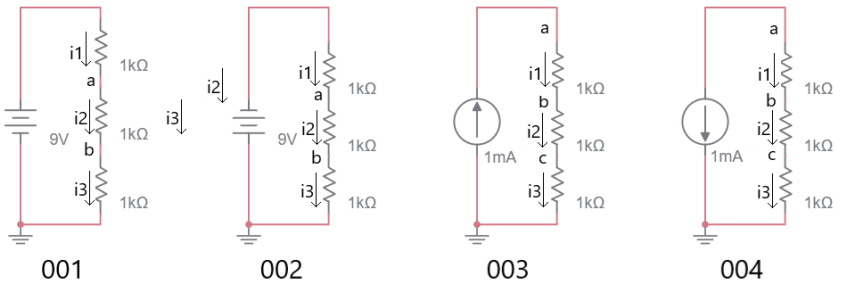
Fall 2025

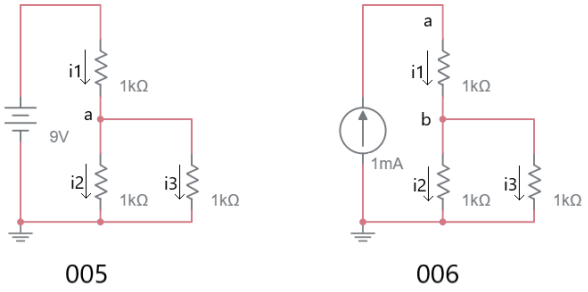


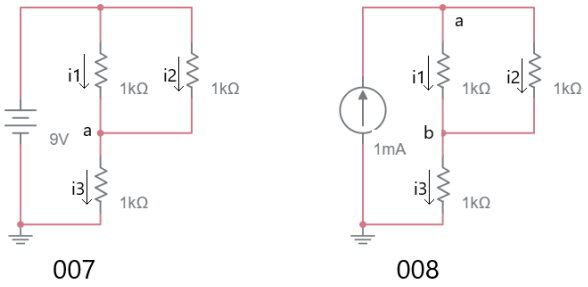
Chapter: Review

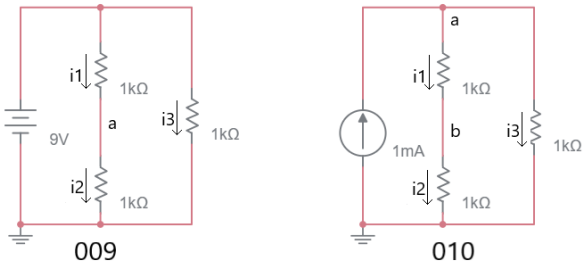
Circuits with resistors, voltage and current sources

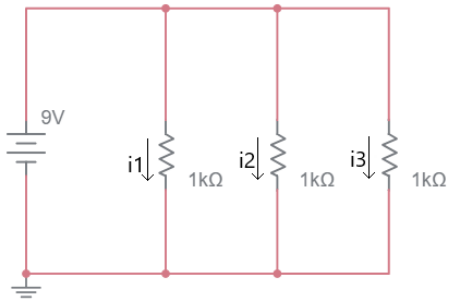
Determine all voltages and currents. Round you answer to 2-significant figures and include units. If the circuit does not have the variable asked for in the table, leave that entry blank.



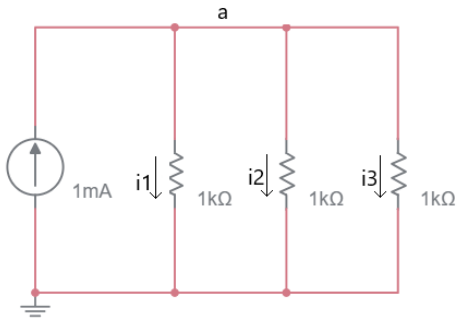








011



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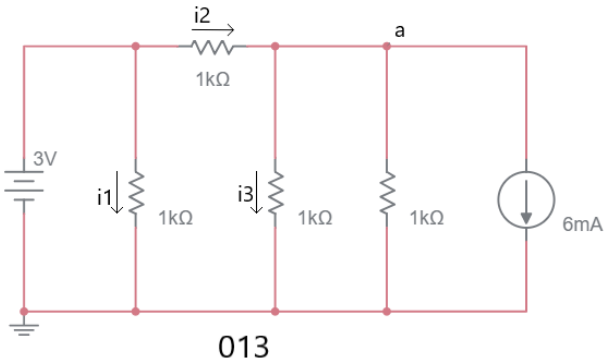


013

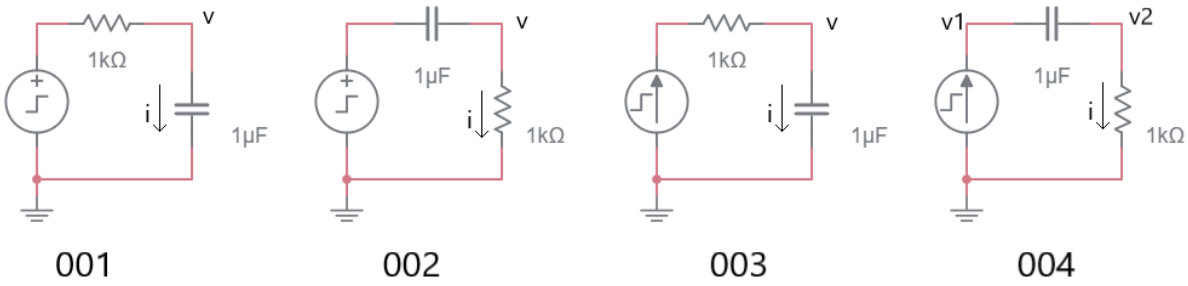
Circuit	a	b	c	i1	i2	i3
001						
002						
003						
004						
005						
006						
007						
008						
009						
010						
011						
012						
013						

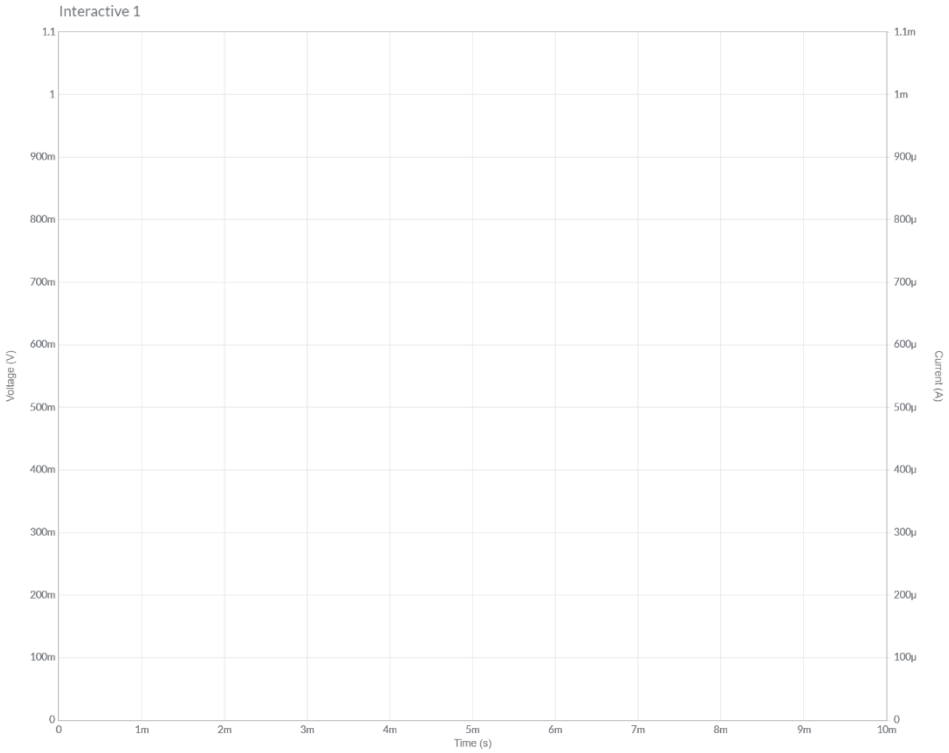
Circuits with resistors and capacitors

Plot all voltage across the capacitor and the current through the capacitor as a function of time. Assume that the capacitor is initially discharged; in other words, the voltage across the capacitor is 0V at time 0.

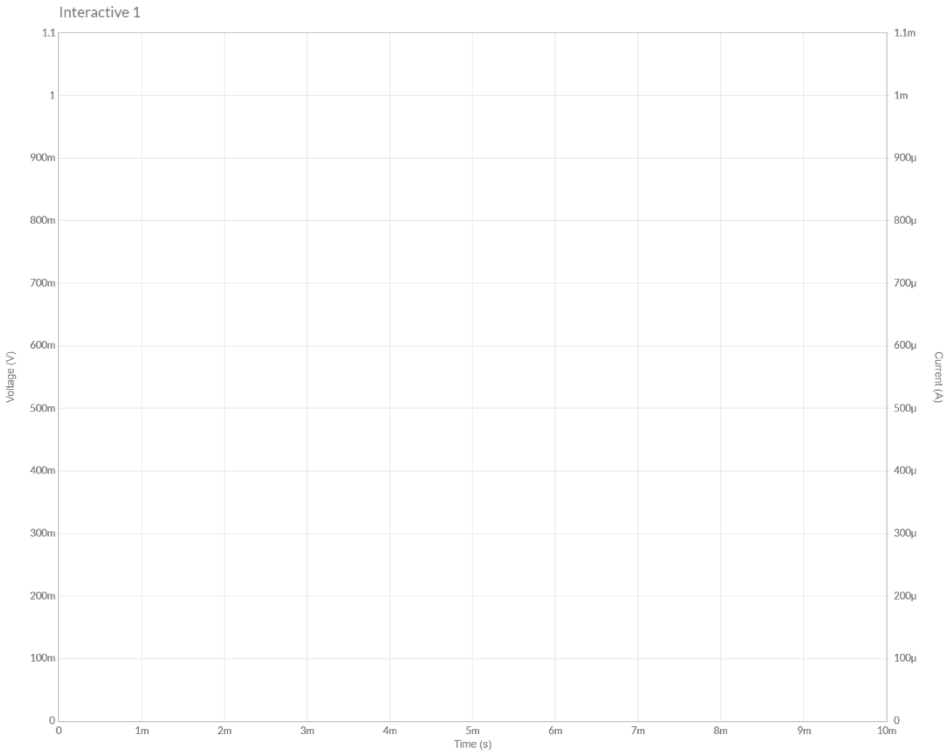
The  symbol is a unit step voltage source that goes from 0V to 1V at time 0.

The  symbol is a unit step current source that goes from 0V to 1mA at time 0.

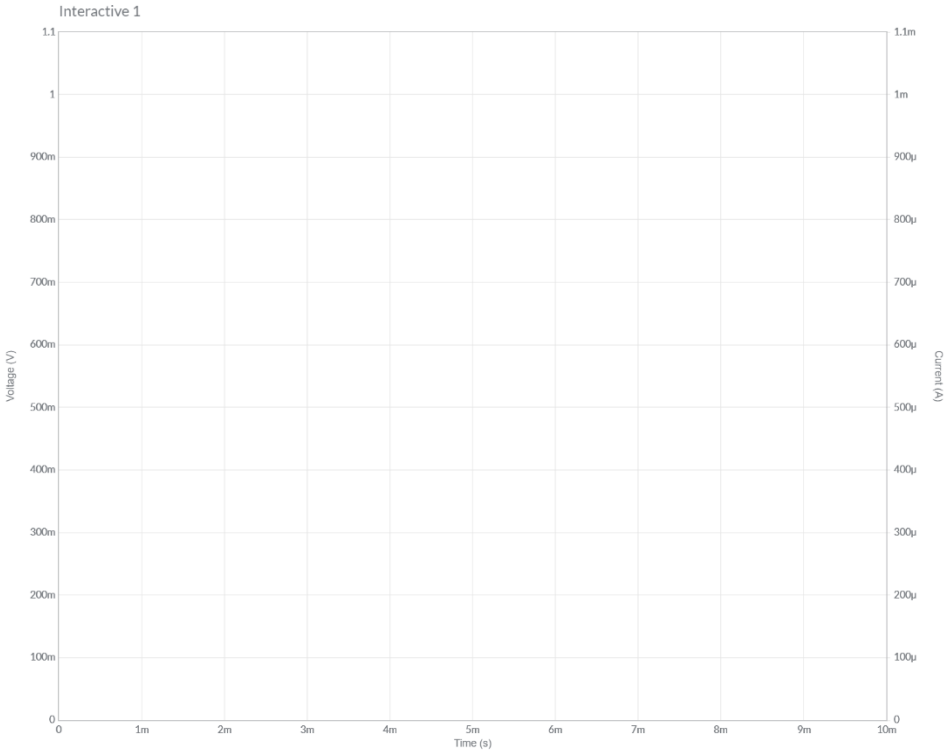




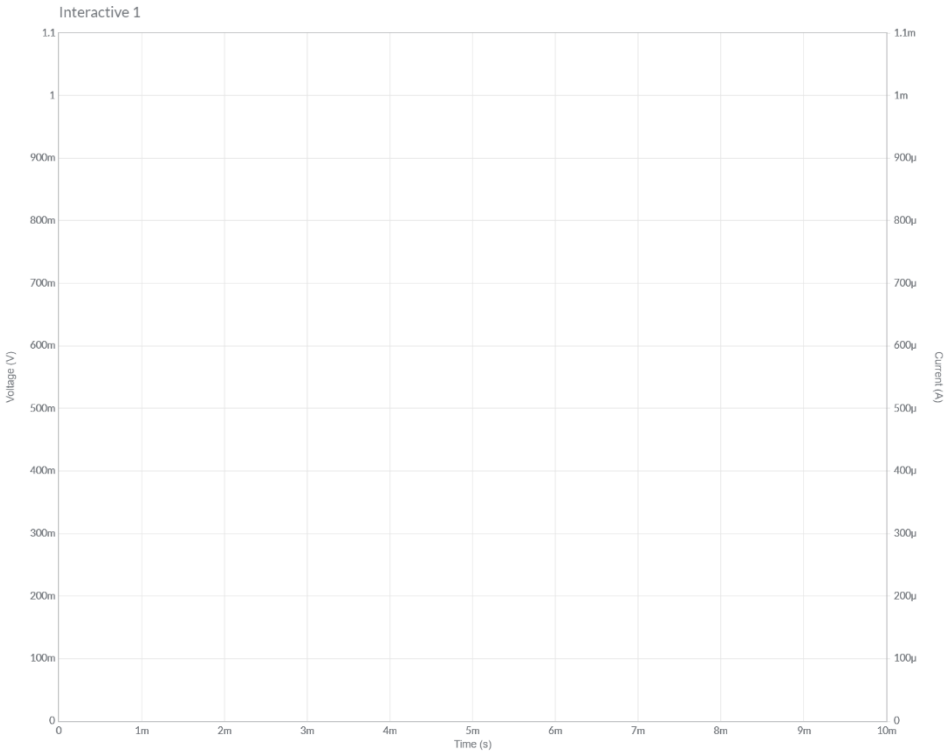
Plot the voltage and current for the circuit labeled 001.



Plot the voltage and current for the circuit labeled 002.

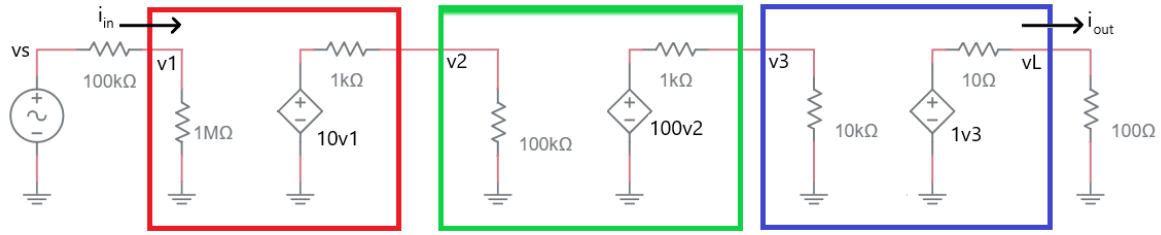


Plot the voltage and current for the circuit labeled 003.



Plot the voltage and current for the circuit labeled 004.

Multistage amplifiers and dependent sources



Determine the voltage gain vL/vs

Step 0

Determine the gain v1/vs by examining the voltage divider formed by the source and the input to the first (red) stage.

Step 1

Determine the gain v2/v1 by examining the voltage divider formed by the output of the first stage (red) and the input to the second stage (green).

Step 2

Determine the gain v3/v2 by examining the voltage divider formed by the output of the second stage (green) and the input to the third stage (blue).

Step 3

Determine the gain vL/v3 by examining the voltage divider formed by the output of the third stage (blue) and the load resistor.

Step 4

Multiply the ratios so that you come out with vL/vs

Determine the current gain $A_i = i_{out}/i_{in}$

Step 1

Using Ohm's law at the input and output

Step 2

Use the step 1 equations to form i_{out}/i_{in}

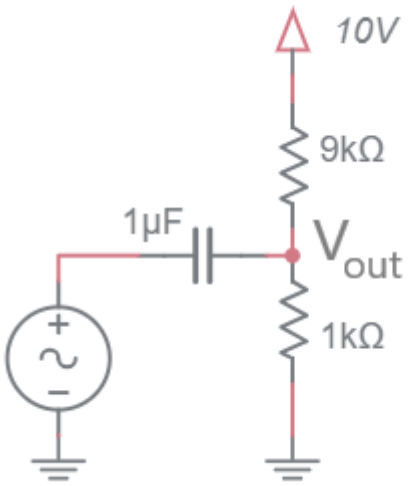
DC and AC simplifications for common circuit elements

As an engineer you will often need to make quick estimate of a circuit's behavior. In these cases, it is completely appropriate to make approximations of component behavior to simplify the analysis.

Element	DC Model	AC Model
Resistor	R	R
Capacitor	Open	C
Inductor	Short	L
Voltage Source	V	Short
Current Source	I	Open

Practical Application – Coupling AC signal on a DC bias

The following circuit is very useful as it allows an AC signal to be DC biased at any level you need. In order to understand how this circuit operates, you will need to invoke the principle of superposition. Superposition dictates that the total response of a system is the sum of the partial response. A partial response is the contributions that one energy source has on the output while all the other energy sources are set to 0. So, in terms of the schematic given the total response is the sum of the partial response due to the AC source (with the 10V supply set to 0V), plus the partial response due to the DC source (with the AC source set to 0).



In this analysis, assume that the AC source is described by 0.5sin(6,280t), a 1V peak to peak 1kHz sine wave.

In the Draw the schematic row, draw the equivalent circuit for each source. For example:

- In the AC Source column draw the schematic with all components replaced by their AC equivalent model from the table in the **DC and AC simplifications for common circuit elements** section and setting the 10V supply to 0V.
- In the DC Source column draw the schematic with all components replaced by their DC equivalent model from the table in the **DC and AC simplifications for common circuit elements** section and setting the AC source to 0V.

In the Vout row, use circuit theory to determine the value of Vout.

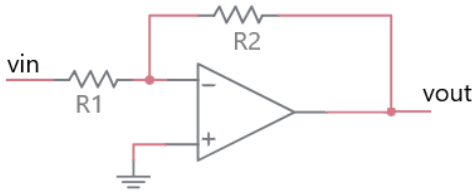
In the Total Response row add together the AC and DC contributions.

	AC Source (Set DC source to 0)	DC Source (Set AC source to 0)
Draw the schematic		
Vout		
Total Response		

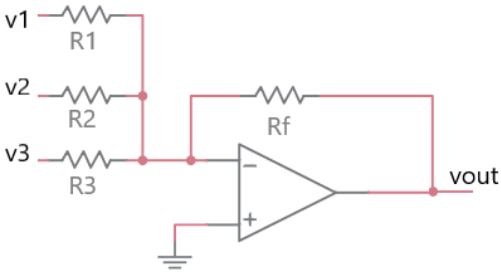
Chapter: Opamp

Circuits with opamps and resistors

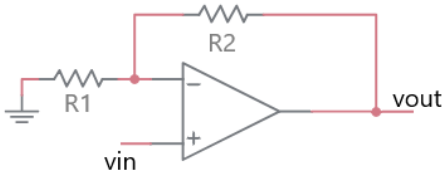
Determine the gain (vout/vin) for circuits 001 and 003. Compute vout in terms of v1, v2, v3 for circuits 002 and 004.



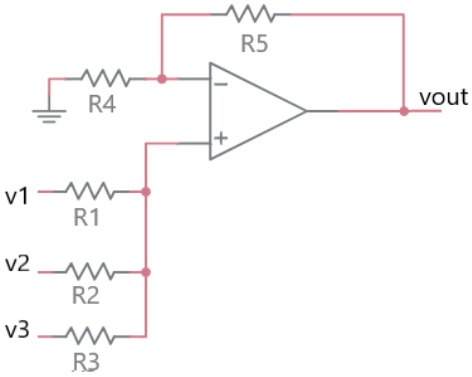
001



002



003

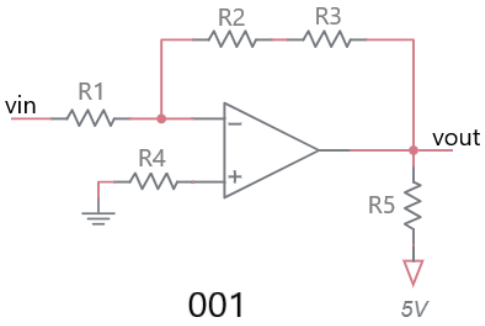


004

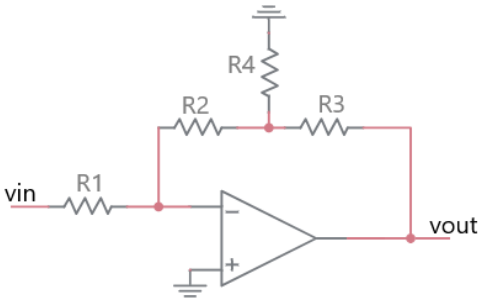
Circuit	Gain or vout
001	
002	
003	
004	

Circuits with opamps and resistors

Determine the gain (vout/vin) for the following circuits.



001

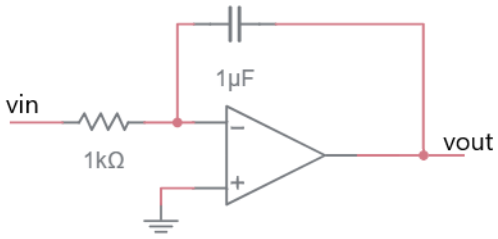


002

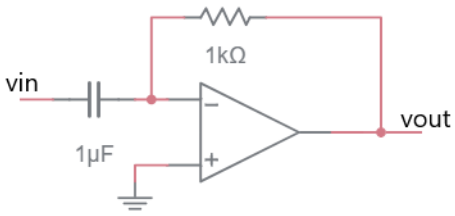
Circuit	Gain
001	
002	

Circuits with opamps, capacitors and resistors

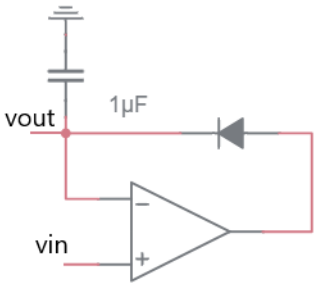
For each of the circuits, plot vout in terms of the input signal (in green) given.



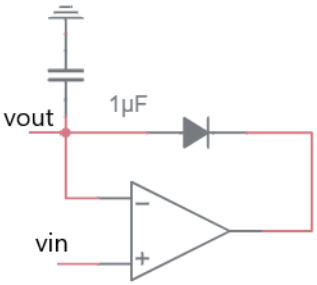
001



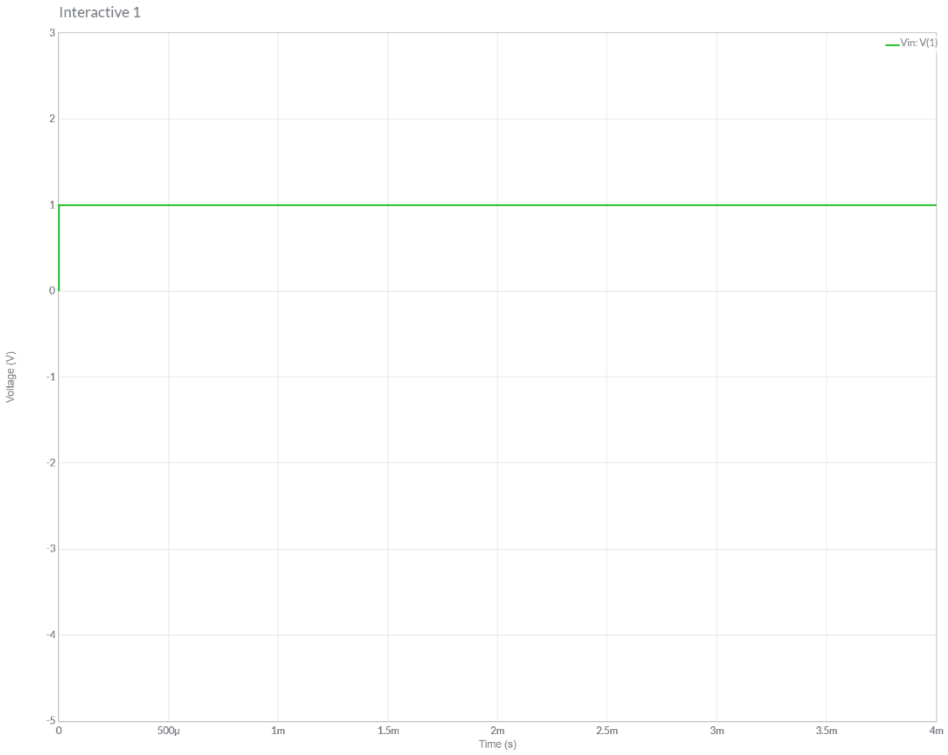
002



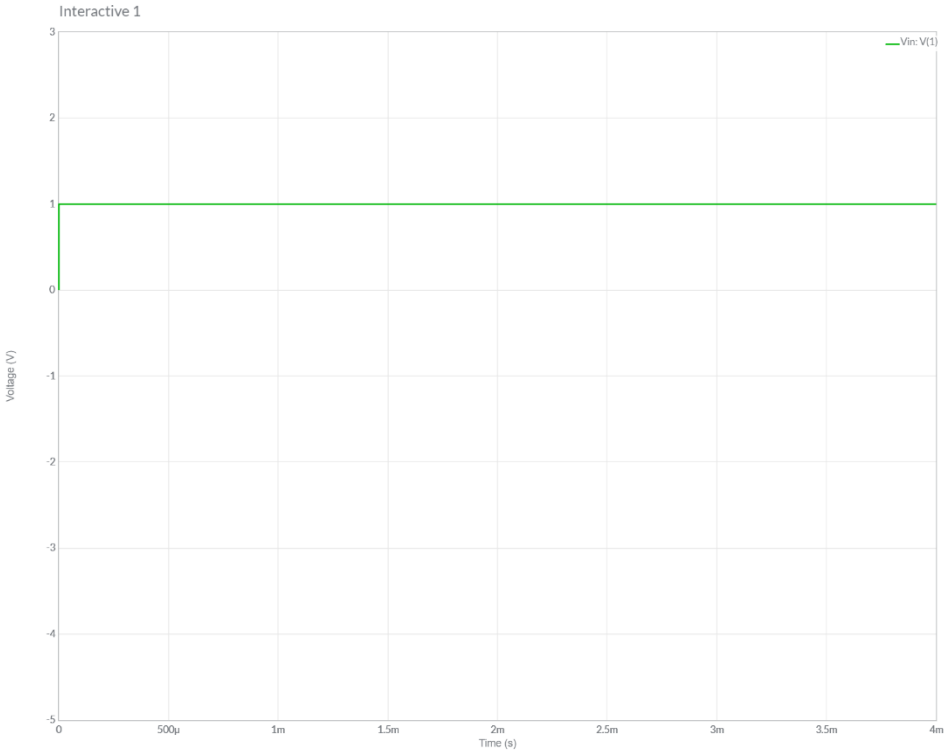
003



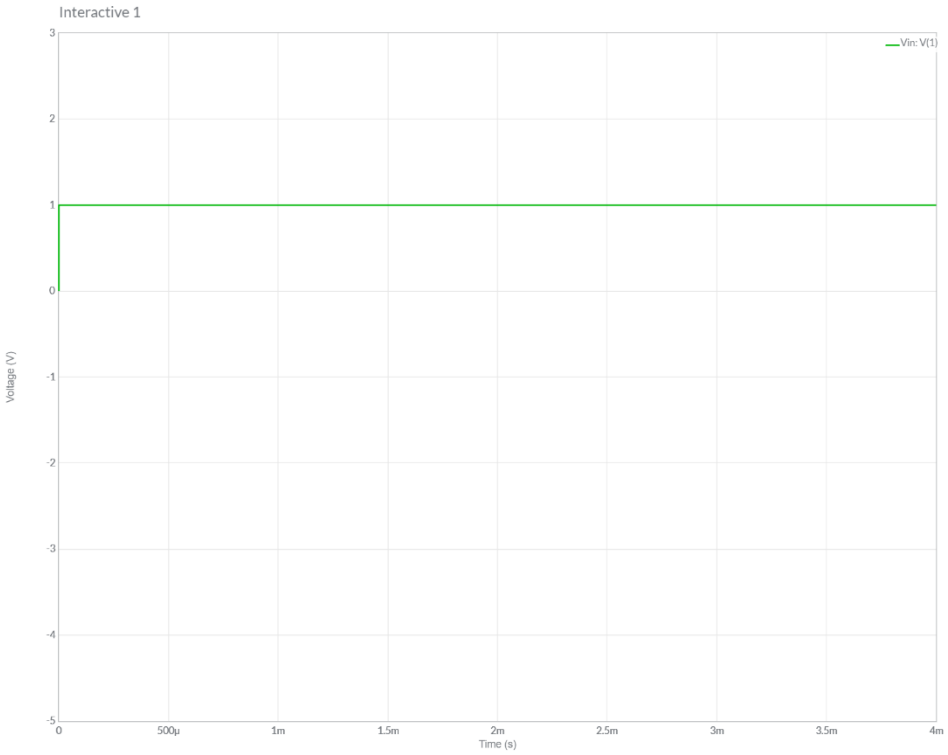
004



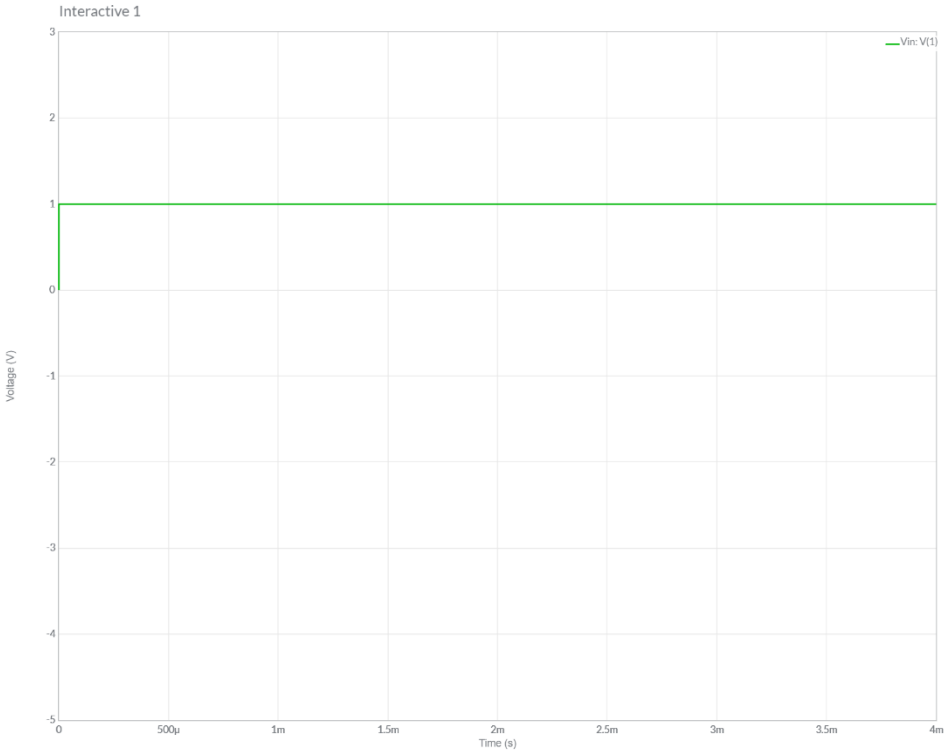
Plot vout for the circuit labeled 001.



Plot vout for the circuit labeled 002.



Plot vout for the circuit labeled 003.



Plot vout for the circuit labeled 004.

The purpose of this assignment is to analyze the schematic of a circuit, built mostly with opamps, that implements a fully analog PID controller based on the architecture shown in the following diagram.

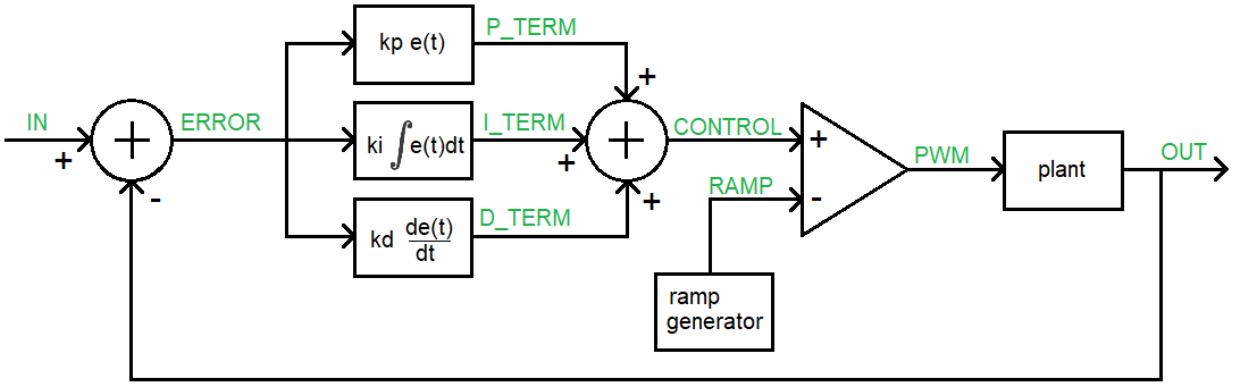
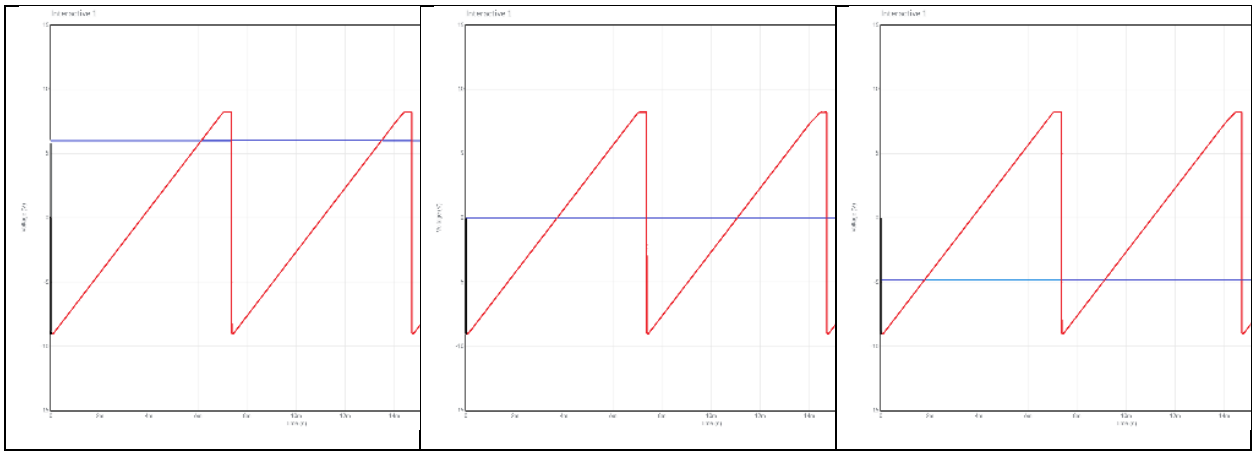


Figure 1: A PID controller subtracts the output from the input to generate an error signal. The error signal, its integral and derivative are multiplied by adjustable constants, added together, and then used to generate a PWM signal whose duty cycle is proportional to the control signal. The PWM signal is the input to the plant (thing that we want to control) which generated the observable output that is feedback into this loop.

Your task is to identify the building blocks in the schematic, analyze their behavior and relate these building blocks to the PID controller shown in Figure 1. When referencing opamps in the schematic, use the "ICxx" label, not the "TLC274P" label. When needed, assume that VCC=9V and VSS=-9V. Annoying to setup but this allows the error to be either positive or negative according to the sign of the voltage – very usefully semantically.

1) The first summer junction
    a. What opamp and resistors form the summer junction that outputs ERROR in Figure 1?
    b. Write an equation for the output ERROR in terms of IN and OUT.
2) The proportional term, P_TERM, is formed by two opamps. ERROR is the input to the first stage and P_TERM is the output from the second stage.
    a. What opamp/resistors in the form the first stage of the P_TERM in Figure 1?
    b. What is the range of the gain of this circuit? Make sure to include the sign.
    c. What opamp/resistors form the second stage of the P_TERM in Figure 1?
    d. What is the gain of this second stage?
    e. What is the purpose of this second opamp stage?
    f. Why didn't I use a non-inverting opamp instead of this 2-stage approach? Hint, look at your answer for part b.
3) The integral term, I_TERM, is formed by two opamps. ERROR is the input to the first stage and I_TERM is the output from the second stage.
    a. What opamp/resistors in the form the first stage of the I_TERM in Figure 1?

   b. Where have you seen this circuit before?
   c. What opamp/resistors form the second stage of the I_TERM in Figure 1?
   d. Write an equation for the output of the second stage, I_TERM, in terms of the input (call it ERROR) and C and R. Use C and R in your equation, not their values of uF and 10kΩ.
   e. Why did I use an inverting integrator circuit instead of a non-inverting integrator?
4) The derivative term, D_TERM, is formed by two opamps. ERROR is the input to the first stage and D_TERM is the output from the second stage.
   a. What opamp/resistors in the form the first stage of the D_TERM in Figure 1?
   b. Where have you seen this circuit before?
   c. What opamp/resistors form the second stage of the D_TERM in Figure 1?
   d. Write an equation for the output of the second stage, D_TERM, in terms of the input (call it ERROR) and C and R. Use C and R in your equation, not their values of 1uF and 10kΩ.
   e. Why did I use an inverting differentiator circuit instead of a non-inverting differentiator?
5) The second summer junction
   a. What opamp and resistors form the summer junction that outputs CONTROL in Figure 1?
   b. Write an equation for the output CONTROL in terms of P_TERM, I_TERM and D_TERM.
   c. What value "should" the 3.3kΩ have? Why did I choose 3.3kΩ instead of this value?
   d. Why did I use an non-inverting summer instead of the simpler inverting summer?
6) The ramp generator is identical to the one you built in Lab 2. Using your lab results will simplify answering the questions in this section.
   a. What components form the Schmitt Trigger Relaxation Oscillator (STRO)?
   b. What is the period/frequency and duty cycle of the waveform generated by the STRO? Assume that potentiometer R35 is set to 0Ω.
   c. Does R35 effect the time high or time low of the STRO waveform?
   d. Components T1, T2, R29, and R30 forms a 0.7mA current source leaving the "bottom" of T1 (it's collector). Assume that C10 is not populated, how long does it take to charge C9 from -9V to +9V? How would you describe the shape of the voltage vs. time waveform?
   e. What is the role of Q1 in generating the RAMP waveform?
   f. What is the role of R35 is this circuit?
7) The comparator
   a. Given RAMP (in red) and CONTROL (in blue) shown in the following timing diagrams, draw the output PWM signal using the open-loop opamp configuration shown in Figure 1.



b. What is the relationship between the CONTROL signal and the duty cycle of the PWM signal? To determine this, plot the duty cycle vs control voltage and then write an equation to describe the straight line y=mx+b style.

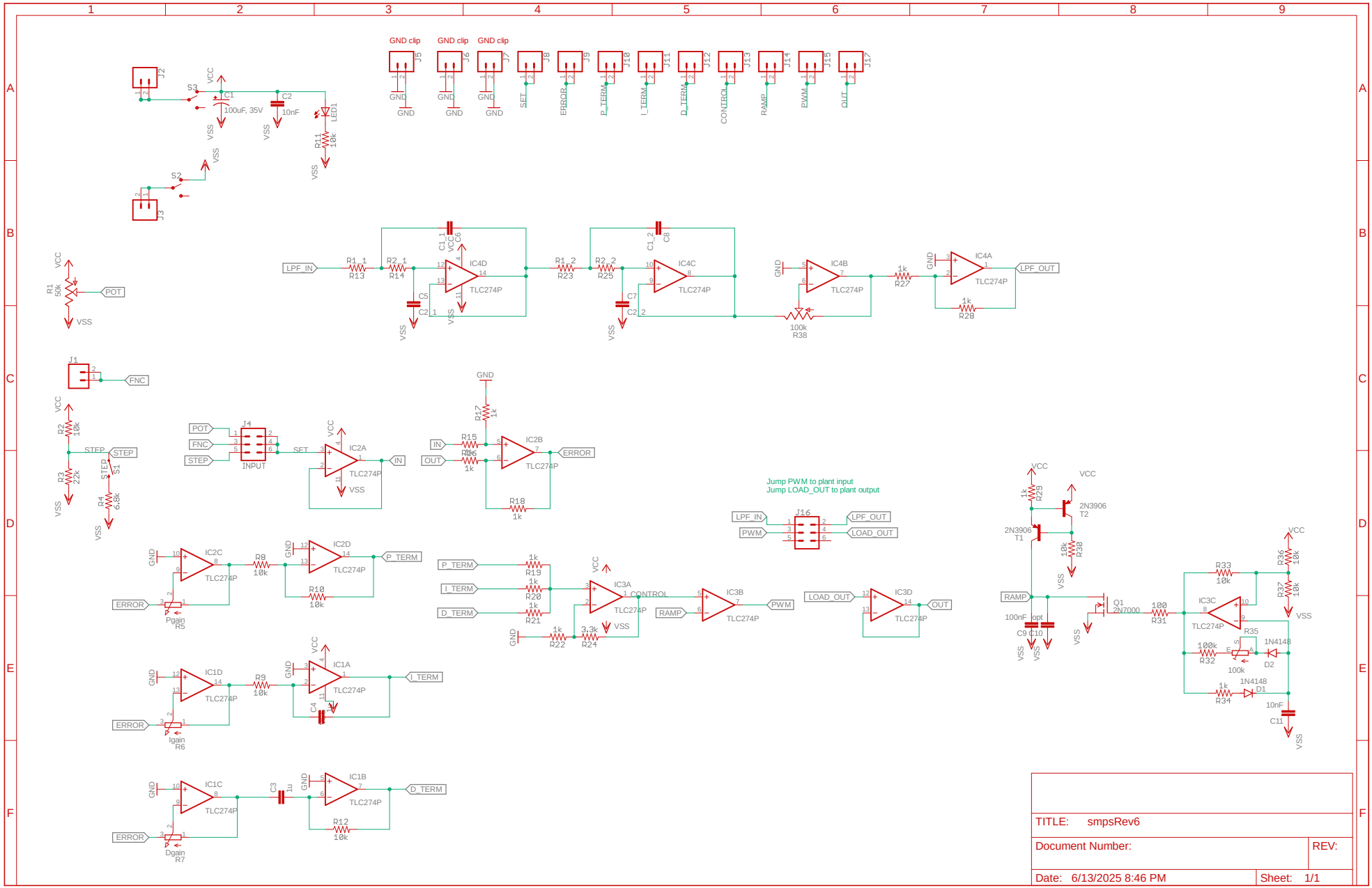
8) The plant, formed by the pair of opamp IC4D and IC4C in Figure 1, is a 4th order low pass filter (LPF) that converts the PWM output of the comparator into a DC signal whose voltage is proportional to the duty cycle over a -9V to +9V scale. The transfer function for IC4D is given by T1 and the transfer function for IC4C is given by T2.

$$T1(s) = \frac{66{,}840}{s^2 + 247s + 66{,}840} \qquad T2(s) = \frac{297{,}100}{s^2 + 97s + 297{,}100}$$

a. Use the following Mattab script to form the Bode Plot of the two stages of the low pass filter (LPF) in series.

```
% Make sure the control systems toolbox is installed
s = tf('s');
T1 =  66810/(s^2 + 247*s + 66810);
T2 = 297100/(s^2 + 97*s + 297100);
bode(T1*T2);          waitforbuttonpress;
nyquist(T1*T2);
```

b. What is the attenuation of the LPF at low frequencies – express your answer in decibels.
c. the -6dB corner frequency in Hz. Remember that the Matlab plots in radians/sec.
d. Using the information in the Bode plot, how does the LPF convert the PWM waveform into a DC value?
e. What role is opamp IC4B and R38 serving?
f. I put IC4A into the circuit to buffer the plant from the other circuit elements. What is the gain of this stage? What is the effect of this stage on the gain of the previous stage.
g. Use the information in the Nyquist plot, is the closed loop feedback system with gain = 1 (integral and derivative gains = 0) stable?



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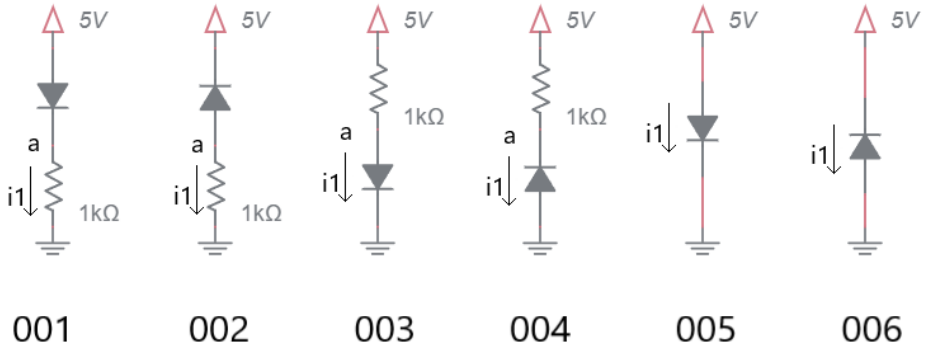
Chapter: Diode

DC circuits with diodes and resistors

Determine the currents and voltages in the following circuit. Assume a constant voltage drop model for the diodes with a cut-in voltage of 0.7V. If a diode is reverse biased write "RB" next to the diode.



001

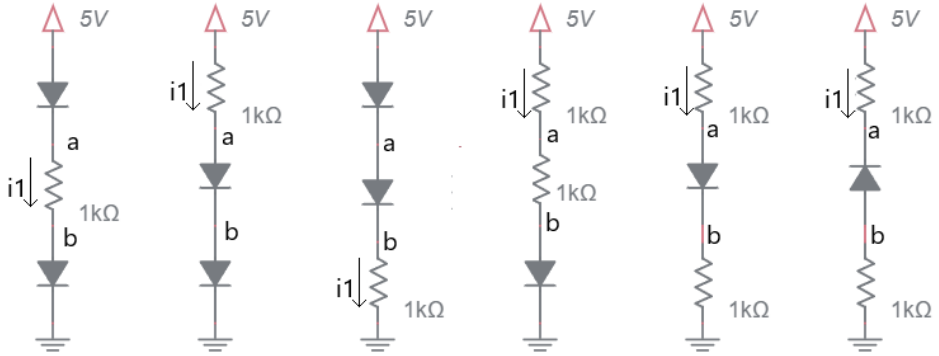
002

003

004

005

006



007

008

009

010

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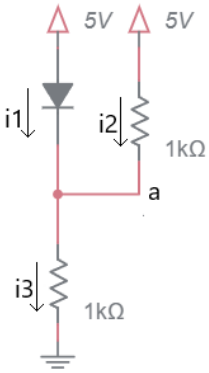

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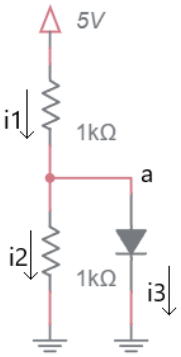
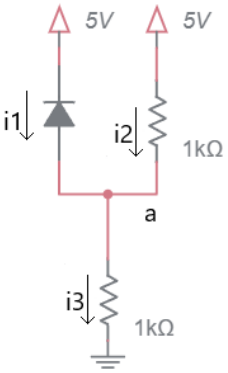
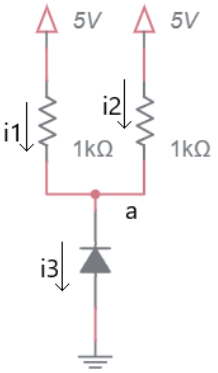


014



015

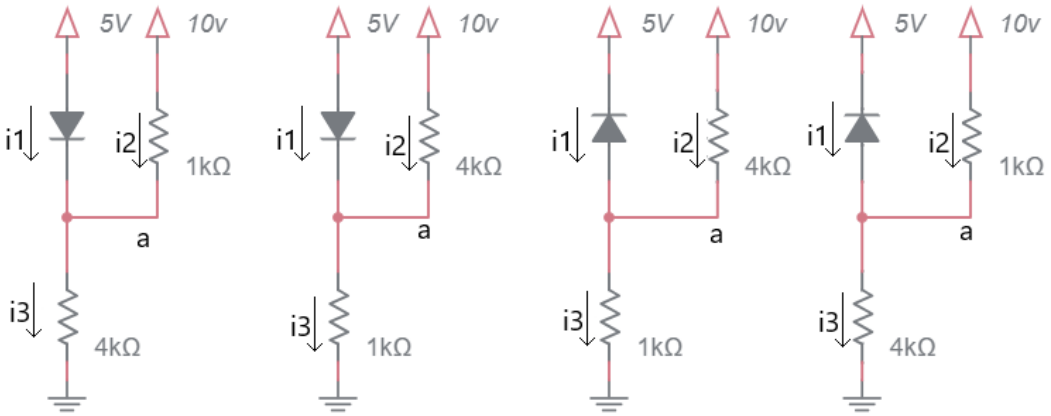


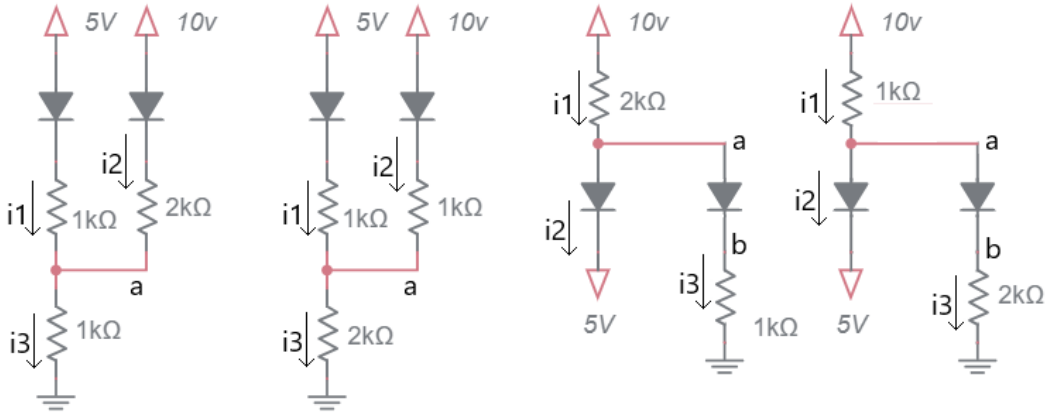
016

Problem	a	b	I1	I2	I3
001					
002					
003					
004					
005					
006					
007					
008					
009					
010					
011					
012					
013					
014					
015					
016					

DC circuits with diodes and resistors

Determine the currents and voltages in the following circuit. Assume a constant voltage drop model for the diodes with a cut-in voltage of 0.7V. **Note, the power rails are 5V and 10V to the circuits!**

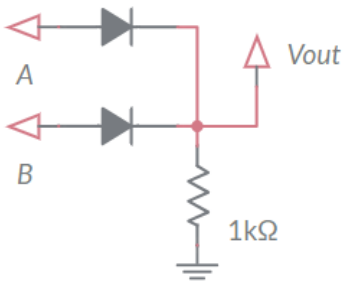




Problem	a	b	i1	i2	i3
001					
002					
003					
004					
005 superpos					
006					
007					
008					

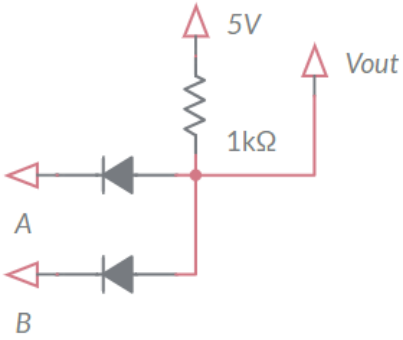
Diodes as logic gates

In the following circuits consider 5V logic 1 and GND as logic 0. Use the ideal diode model for analysis. Complete the truth table for the circuit shown and describe the logic function instantiated by each.



001

A	B	Vout
0	0	
0	1	
1	0	
1	1	

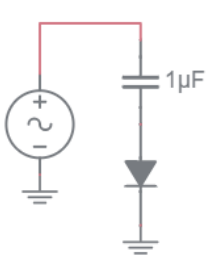


002

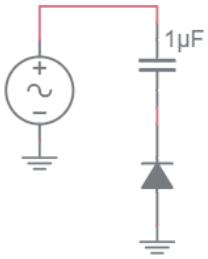
A	B	Vout
0	0	
0	1	
1	0	
1	1	

AC circuits with diodes and resistors

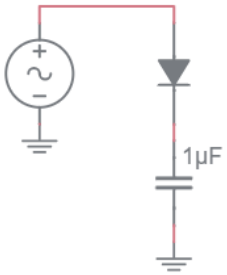
For each of the circuits below, complete the timing diagrams.



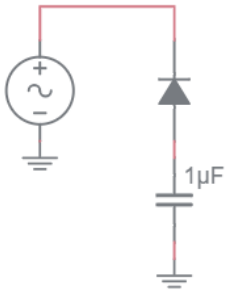
001



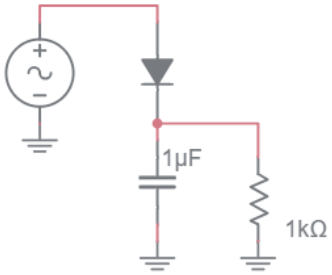
002



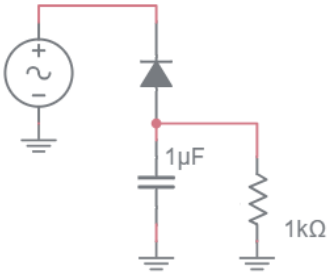
003



004



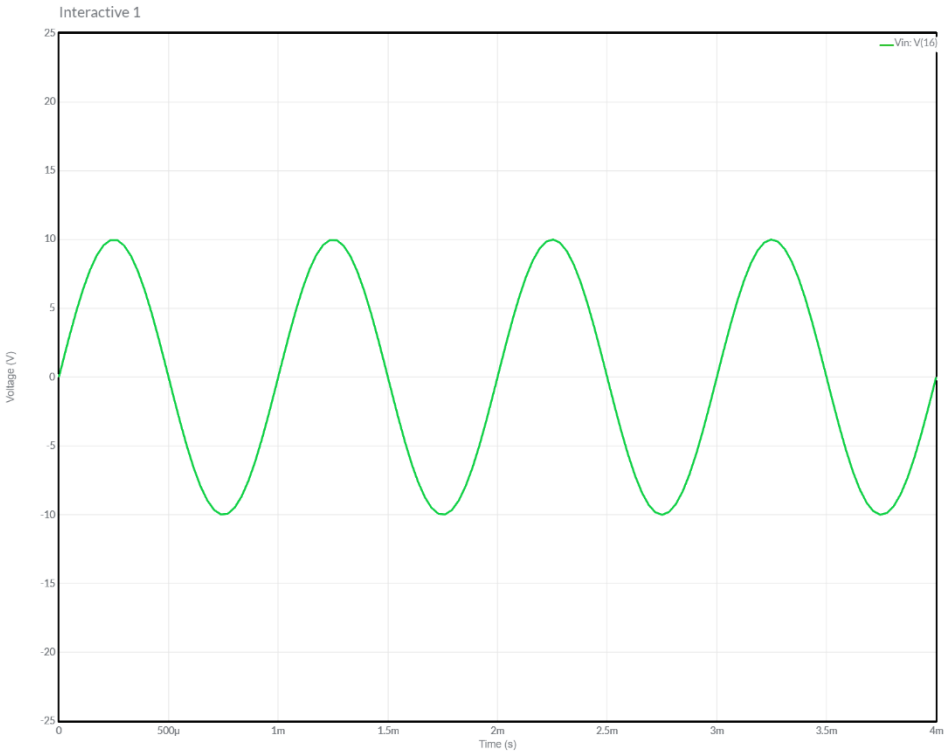
005



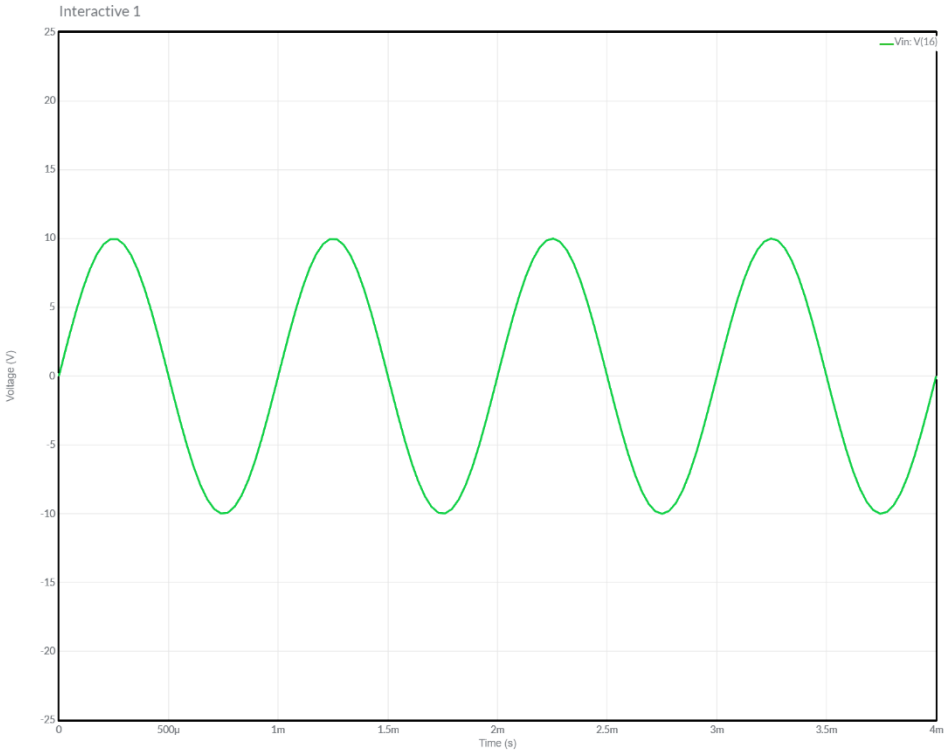
006

After you complete the timing diagrams for circuits 001 to 004, look at their behavior and assign the circuits one of the following names – one name for each circuit.

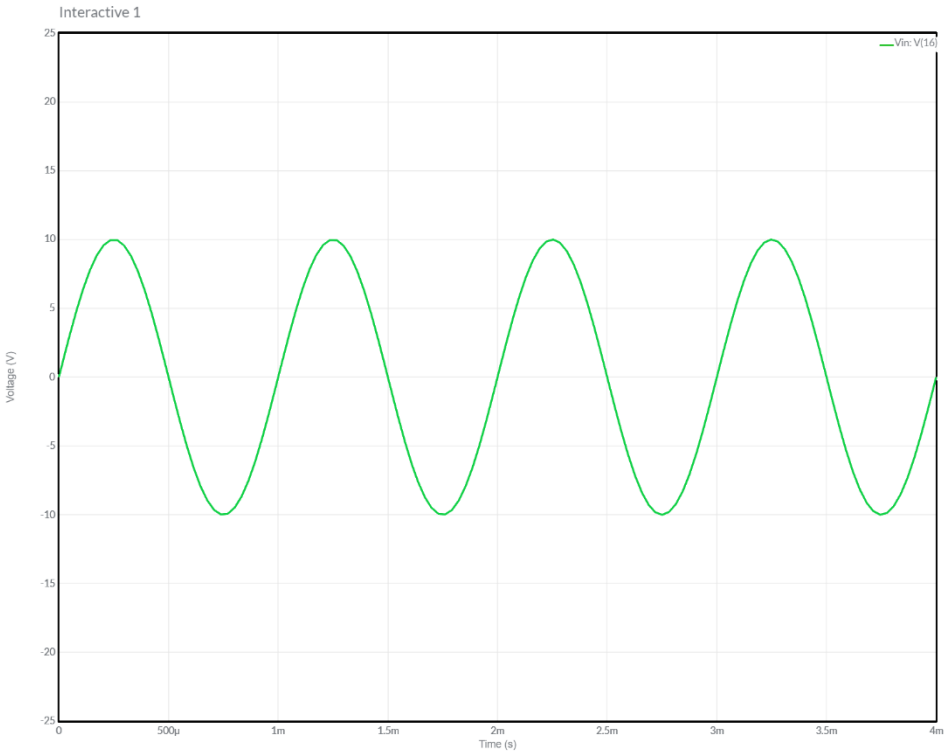
- Peak detector
- Positive level shifter
- Trough detector
- Negative level shifter



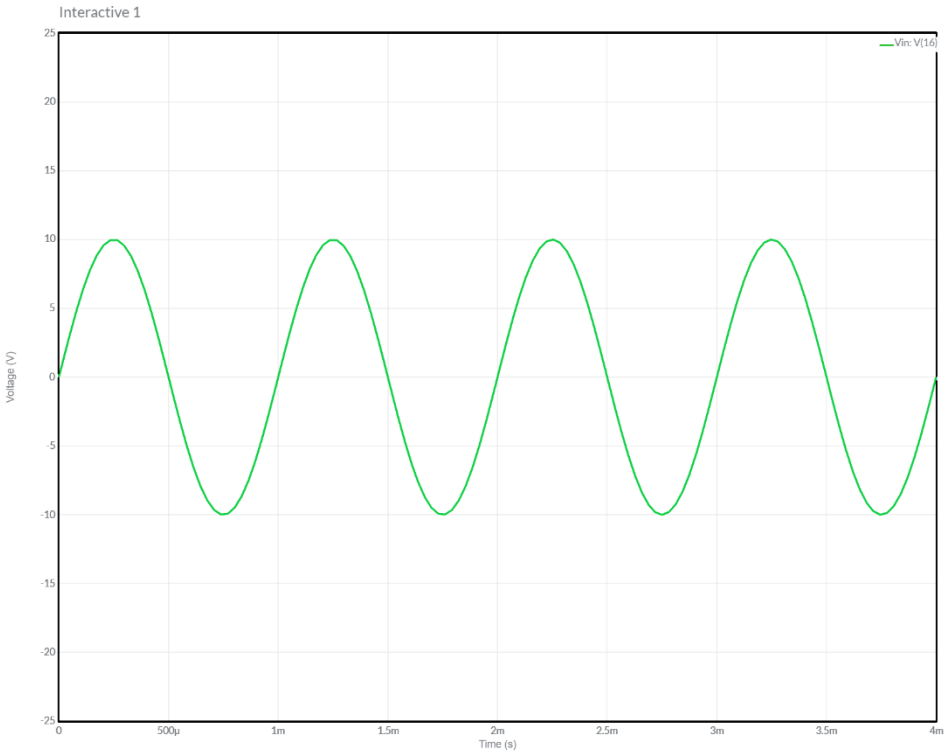
Plot the voltage and current for the circuit labeled 001.



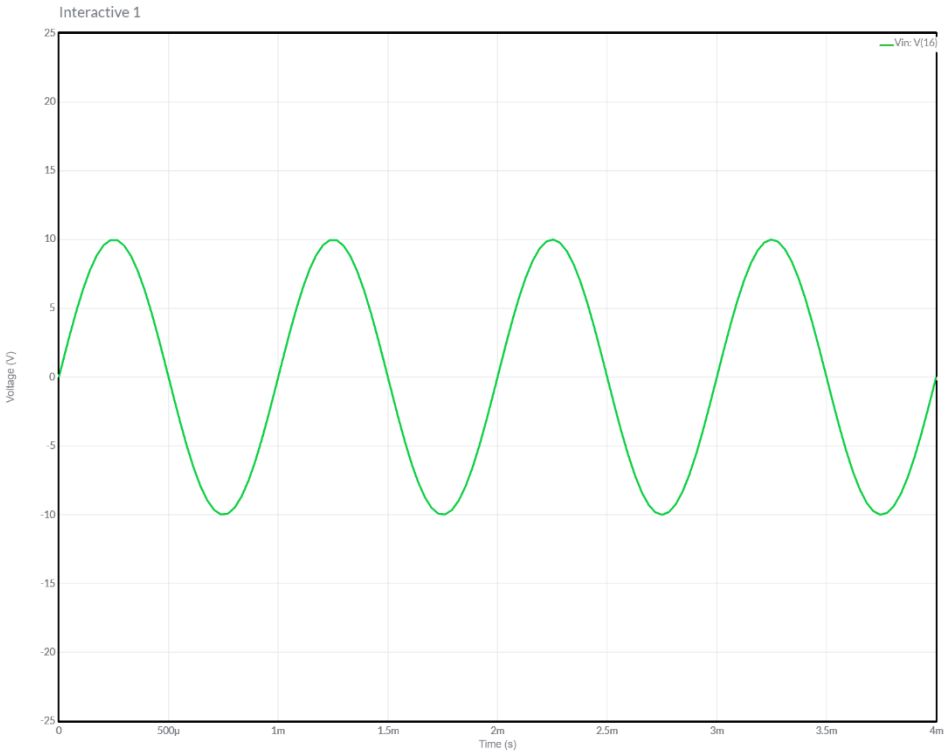
Plot the voltage and current for the circuit labeled 002.



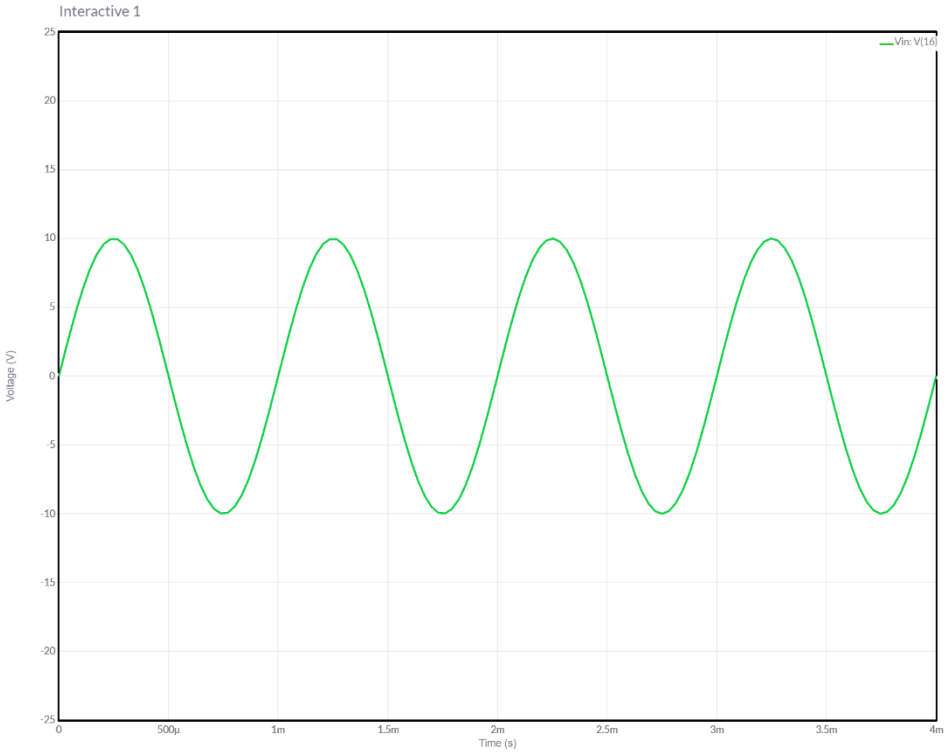
Plot the voltage and current for the circuit labeled 003.



Plot the voltage and current for the circuit labeled 004.



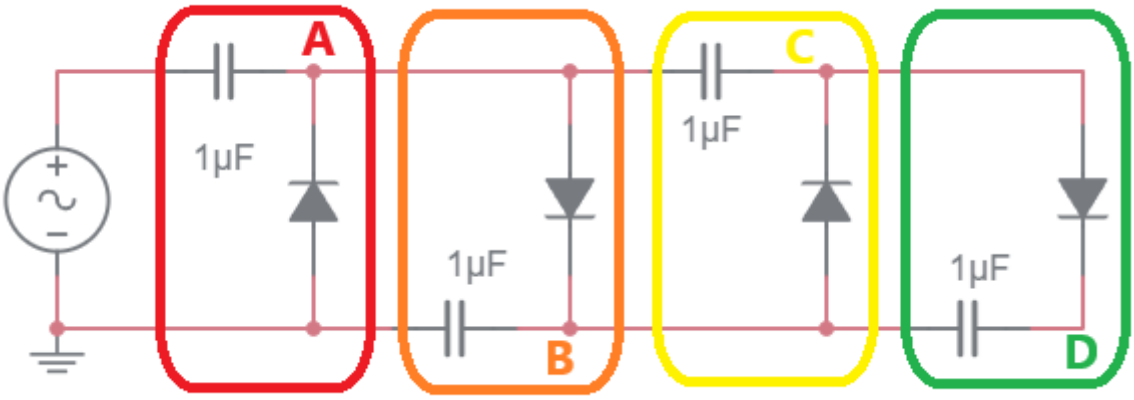
Plot the voltage and current for the circuit labeled 005.



Plot the voltage and current for the circuit labeled 006.

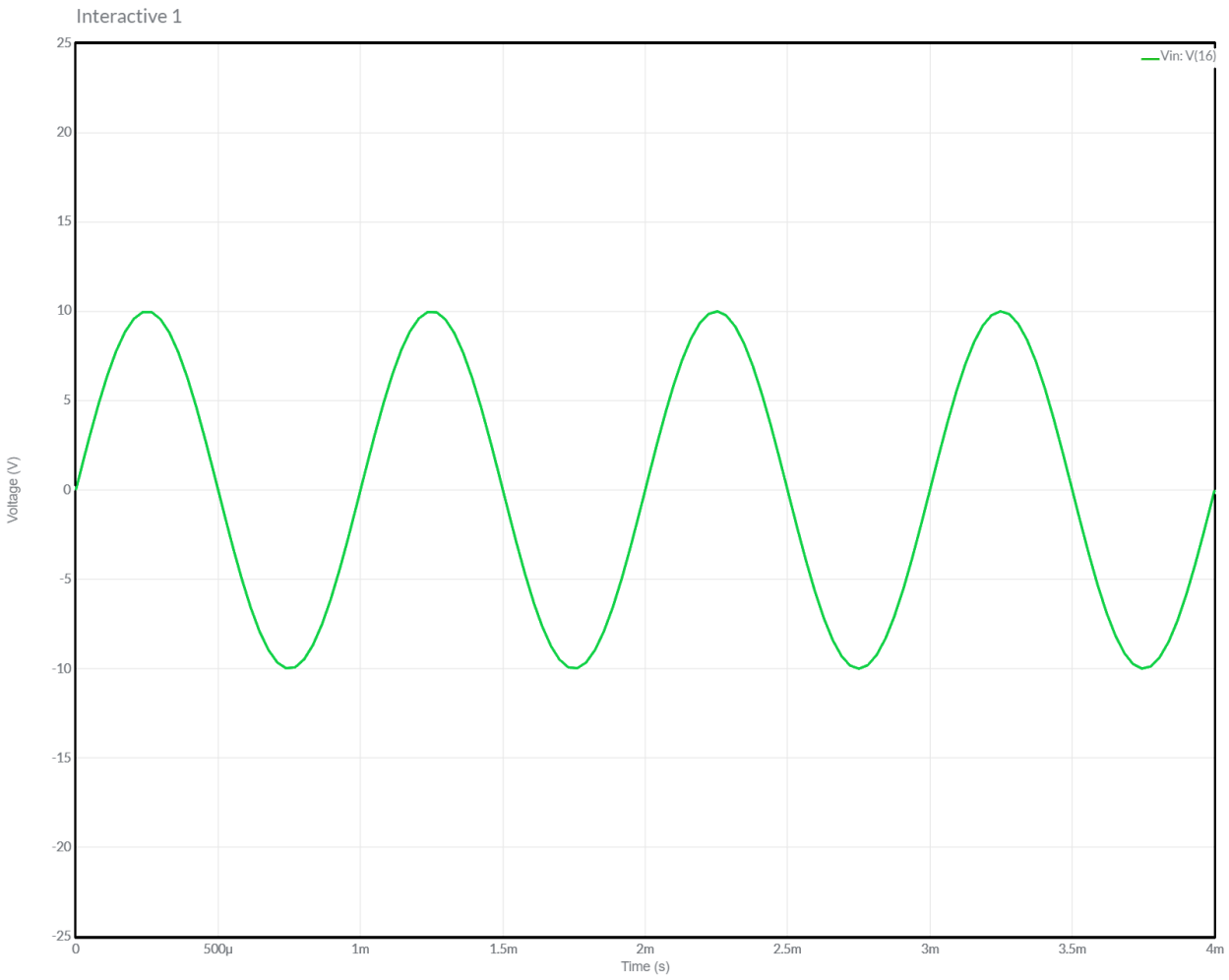
Practical Application – Voltage Doubler

The circuit below takes combinations of circuits from the **AC circuits with diodes and resistors** section and combines them to produce a larger voltage than the input voltage. Before starting on this analysis, you must first have successfully completed all the problems in the **AC circuits with diodes and resistors** section.



1. Look at the circuit outlined in red and compare it to circuits 001 to 004 in the **AC circuits with diodes and resistors** section. Which circuit is it and what name did you assign it?
   Circuit 002 is the positive level shifter
2. The circuit outlined in orange gets it input from A. Look at the circuit outlined in orange and compare it to circuits 001 to 004 in the **AC circuits with diodes and resistors** section. Which circuit is it and what name did you assign it?
   Circuit 003 is the peak detector.
3. The circuit outlined in yellow gets it input from A and its ground terminal is connected to B. Look at the circuit outlined in yellow and compare it to circuits 001 to 004 in the **AC circuits with diodes and resistors** section. Which circuit is it and what name did you assign it?
   Circuit 002 is the peak detector.
4. The circuit outlined in green gets it input from C and its ground terminal is connected to B. Look at the circuit outlined in green and compare it to circuits 001 to 004 in the **AC circuits with diodes and resistors** section. Which circuit is it and what name did you assign it?
   Circuit 003 is the peak detector.

Use this information to plot the output of each colored stage given the input shown.


Interactive 1
Vin: V(16)
25
20
15
10
5
0
-5
-10
-15
-20
-25
Voltage (V)
0
500µ
1m
1.5m
2m
2.5m
3m
3.5m
4m
Time (s)

Practical Application – I/V Curve for LED

You are required to illuminate a Cree Xlamp XM-L2 High Power LED using either a current source or voltage source, the choice is yours. The LED has a I vs. V curve is shown in Figure 2. You are tasked to operate the LED at 3V and 1.3A – the point in the middle of the curve.

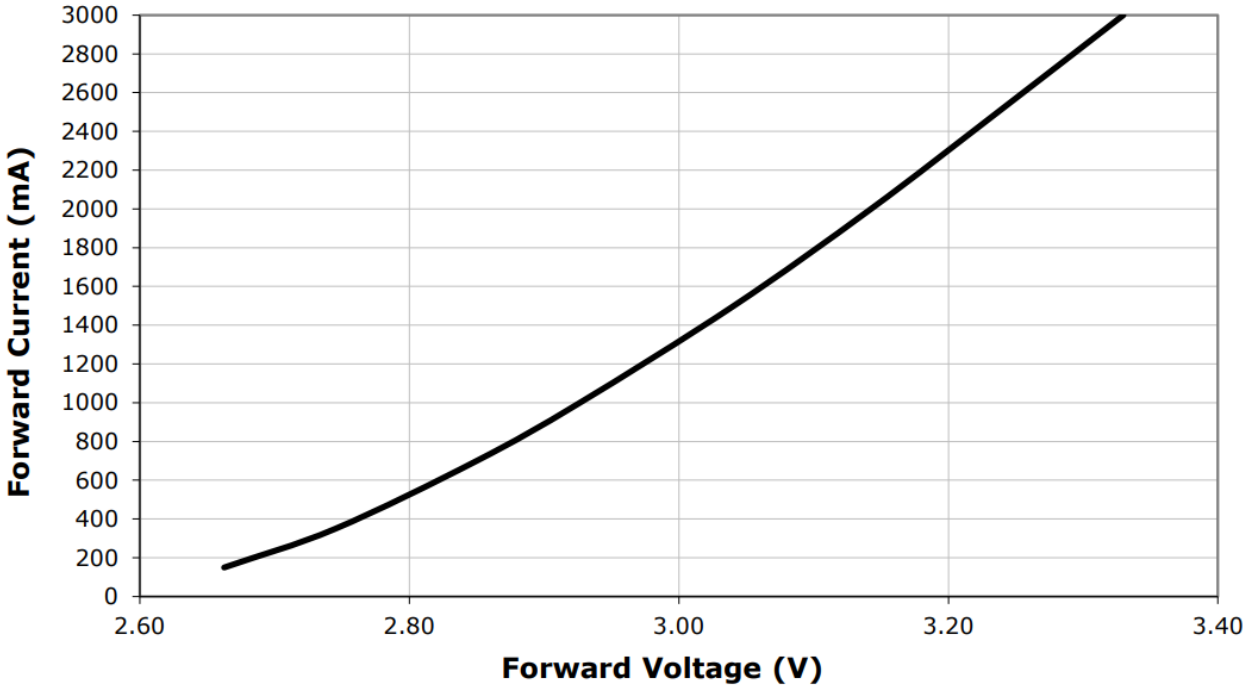


Figure 2: I/V curve for a Cree Xlamp XM-L2 High Power LED.

If you use a voltage source, you will have a ±10% variation in voltage.

a. What is the range of voltages across the LED?
b. Using the I/V curve in Figure 2, what is the range of current through the LED?
c. What is the range of power dissipated by the LED voltage source?

If you use the current source, you will have a ±10% variation in current.

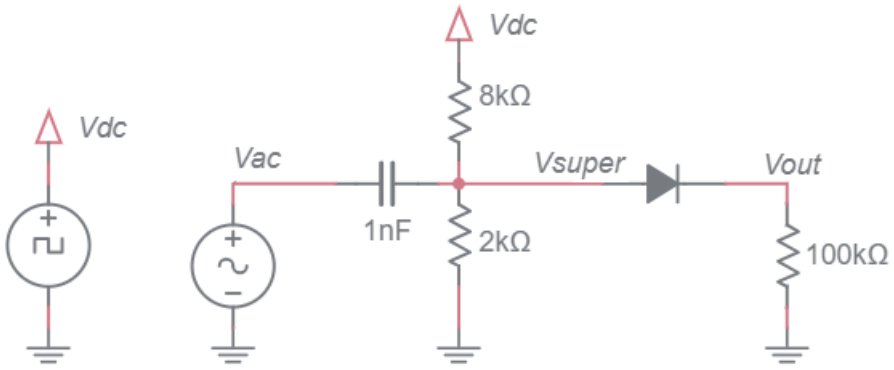
a. What is the range of current through the LED?
b. Using the I/V curve in Figure 1, what is the range of voltage across the LED?
c. What is the range of power dissipated by the LED using the current source?

What supply (voltage and current) produces the least variation in power?

What characteristic of the I/V curve determines the sensitivity to changes in voltage or current?

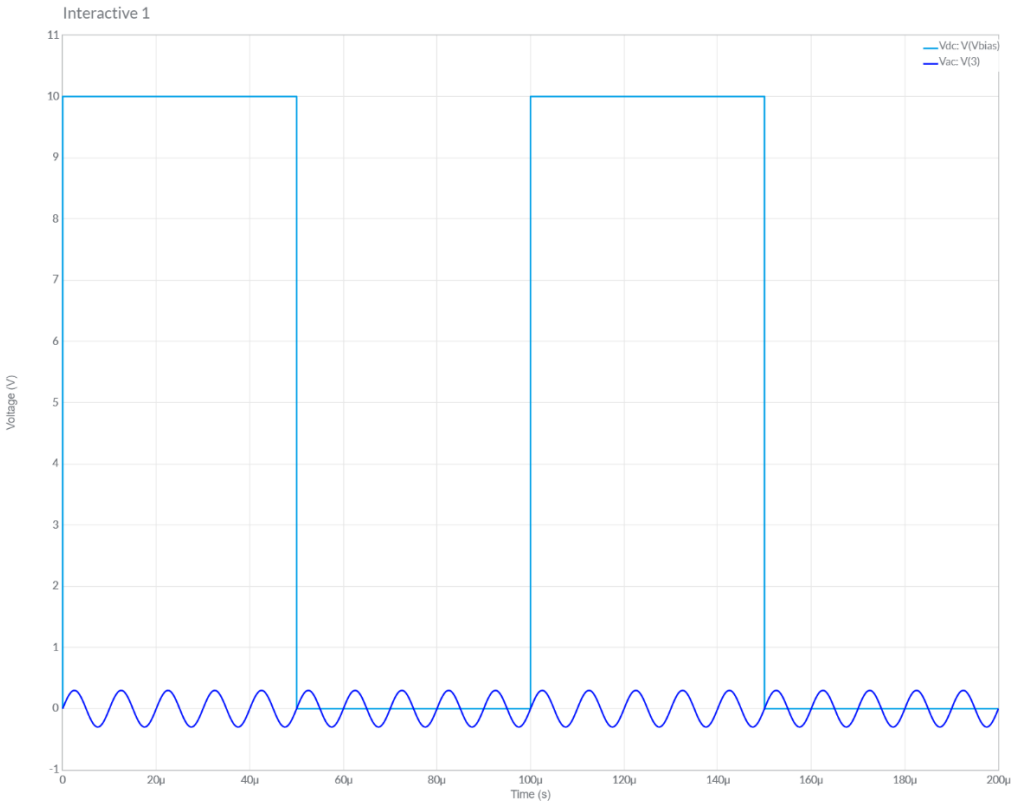
Practical Application – Using diodes as a switch

The following circuit shows how you can use a diode to switch a (small) AC signal on or off.



Your first task is to determine the signal *Vsuper* from the *Vac* and *Vdc* signals. To do this ignore the diode and 100kΩ resistor and use superposition. Note that the *Vdc* signal is a square wave that alternates between 0V and 10V at 10kHz (see graph below). If you are having a problem with this open the workbook to the Review section and find the **Practical Application – Coupling AC signal on a DC bias** section.

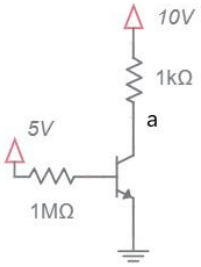
Now compute the *Vout* by running the *Vsuper* signal through a diode modeled as a constant voltage drop. You should see that when the *Vdc* signal is at 10V the AC signal passes through to *Vout*. When the *Vdc* signal is at 0V, *Vout* = 0V.



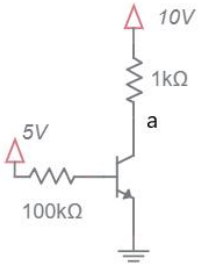
Chapter BJT @ DC

DC circuits with NPN BJTs and resistors

Determine the voltage at labeled nodes and determine ic, ib and ie in the following circuit. If the BJT is in the active region, assume ß = 100 and ic=ie. If the BJT is in saturation, assume that Vce = 0.2V. Only compute ß when the BJT is in saturation. Round you answer to 2-significant figures and include units. If the circuit does not have the variable asked for in the table, leave that entry blank



001



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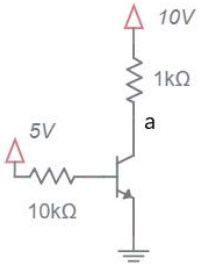

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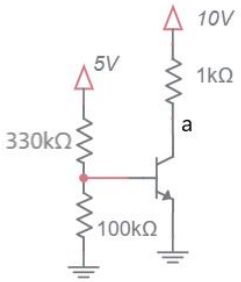

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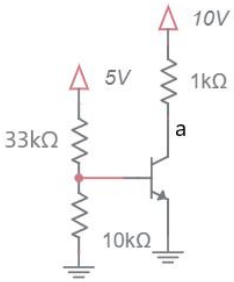
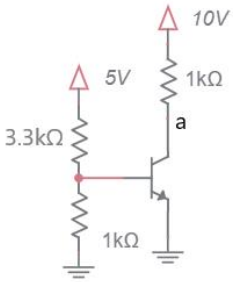
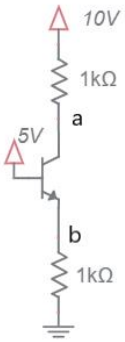


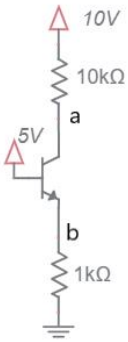
005



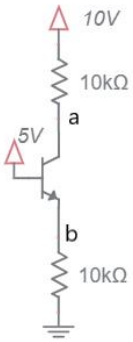
006



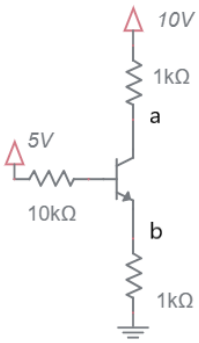
007



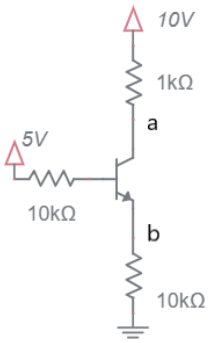
008



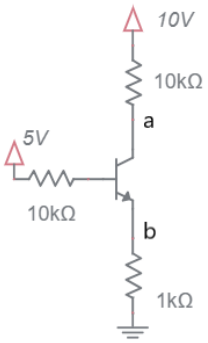
009



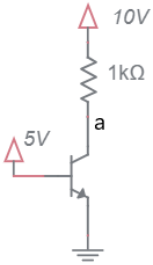
010



011



012



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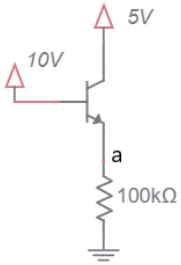

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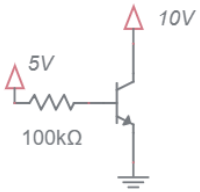
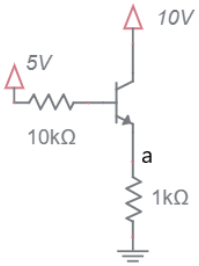
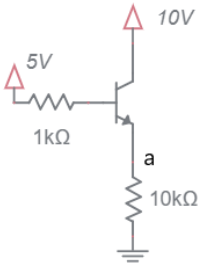


015



016

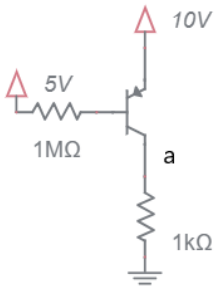


017

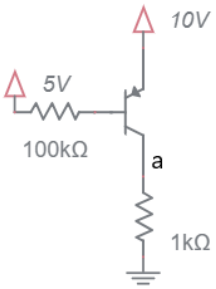
Problem	a	b	ic	ib	ie	ß
001						
002						
003						
004						
005						
006						
007						
008						
009						
010						
011						
012						
013						
014						
015						
016						
017						

DC circuits with PNP BJTs and resistors

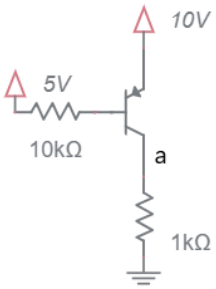
Determine the voltage at labeled nodes and determine ic, ib and ie in the following circuit. If the BJT is in the active region, assume ß = 100 and ic=ie. If the BJT is in saturation, assume that Vce = 0.2V. Only compute ß when the BJT is in saturation. Round you answer to 2-significant figures and include units. If the circuit does not have the variable asked for in the table, leave that entry blank



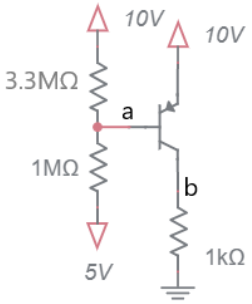
001



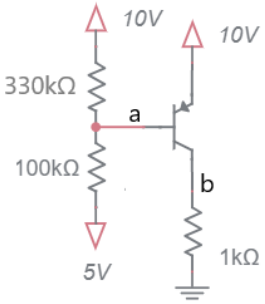
002



003



004



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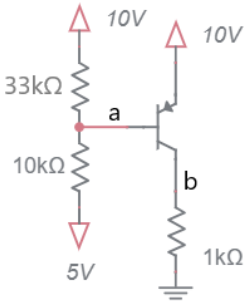

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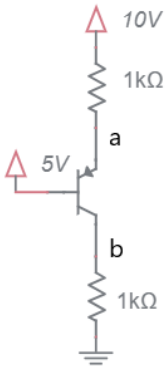

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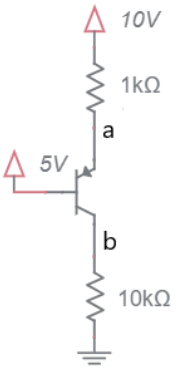

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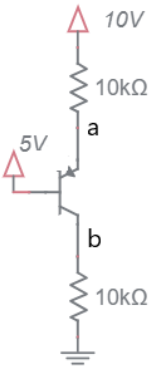

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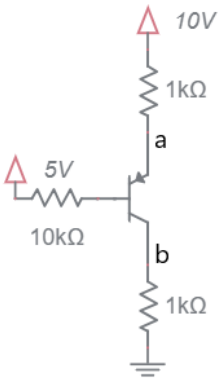
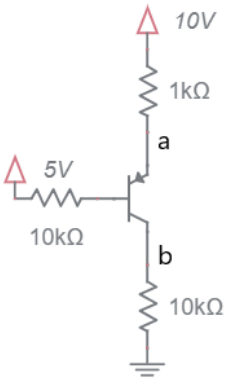
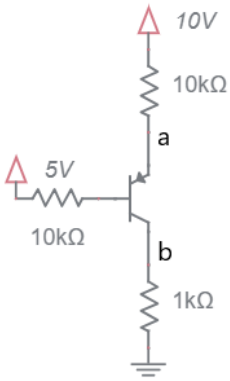


010



011



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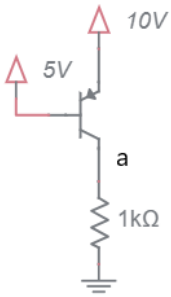

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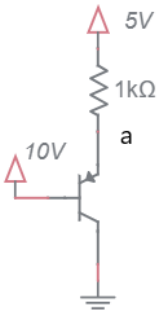

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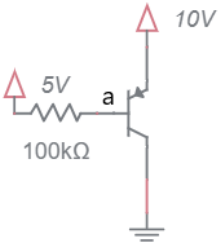
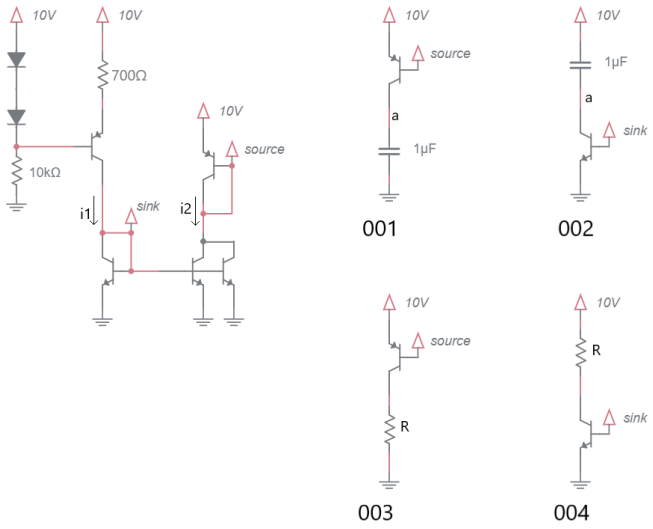


015

Problem	a	b	ic	ib	ie	ß
001						
002						
003						
004						
005						
006						
007						
008						
009						
010						
011						
012						
013						
014						
015						

BJT Current Sources and mirrors



1. Determine the currents i1 and i2.
2. What is the range of resistance in the circuits 003 and 004 to keep their BJTs in the active region?
3. Plot the volage at point a in circuits 001 and 002 assuming the capacitor is discharge at time 0. You can use the following questions to help.
    a. Use the voltage/current equation for a capacitor to determine dv/dt for the capacitor.
    b. The initial voltage drop across the capacitors is 0V. What is the voltage at point a?
    c. The final voltage drop across the capacitors is 10V. What is the voltage at point a?

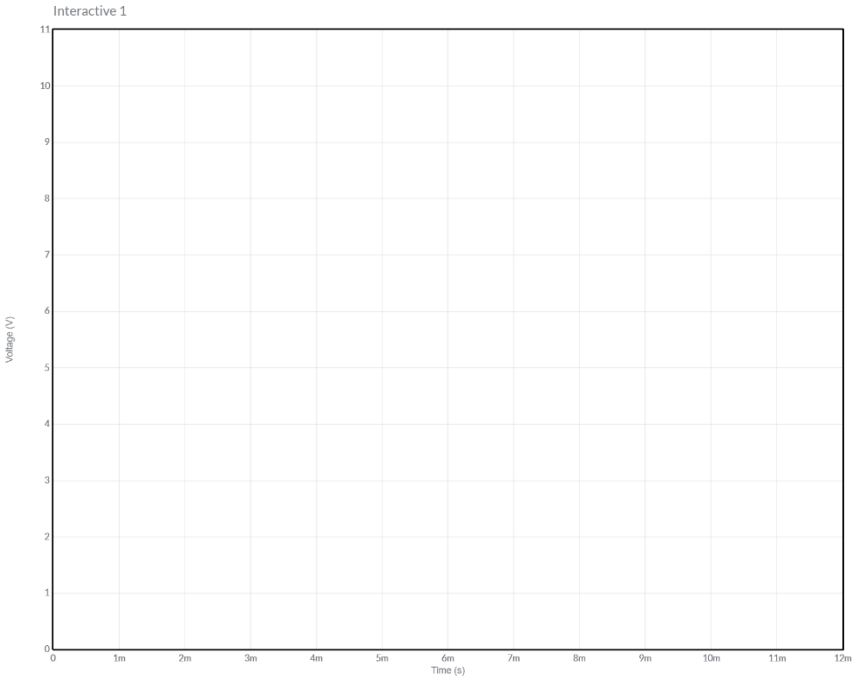


*Figure 3: Plot the voltage at node **a** for the circuits shown in 001 and 002*

Practical Application – Power dissipated by BJT

You are required to illuminate a Cree Xlamp XM-L2 High Power LED using a current source. The LED has a I vs. V curve is shown at left in Figure 2. Your current source, shown at right in Figure 2, uses a TIP31 (a high powered NPN transistor) and a 2.7V Zener diode. You need to run the LED at 2 amps.

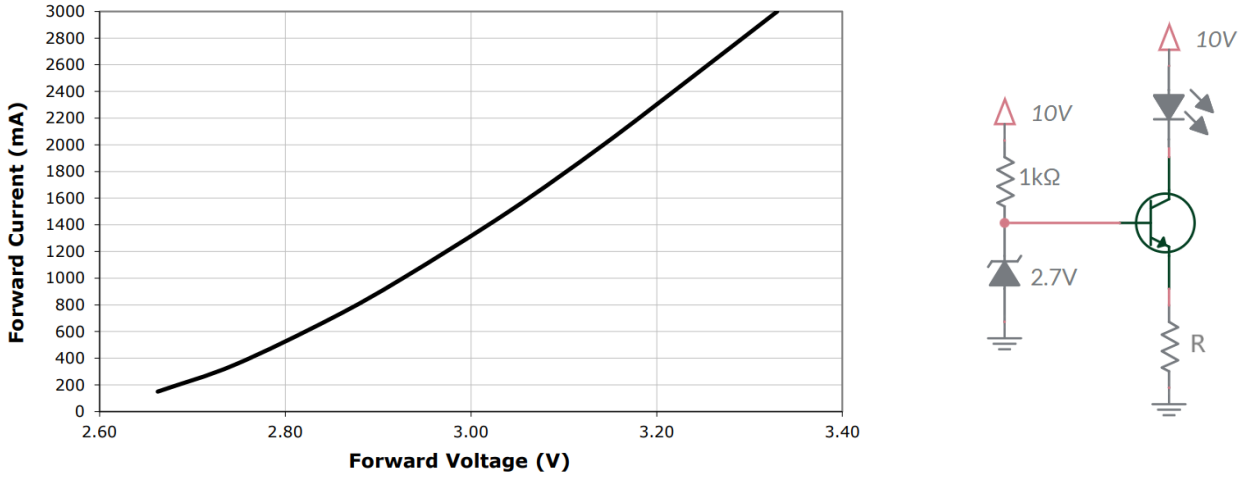


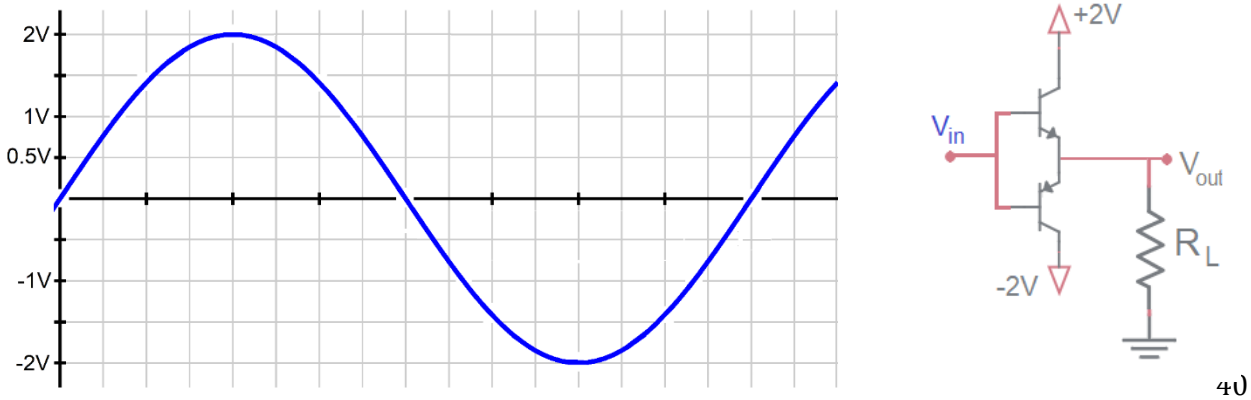
Figure 4: (Left) I/V curve for a Cree Xlamp XM-L2 High Power LED. (Right) The constant current source used to drive the LED.

a. What is the emitter voltage?
b. What value of emitter resistor, R, will produce the needed 2A through the LED?
c. What is the voltage drop across the LED at 2A?
d. What is the power dissipated by the LED at 2A?
e. What is the power dissipated by the resistor R at 2A?
f. What is the voltage across the BJT at 2A?
g. What is the power dissipated by the BJT at 2A?

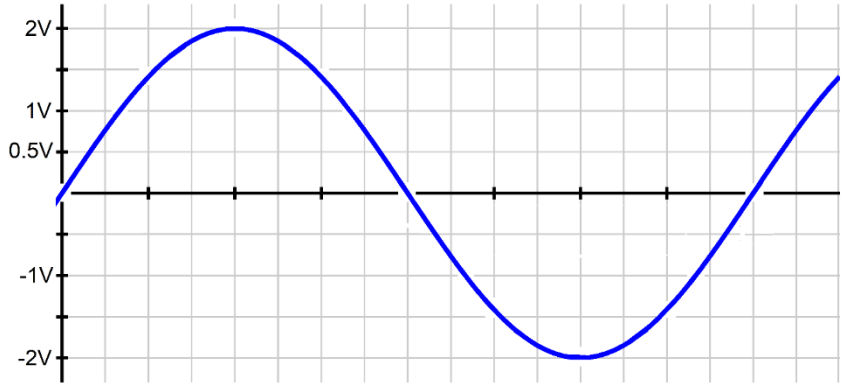
How can you reduce the power dissipation of the BJT while keeping 2A running through the LED? Do not change the circuit topology.

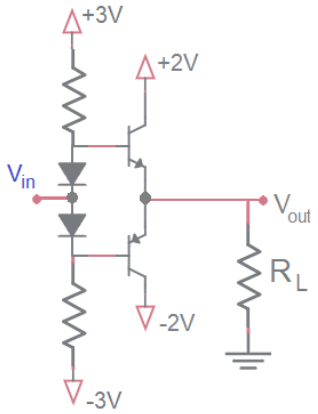
Practical Application - Cross Over Distortion

The blue sine wave shown in the graph below is applied as the input, V_{in}, to the circuit shown below at right. Determine the output, V_{out}, and graph it on the graph below. The value of the load resistor, R_L is unimportant.

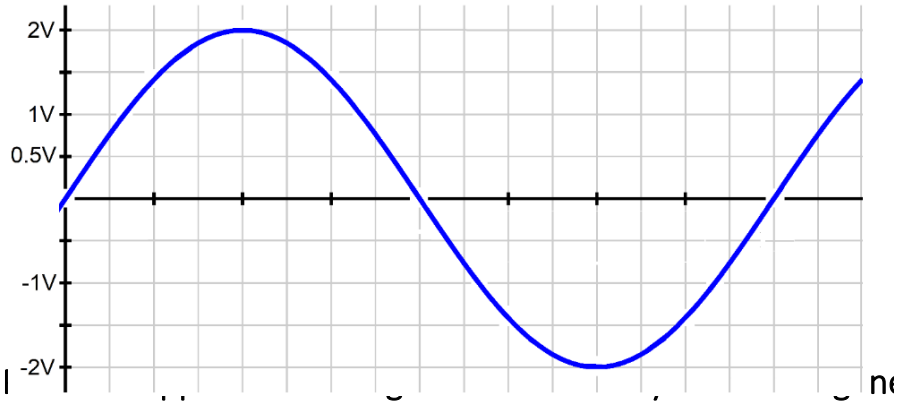


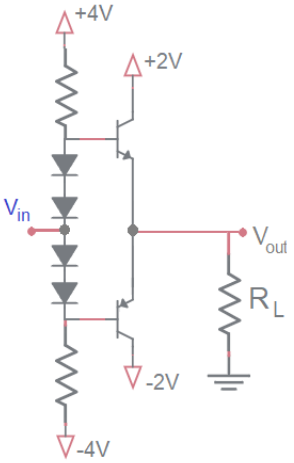
The blue sine wave shown in the graph below is applied as the input, V_{in}, to the circuit shown below at right. Determine the output, V_{out}, and graph it on the graph below. The value of the resistors are unimportant.





The blue sine wave shown in the graph below is applied as the input, V_{in}, to the circuit shown below at right. Determine the output, V_{out}, and graph it on the graph below. The value of the resistors are unimportant.

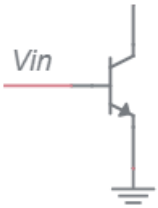




In the Ebers-Moll equation of a BJTs the collector current is described as

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

The I_S term, the reverse saturation current, is strongly temperature dependent. According to multiple sources, it doubles for every 10°C rise in temperature. This dependency can lead to thermal runaway in the common emitter circuit show at right. In the following questions assume that Vin is constant and that the BJT is operating in the active region.

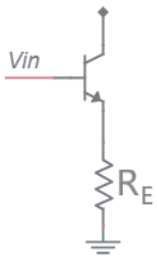


1. Look at the schematic at right, does the base emitter voltage depend on the collector current?
2. If the temperature of the BJT increases, does I_s increase or decrease?

3. If I_S increases, does I_C increase or decrease?
4. If I_C increases does the power dissipated by the BJT increase or decrease? Assume V_C is constant.
5. If the power dissipated by the BJT increases, does the temperature of the BJT increase or decrease?

From these inferences you should see that an increase in the BJT's temperature causes further increase in the temperature of the BJT – thermal runaway. This is an example of positive feedback – a tendency of a system to increase a parameter without bound. While you may like positive feedback, electrical systems can do bad things when they have too much positive feedback.

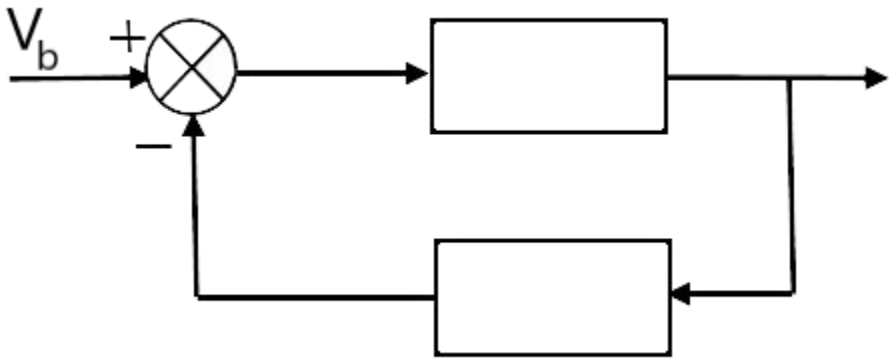
Now consider the circuit shown at right. This is a common emitter with emitter degeneration resistor. As we will see, the addition of a resistor to the emitter adds negative feedback which greatly decreases the tendency of the BJT to experience thermal runaway. In the following questions assume that Vin is constant and that the BJT is operating in the active region.



1. Look at the schematic at right. Does the base emitter voltage increase or decrease when the emitter current increases?
2. When the collector current increase, does the emitter current increase or decrease?
3. If the temperature of the BJT increases, does I_s increase or decrease?
4. If I_S increases, does I_C increase or decrease?
5. If I_C increases, does I_E increase or decrease?
6. If I_E increases, does V_E increase or decrease?
7. If V_E increases, does V_{BE} increase or decrease?
8. If V_{BE} decreases, does I_C increase or decrease?
9. If I_C decreases, does the power dissipated by the BJT increase or decrease?
10. If the power dissipated by the BJT decreases, does the temperature of the BJT increase or decrease?

The ability of the deceasing V_{BE} being able to keep the increasing I_S in check depends on the magnitude of the emitter resistor. If it the emitter resistor is too small, then the BJT may still exhibit thermal runaway. In that case, you should increase the emitter resistor until thermal runaway is kept in check.

Now, let's see if you can make a feedback diagram to describe this negative feedback using the diagram below.

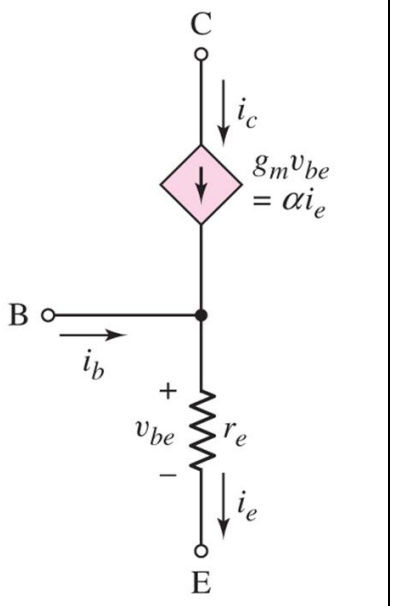
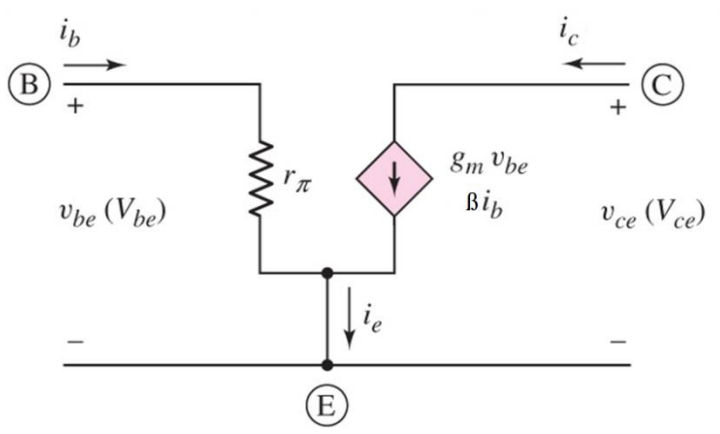


1. Make the reference input equal to V_b
2. What must the inverting input to the summer junction be for the output of the summer junction to be V_{be}? Write this signal and V_{be} on the diagram.
3. Fill in the upper block with the RHS of the Ebers-Moll equation.
4. Label the output of the block diagram with the LHS of the Ebers-Moll equation. This should make sense because the Ebers-Moll equation is a bunch of constants with two variables.
5. Fill in the lower block with an equation which converts the block diagram output into the variable used in the inverting input to the summer junction. Hint, its Ohm's law.

This block diagram shows the If I_S variable on the forward path and the R_E variable on the backward path. The interplay between these two determines the thermal stability of the common emitter with emitter degeneration resistor circuit.

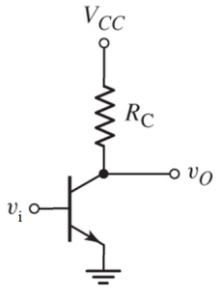
Chapter: BJT @ AC

Variable	g_m	r_π	r_e	r_o
Equation				
Typical value				

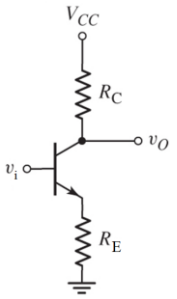
T model	Hybrid Pi model
	

Element	DC Model	AC Model
Resistor	R	R
Capacitor	Open	C
Inductor	L	Short
Diode	0.7V drop	$R_d = V_t/I_D$
Indep. Voltage Source	V	Short
Indep. Current Source	I	Open
BJT	Diode/Current Src	Pi or T model

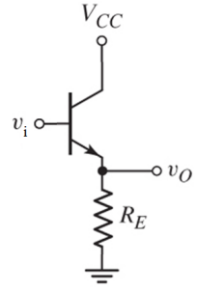
Common Emitter

	Input resistance	
	Output resistance	
	Gain	

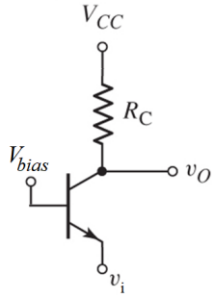
Common Emitter with degeneration resistor

	Input resistance	
	Output resistance	
	Gain	

Common Collector

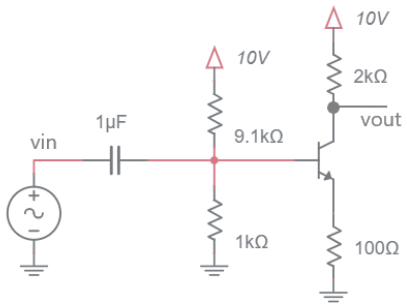
	Input resistance	
	Output resistance	
	Gain	

Common Base

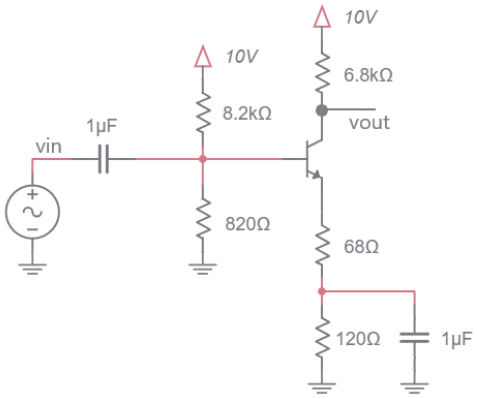
	Input resistance	
	Output resistance	
	Gain	

Small signal analysis of BJT circuits

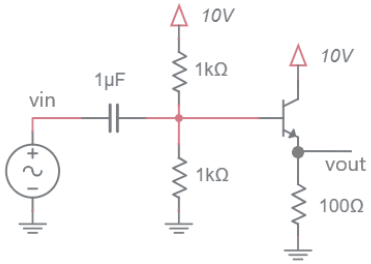
Complete the following table for these circuits. Assume infinite Early voltage.



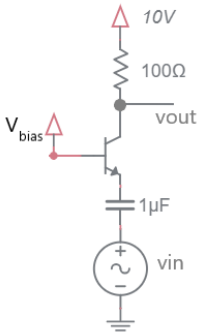
001



002



003

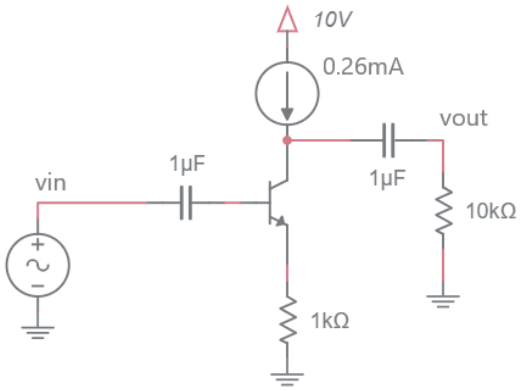


004

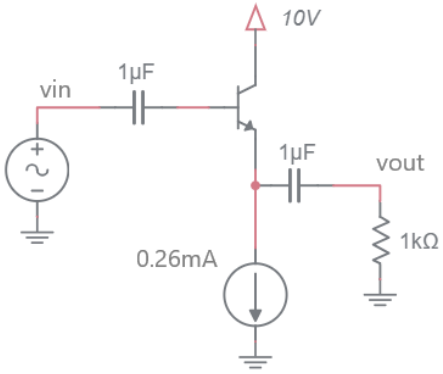
Circuit	I_C	V_{OUT}	g_m	r_e	A_V
001					
002					
003					
004					

Small signal analysis of BJT circuits

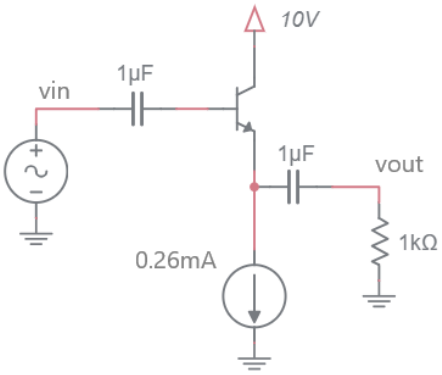
Complete the following table for these circuits. Assume infinite Early voltage.



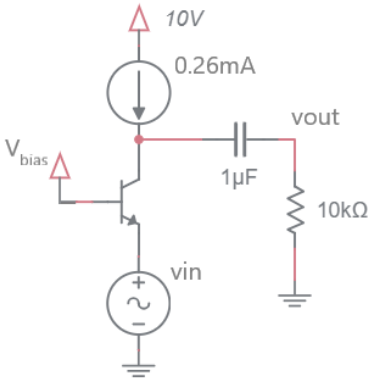
001



002



003

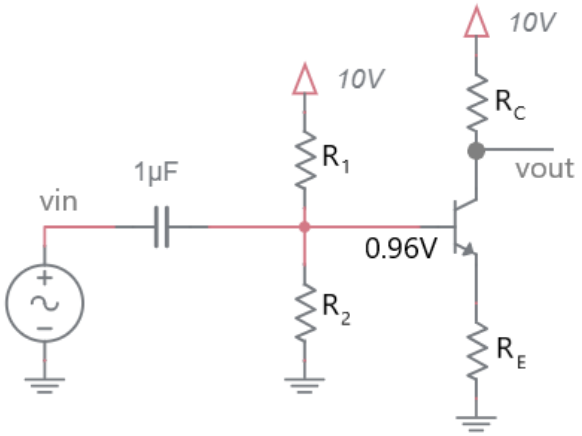


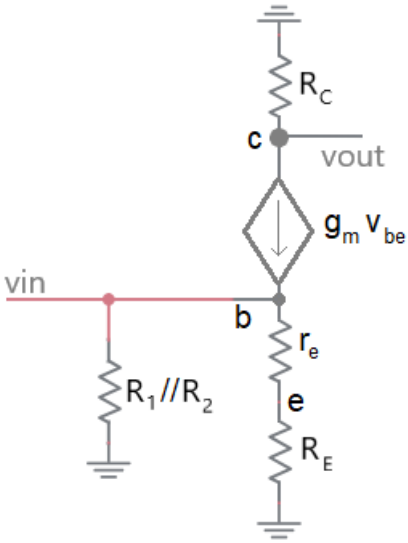
004

Circuit	I_C	V_{OUT}	g_m	r_e	A_V
001					
002					
003					
004					

Small signal analysis of BJT circuits

Let's explore the range of AC gain that you can achieve with the following circuit. The values of R1 and R2 have been selected so that the base of the BJT is DC biased to 0.96V – you do not need to compute the resistors values needed to make this happen.





Step 1: Describe I_C in terms of R_E

Step 2: Describe V_{OUT} in terms of R_E and R_C

Step 3: Describe g_m and r_e in terms of R_E

Step 4: Build a small signal model for the circuit

Step 5: Describe the small signal gain in terms of R_E and R_C

Step 6: Describe V_{OUT} in terms of A_v

Step 7: Find the maximum gain before the BJT saturates

Chapter: Frequency Domain

Apply definitions of decibels and decades

1. (vin/vout to dB) If an electronic component takes a 1.0v sine wave as input and output a 0.1v sine wave, how much attenuation would it have?

2. (vin/dB to vout) If you input a 2.4 V sin wave into a circuit that attenuated it by -32dB, what would the amplitude of the output waveform be?

3. (out/dB to vin) A circuit attenuates an input signal by -68 dB to produce a 0.5 V signal. What is the amplitude of the input signal?

4. (fhi/flo to decades) How many decades separate 10kHz and 30kHz?

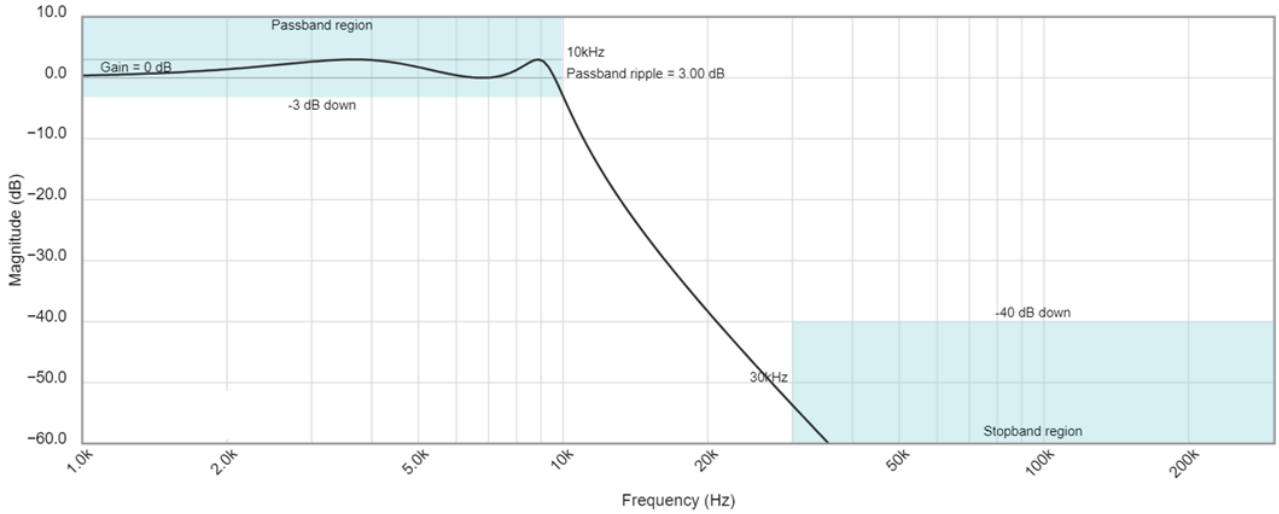
5. (fhi/decades to flo) What frequency is 1.5 decades below 300kHz?

6. (flo/decades to fhi) What frequency is 1.5 decades above 10kHz?

Interpret a Bode plot

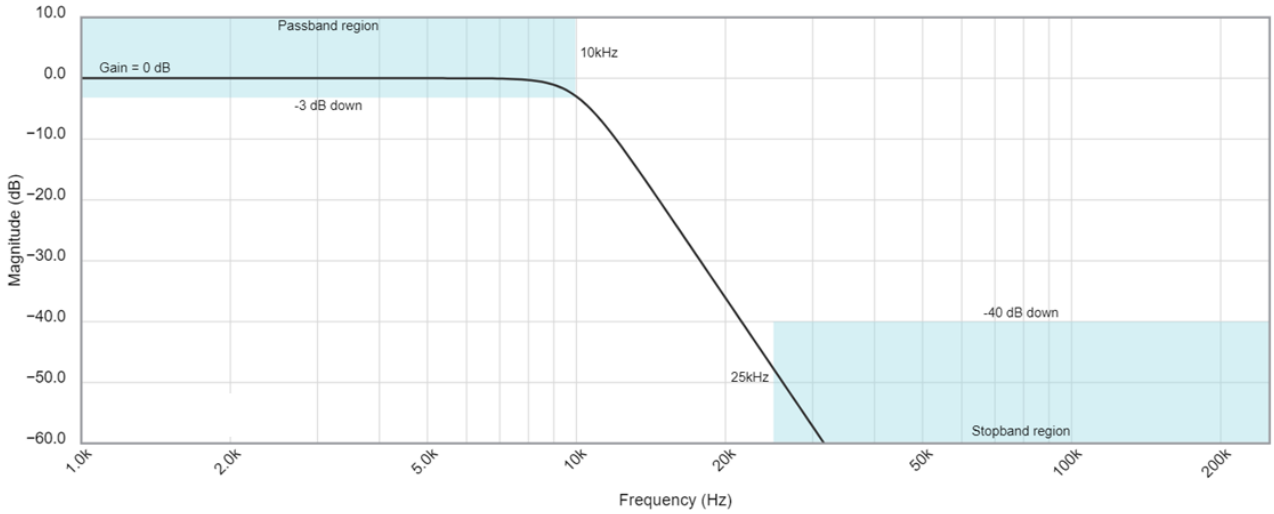
The following (magnitude) Bode plots were created using the Analog Devices filter wizard at tools.analog.com/en/filterwizard

The following Bode plot is from a 4th order Chebyshev low pass filter (note the ripple in the pass band) with corner frequency of 10kHz. Use the information in the Bode plot to answer the following questions.

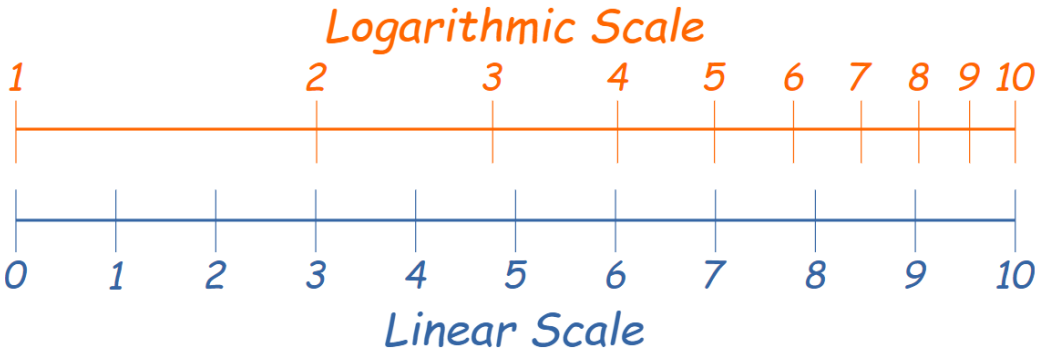


7. If you apply a 20kHz sin wave to this filter, how much attenuation will the output experience?
8. You want -45dB of attenuation, what frequency sin wave should you apply?
9. Estimate the slope of the magnitude in the stop band and use this to estimate the order of the filter. Hint, use the corner frequency as one of your points.

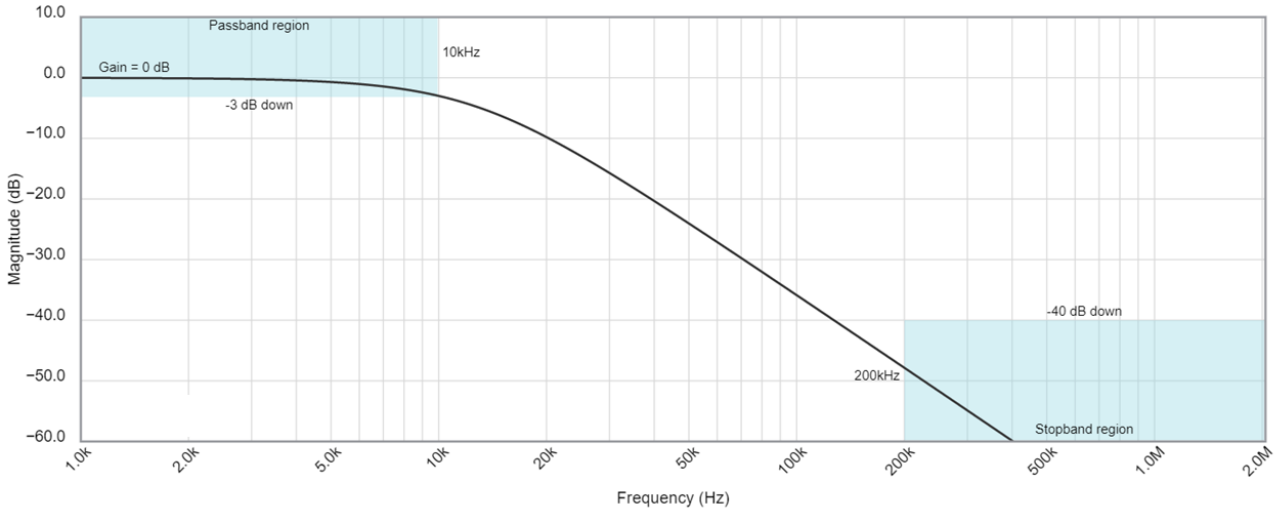
The following Bode plot is from a 6th order Butterworth low pass filter with corner frequency of 10kHz. Use the information in the Bode plot to answer the following questions.



10. If you apply a 25kHz sin wave to this filter, how much attenuation will the output experience?
11. You want -35dB of attenuation, what frequency sin wave should you apply?
12. Estimate the slope of the magnitude in the stop band and use this to estimate the order of the filter. Hint, use the corner frequency as one of your points.



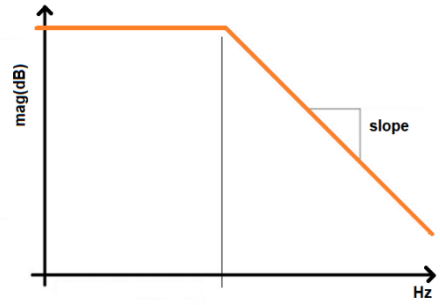
The following Bode plot is from a 2nd order Bessel low pass filter (note the slow roll off) with corner frequency of 10kHz. Use the information in the Bode plot to answer the following questions.



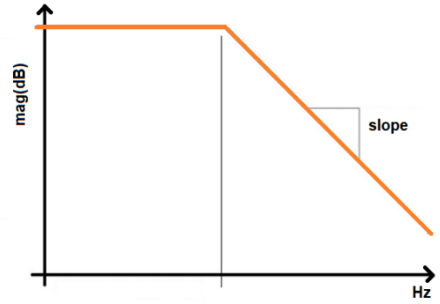
13. If you apply a 20kHz sin wave to this filter, how much attenuation will the output experience?
14. You want -55dB of attenuation, what frequency sin wave should you apply?
15. Estimate the slope of the magnitude in the stop band and use this to estimate the order of the filter. Hint, use the corner frequency as one of your points.

The following questions are based on a 1st order LPF with 0dB of attenuation in the passband. You will find it helpful to annotate the Bode plot with the

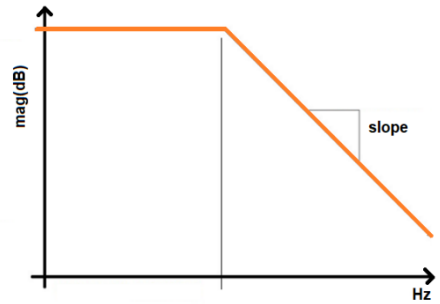
a. Given an 80kHz input signal, how much is the output attenuated?



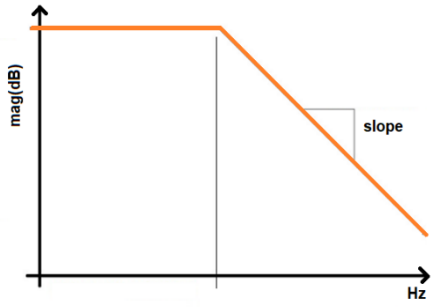
b. Given that the output signal has been attenuated by -48dB, what was the frequency of the input?



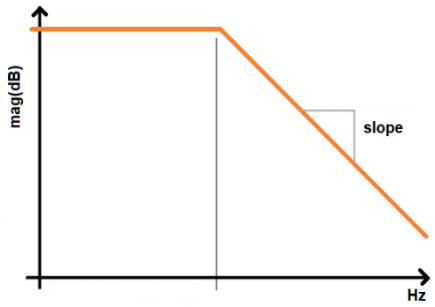
16. Determine the corner frequency of a 4th order LPF that has 0dB of attenuation in the passband and attenuates a 130kHz input by -68dB.



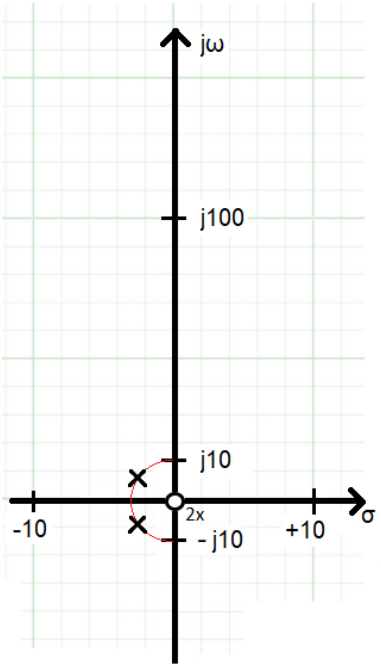
17. Determine the order of a filter that has 0dB of attenuation in the passband, a 15kHz corner frequency and attenuates a 90kHz input by -77.8dB.

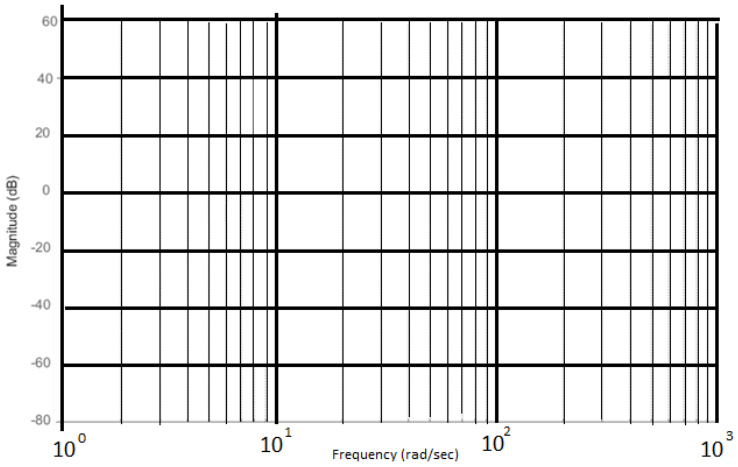


18. Determine the magnitude in the passband of a second order LPF, an 8kHz corner frequency and attenuates a 56kHz input by -13.8dB.

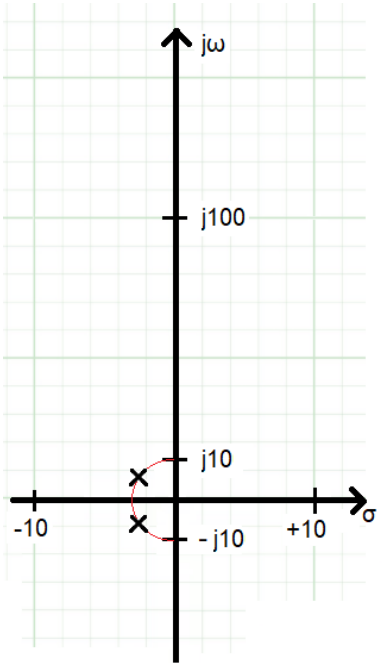


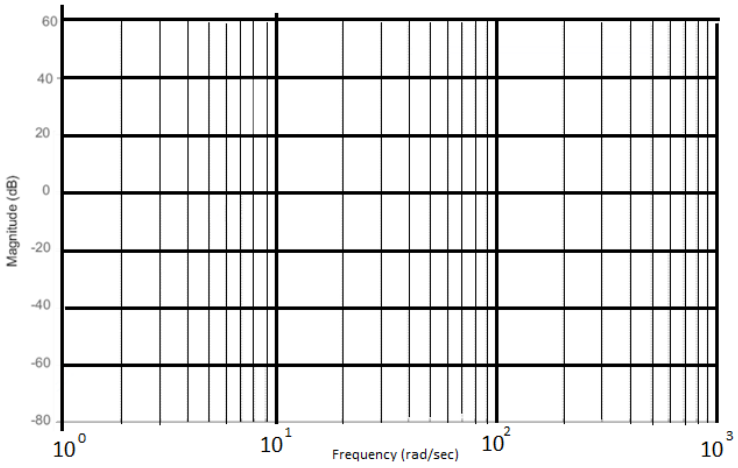
13. Use the pole zero locations of a transfer function given in the plot below to determine the frequency response of the transfer function. The real and imaginary axis are scaled differently. There are two zeros at the origin.



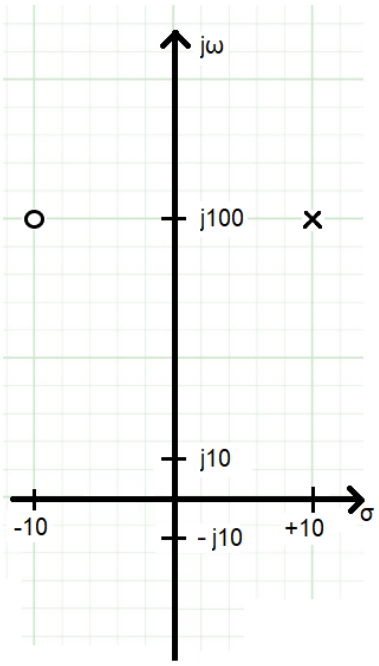


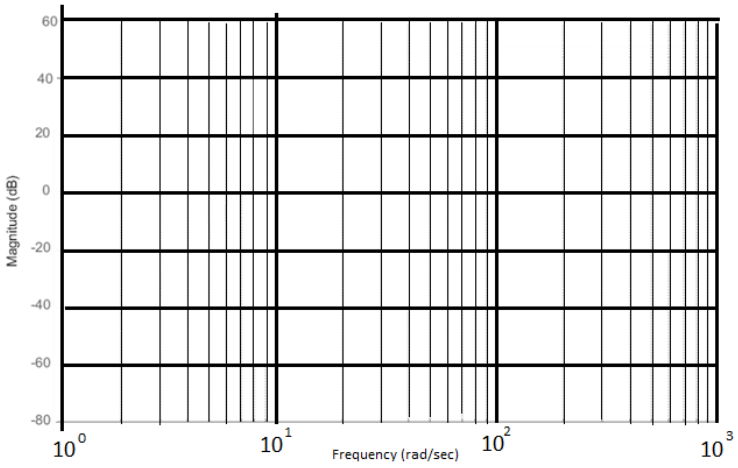
14. Use the pole zero locations of a transfer function given in the plot below to determine the frequency response of the transfer function. The real and imaginary axis are scaled differently.



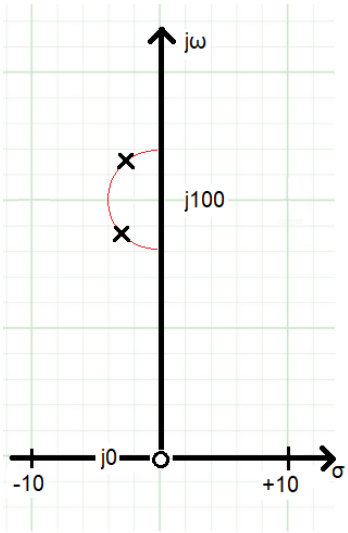


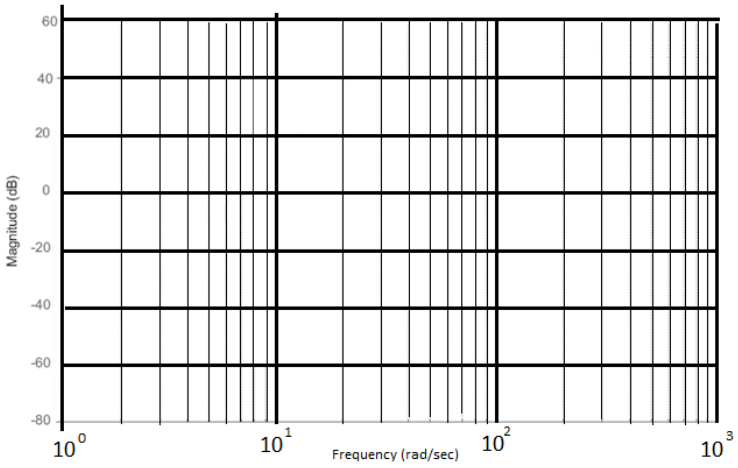
13. Use the pole zero locations of a transfer function given in the plot below to determine the frequency response of the transfer function. The real and imaginary axis are scaled differently.



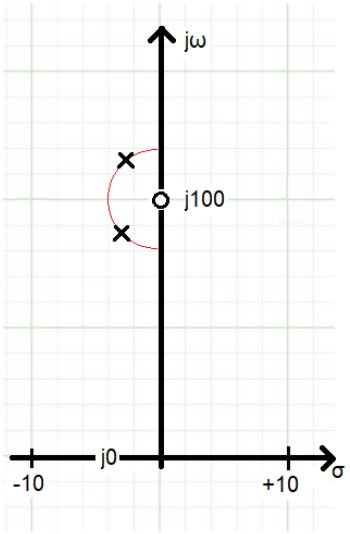


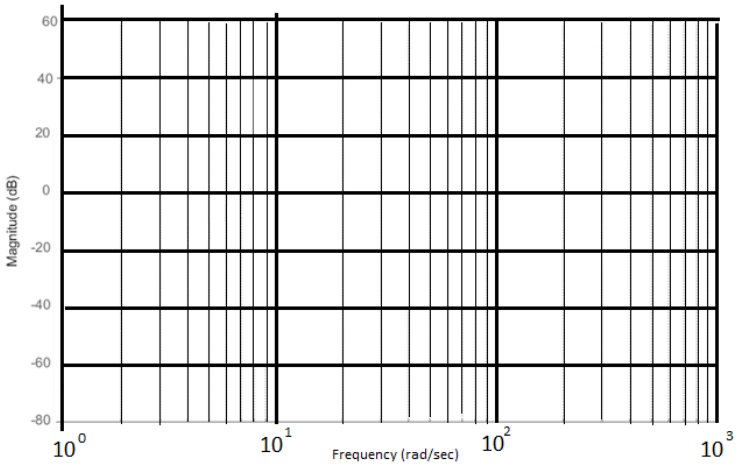
13. Use the pole zero locations of a transfer function given in the plot below to determine the frequency response of the transfer function. The real and imaginary axis are scaled differently. There is one zero a the origin.



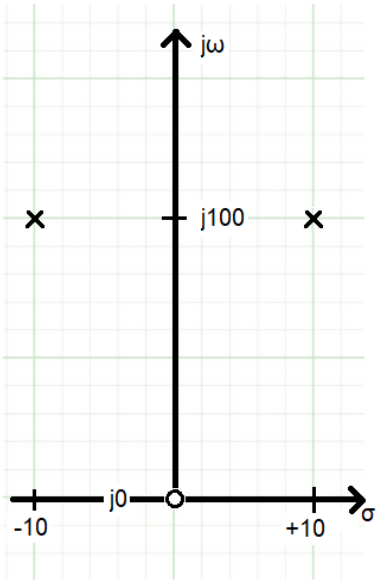


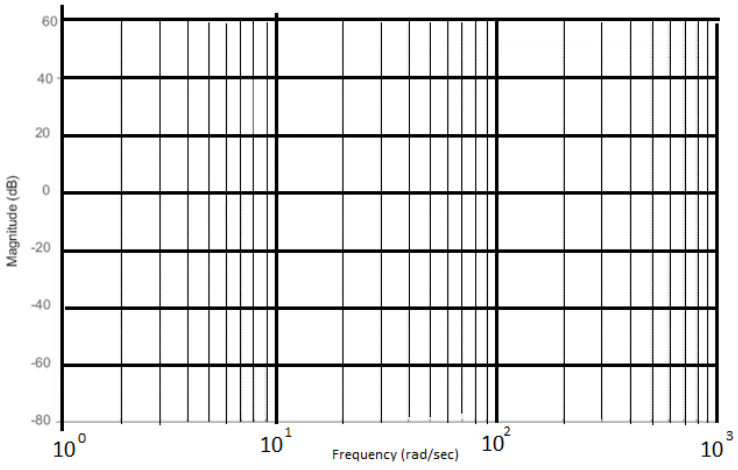
13. Use the pole zero locations of a transfer function given in the plot below to determine the frequency response of the transfer function. The real and imaginary axis are scaled differently. There is one zero at j100.





15. Use the pole zero locations of a transfer function given in the plot below to determine the frequency response of the transfer function. The real and imaginary axis are scaled differently.





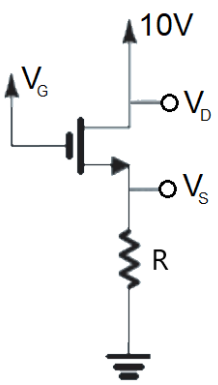
Chapter: MOSFETs

MOSFET circuits with Resistor(s) and DC source.

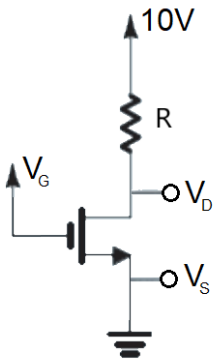
Fill in the blanks in the following table given the four circuit configurations below. Assume V_T = 1V and k = 1mA/V^2. In the Mode column enter one of the following:

- "Off" when V_G<V_T,
- "Triode" when V_{DS} < V_{GS} - V_T or
- "Saturation" when V_{DS} >= V_{GS} - V_T.

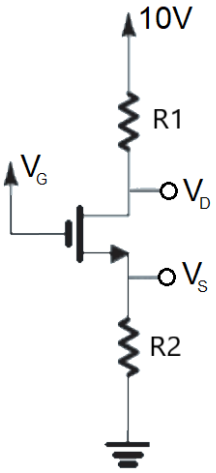
When the MOSFET is in the triode mode put "??" in the I_D column and any column that depends on I_D. When the MOSFET is in off mode, put "??" in the I_D column and any column that depends on I_D.



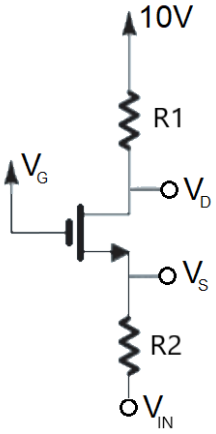
001



002



003



004

Circuit	V_D	V_G	V_S	V_{GS}	V_{OV}	R	I_D	Mode
001		0V				xx		
001		3V				1k		
001		6V				1k		
001		3V				10k		
001		6V				10k		
001		3V				100k		

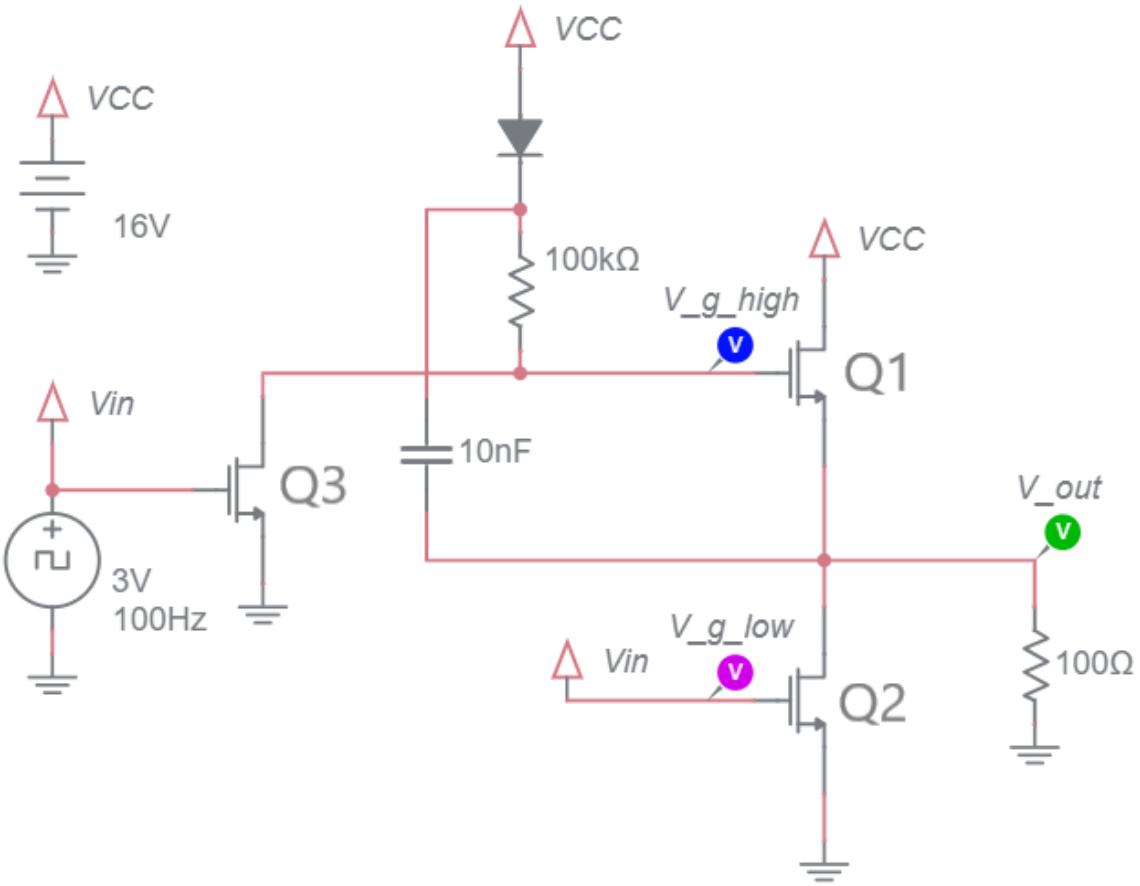
Circuit	V_D	V_G	V_S	V_{GS}	V_{OV}	R	I_D	Mode
002		0V				x		
002		3V				100Ω		
002		3V				1kΩ		
002		3V				10kΩ		
002		6V				100Ω		
002		6V				1kΩ		

Circuit	V_D	V_G	V_S	V_{GS}	V_{OV}	R1	R2	I_D	Mode
003		0V				xx			
003		3V				1kΩ	1k		
003		6V				1kΩ	1k		
003		3V				10k	10k		
003		3V				100k	1k		
003		6V				10k	1k		

Circuit	V_D	V_G	V_S	V_{GS}	V_{OV}	R1	R2	I_D	Mode
004		6V				1kΩ	1kΩ		

Practical Application - Half Bridge circuit with bootstrap capacitor

The following circuit allows a low power signal, modeled as the 3V, 100Hz square wave in the schematic, to control a high voltage, high power load, modeled as the 100Ω resistor. In order to understand how the following circuit accomplishes this, work through the following questions.



Assume that Vin is 3V

1. Do MOSFETs Q2 and Q3 act more like open switches (allowing no current to flow) or closed switches (allowing current to flow)?
2. Assume MOSFET Q3 is acting like a closed switch
    a. What is the gate voltage of MOSFET Q1?
    b. Can V_{gs} of Q1 ever be greater than V_T?
    c. Does Q1 act like an open switch or closed switch?

The switch settings you have discovered are incorporated in the schematic to produce the modified schematic shown below left.

3. After a short delay, what will be the voltage across the 10nF capacitor. For simplicity, assume an ideal diode model.

Assume that Vin is 0V

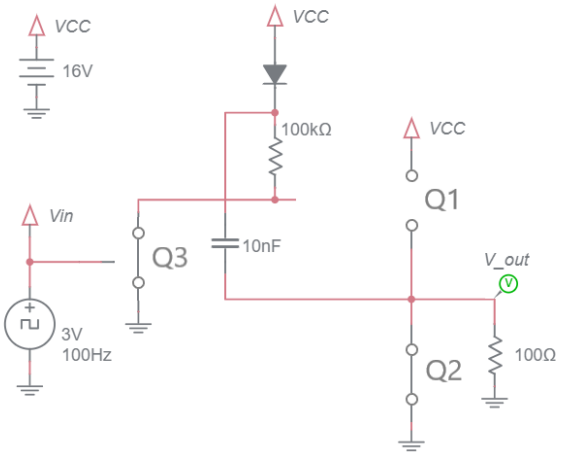
1. Do MOSFETs Q2 and Q3 act more like open switches (allowing no current to flow) or closed switches (allowing current to flow)?
2. Assume MOSFET Q3 is acting like an open switch and that the 10nF is fully charge from a period where Vin was 3V

a. What is V_{gs} for MOSFET Q1? Hint the answer is dictated by the voltage stored on the 10nF capacitor.
b. Does Q1 act like an open switch or closed switch?

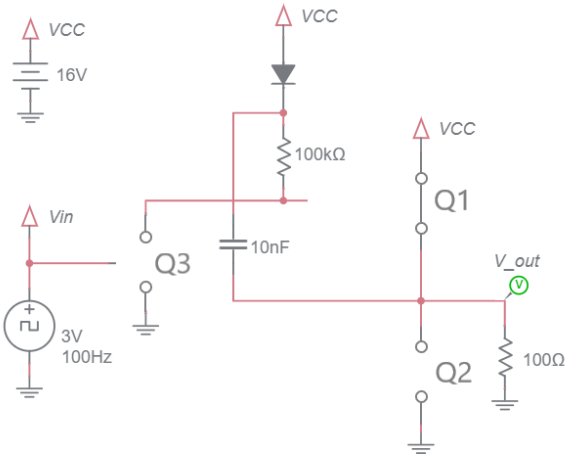
The switch settings you have discovered are incorporated in the schematic to produce the modified schematic shown below right.

3. The charge on the top plate of the capacitor flow could flow
   a. Through the 100kΩ and on to the drain of Q3 to ground
   b. Through the 100kΩ and on to the gate of Q1
   c. Through the diode to Vcc

   In each case, explain why no charge will flow off the top plate of the capacitor.



MOSFET behavior when Vin = 3V



MOSFET behavior when Vin = 0V