

# EENG307: PD Design Using Root Locus and SISOtool<sup>1</sup>

Elenya Grant, Kathryn Johnson, and Hisham Sager<sup>2</sup>

Department of Electrical Engineering  
Colorado School of Mines

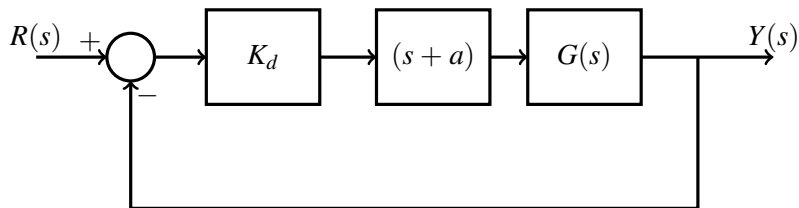
## Lecture 19

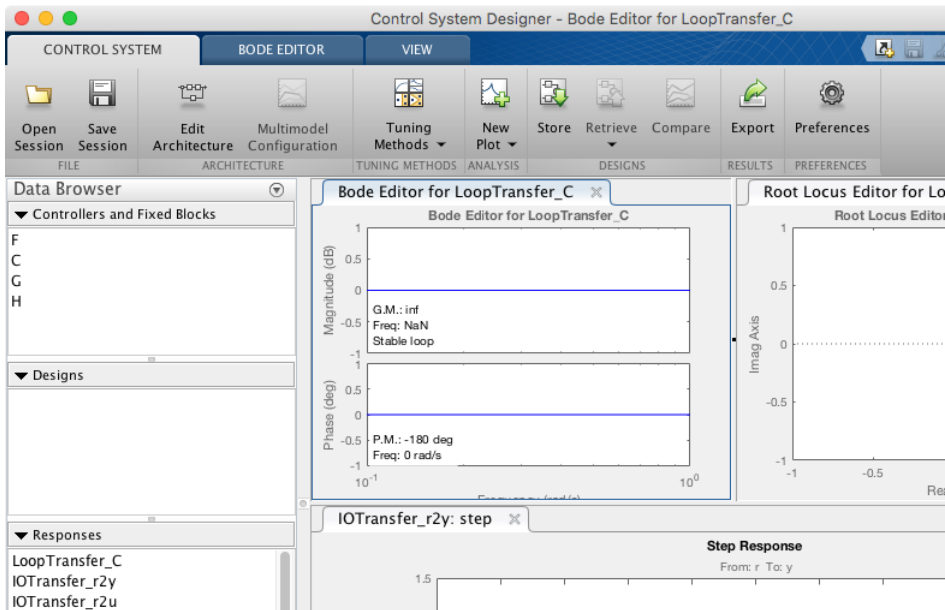
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<sup>2</sup> Developed and edited by Tyrone Vincent and Kathryn Johnson, Colorado School of Mines, with contributions from Salman Mohagheghi, Chris Coulston, Kevin Moore, CSM and Matt Kupilik, University of Alaska, Anchorage

# Root Locus Design Problem





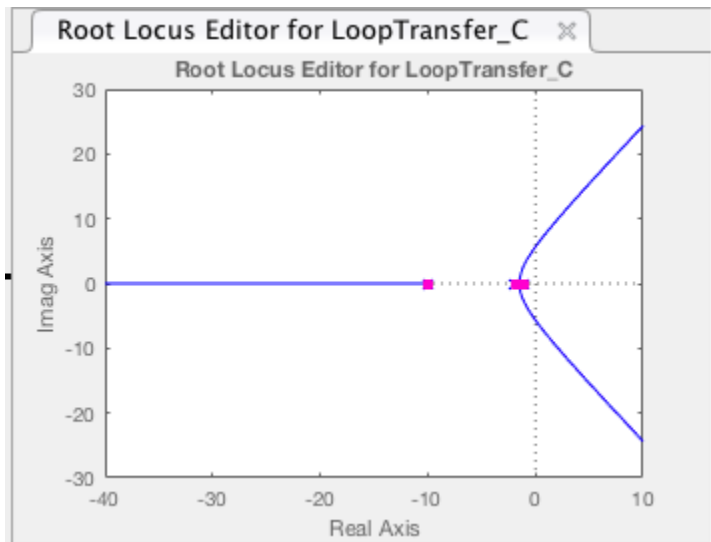
**Edit Architecture - Configuration 1**

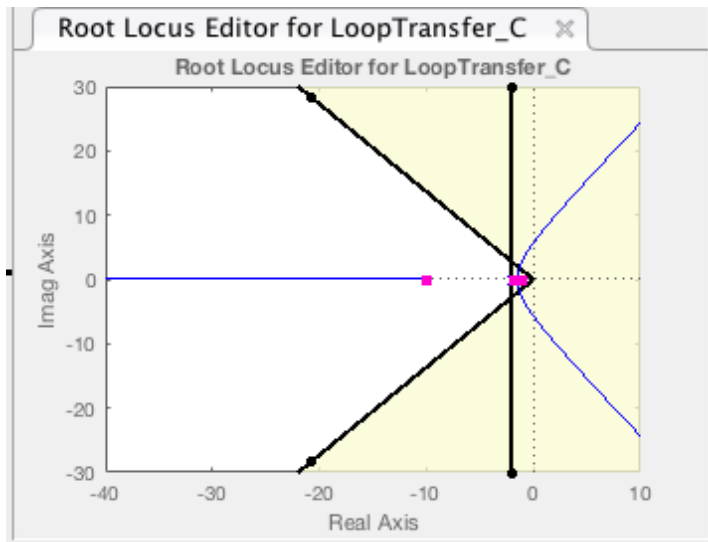
Select Control Architecture:

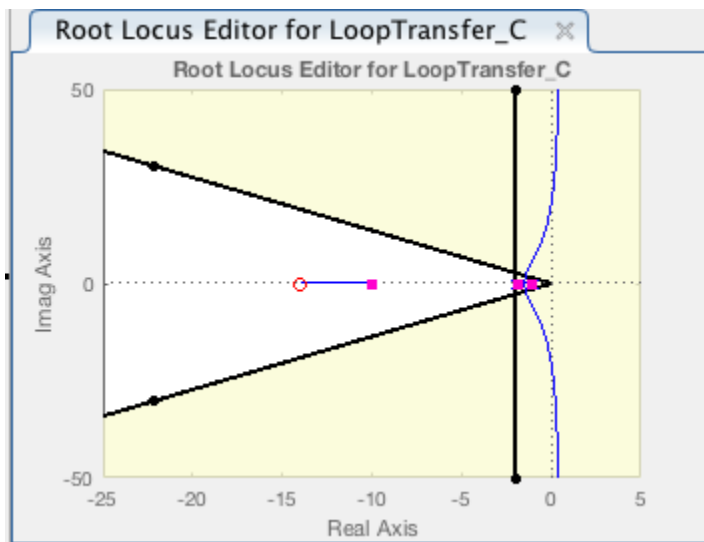
**Blocks**   **Loop Signs**

Identifier	Block Name	Value
C	C	<1x1 zpk>
F	F	<1x1 zpk>
G	G	sys
H	H	<1x1 tf>

OK   Cancel   Help







**Data Browser** ▼

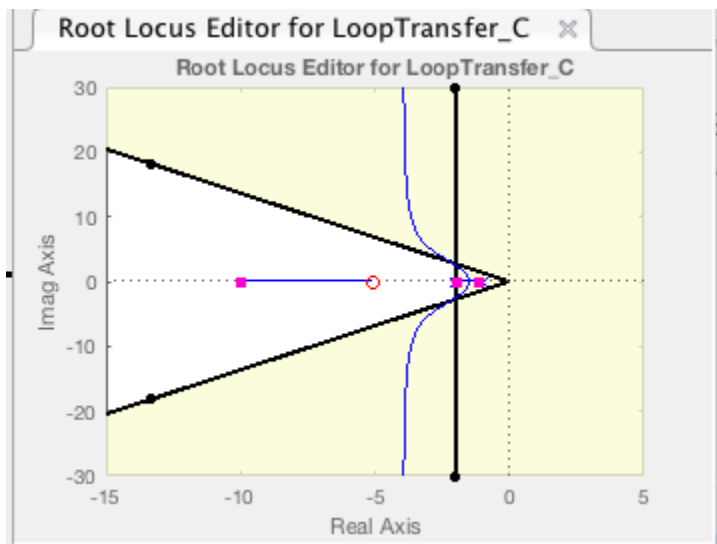
▼ Controllers and Fixed Blocks

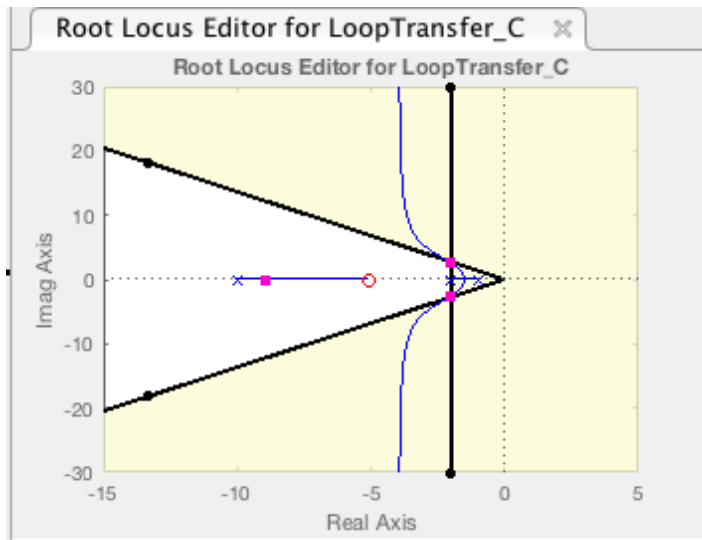
- F
- C**
- G
- H

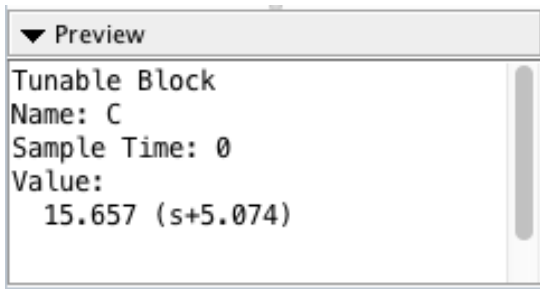
▼ Preview

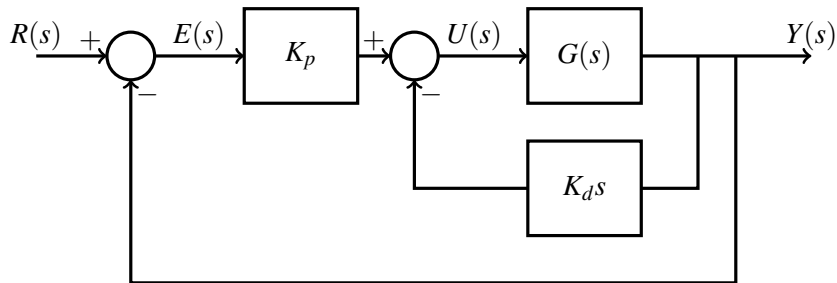
Tunable Block  
Name: C  
Sample Time: 0  
Value:  
0.071353 (s+14.01)











»  $\text{step}(T)$

