EE382M-11, Verification of Digital Systems — J. Abraham

Spring 2018 — Outline Solution for Exam — April 12, 2016

Name:

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1. System Verilog constraints:

constraint cond_fifo_write { fifo_full -> !wr; }

constraint cond_fifo_read { fifo_empty -> !rd; }

2.

(a) Option (C): (00*11*)* + (11*00*)*
Counter examples for rest of the options:
Option (A): 101; Option (B): 101; Option (D): 00111100

(b) Option (D): 1*+ 1*01*
Counter examples for rest of the options:
Option (A): 011 or 110; Option (B): 101; Option (C): 0 or 101 or 10

(c) Option (C): (0+10)*1*
Counter examples for rest of the options: Options A, B and D have the term (1+0)* which covers all string patterns.

3.

(a) Option (A): (a+b)*abb
Counter examples for rest of the options:
Option (B): bb - Not detected by FSM; Option (C): (a)(ba)(ba)bb - Not detected by this regular expression; Option (D): aaa - Not detected by FSM; Option (E): bbb - Not detected by FSM.

(b) Option (D): (b*a)(b*a)* Counter examples for rest of the options: Option (A): aa - Not detected by this regular expression; Option (B): aa - Not detected by this regular expression; Option (C): Null string - Not detected by FSM; Option (E): aa - Not detected by this regular expression.

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4. One of the satisfying assignments is {a=0, b=0, c=1, d=1, e=0, f=0, g=1}

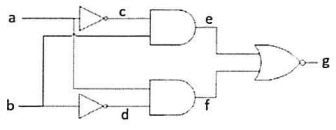

Figure 1: Gate level circuit diagram

5.

(a) Transition Functions:
$x' = x.\overline{r} + ry$
$y' = y.\overline{r} + r.x$
$T(x, y, x', y') = (x' \leftrightarrow x)(y' \leftrightarrow y) + (x' \leftrightarrow y)(y' \leftrightarrow x)$

(b) Finding unreachble states using forward reachability algorithm. Given $I(V) = x.\overline{y}$, let $R(V)$ denote the set of all states reachable. We will initialize $R(V)$ with $I(V)$ and use the image computation algorithm with the transition relation $T(V, V')$.
For each iteration, let $F(V)$ denote the set reachable from $R(V)$ in one step.

Step 1: $R(V) = x.\overline{y}$
$F(V') = \exists V\_R(V).T(V, V')$
$F(V') = x'.\overline{y'} + y'.\overline{x'}$
$F(V) = x.\overline{y} + y.\overline{x}$
New state is discovered, so we will continue to the next iteration.
$R(V) = R(V) \vee F(V)$

Step 2: $R(V) = x.\overline{y} + y.\overline{x}$
$F(V') = \exists V\_R(V).T(V, V')$
$F(V') = x'.\overline{y'} + y'.\overline{x'}$
$F(V) = x.\overline{y} + y.\overline{x}$
No new state is discovered, that is, $R(V) = F(V)$. Hence, the unreachable states are $\overline{x}.\overline{y}$ and x.y.

(c) Assertion:
a_state_check: assert property(@(posedge clk) disable iff(!reset) $x \hat{} y$);

6.

(a) For Property 1, sig1 is true in the first clock tick, and sig3 is true in the last clock tick with sig 2 true in the penultimate clock tick. Including this penultimate clock tick sig2 is true for at least 2 and at most 6 consecutive clock ticks
One such waveform :

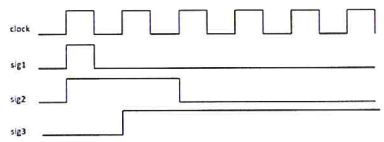

Figure 2: Waveform for 6(a)

(b) For Property 2, sig1 is true in the first clock tick, and sig3 is true in the last clock tick with sig 2 true in the penultimate clock tick. Including this penultimate clock tick sig2 is true for at least 2 and at most 6 non consecutive clock ticks
One such waveform :

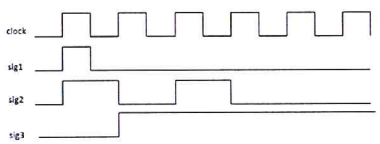

Figure 3: Waveform for 6(b)