EE382M.11, Verification of Digital Systems J. Abraham

Spring 2018 Exam April 12, 2018

Name: _____

Open Book, Open Notes, 80 minutes (pace yourself). Write all your answers in the spaces/boxes provided, and show any calculations in these pages using the back of the pages if needed.

1. (**15 Points**) **[SystemVerilog Constraints]** Consider a FIFO of depth 4 and width 32, with the module definition given below.

   module fifo(
   input clk, // Clock
   input rst, // Active high reset
   input rd, // Active high read enable
   input wr, // Active high write enable
   input [31:0] wr_data, // 32-bit wide write data
   output [31:0] rd_data, // 32-bit wide read data
   output fifo_empty, // When 1, indicates FIFO is empty, that is, the number of elements in the FIFO is zero.
   output fifo_full // When 1, indicates FIFO is full, that is, the number of elements in FIFO is four.
   );
   - - -
   endmodule

   Write the SystemVerilog constraints to (a) **NOT** perform a read when the FIFO is empty, and (b) to **NOT** perform a write when the FIFO is full.

2. (**15 Points**) Pick the regular expressions for the following strings.
In each case the alphabet is {0, 1}.

   (a) (**5 Points**) The set of all strings in which the number of groups of consecutive 1s equals the number of groups of consecutive 0s.

   (A) (1*0*)*
   (B) (1*0*)* + (0*1*)*
   (C) (00*11*)* + (11*00*)*
   (D) ((00*11*) + (11*00*))*

   (b) (**5 Points**) The set of all strings with at most one 0.

   (A) 11*011* + 1*
   (B) 01* + 1*0
   (C) 1*
   (D) 1*+ 1*01*

   (c) (**5 Points**) The set of strings that do not contain the substring 110.

   (A) (01+(1+0))*
   (B) (0+1)*1(0+1)*1(0+1)*1
   (C) (0+10)*1*
   (D) (0+1)((0+1)(0+1))*

3. (**20 Points**) The input symbol set of the following FSM is {a, b}, and the starting state is indicated by the arrow.

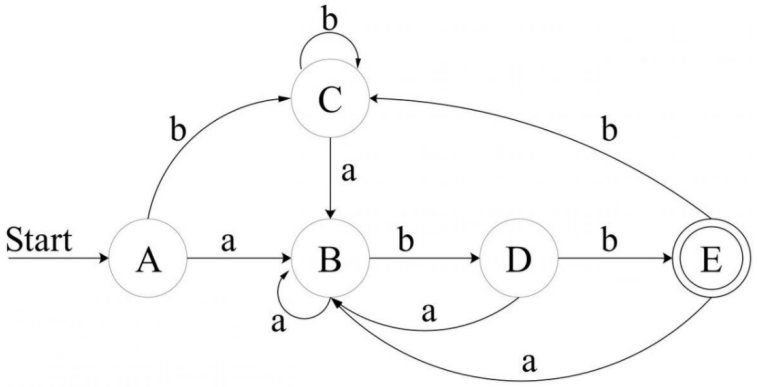


Figure 1: FSM

(a) (**10 Points**) Pick the regular expression for the sequence detected by this FSM with E as end (accepting) state.

(A) (a+b)*abb
(B) (b*a)*bb
(C) (a+bb*a)(a*+b*a)bb
(D) (a+b)*
(E) (a+b)a*bb

(b) (**10 Points**) Pick the regular expression for the sequence detected by this FSM with B as an accepting (end) state.

(A) a+bb*a
(B) (a+bb*a)(bb*a)*
(C) (b*a)*
(D) (b*a)(b*a)*
(E) (b*a)(ba+bba+bbb*a)*

4. (**15 Points**) Given the CNF clauses below, find a satisfying assignment and draw the circuit diagram for the set of clauses.

   CNFclause $= (a+c)(\overline{a}+\overline{c})(\overline{c}+\overline{b}+e)(c+\overline{e})(b+\overline{e})(b+d)(\overline{b}+\overline{d})(\overline{a}+\overline{d}+f)(a+\overline{f})(d+\overline{f})(e+f+g)(\overline{g}+\overline{e})(\overline{f}+\overline{g})g$

5. (**20 Points**) Consider the FSM circuit shown in Figure 2. The FSM retains or swaps the values of the state variables based on the input r. Let $V = \{x, y\}$ be the current state, $V' = \{x', y'\}$ the next state, and the initial state is $I(V) = \{x = 1, y = 0\}$.

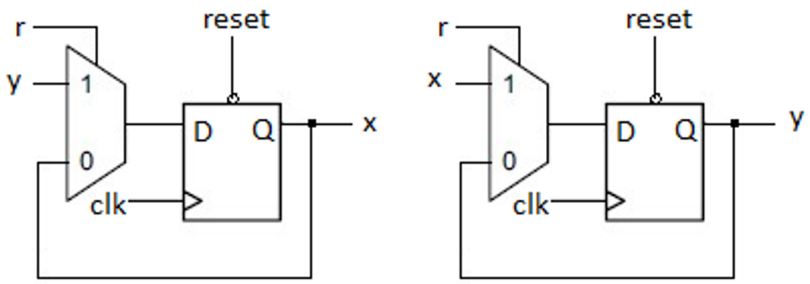


Figure 2: FSM circuit

(a) (**5 Points**) Write the transition functions for x' and y' and the transition relation $\widetilde{T}(V, V')$.

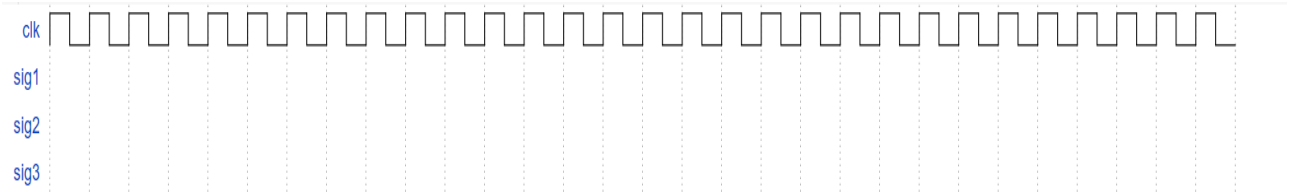
(b) (**10 Points**) Find the unreachable state/states using forward reachability.

(c) (**5 Points**) Write the SystemVerilog assertion which will fail if the FSM enters the unreachable state/states.

6. (**15 Points**) **[System Verilog Assertions]**

Draw one of the possible matching wave forms for each of the following properties.

(a) property p;
@(posedge clock) $rose(sig1) |-> sig2[*2:6] ##1 (sig3 == 1);
endproperty
a: assert property(p);



(b) property p;
@(posedge clock) $rose(sig1) |-> sig2[=2:6] ##1 (sig3 == 1);
endproperty
a: assert property(p);