03/11/19 HOMEWORK # 04 Saqib Khan
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1 a) Describe some safety properties of this arbiter?

A safety property asserts that nothing bad happens

i) If rst_n is triggered and grant0 ⇐ 1 or grant1 ⇐ 0
ii) if grant0 or grant 1 changes value without a posedge clk or negedge rst_n

b) Describe some liveness properties of this arbiter?

A liveness property asserts that something good eventually happens.

i) If rst_n is triggered and grant0 ⇐ 0 or grant1 ⇐ 1
ii) If grant0 ⇐ req0 && ((!req1) || ((!grant0) && grant1)) during a posedge clk or negedge rst_n

1 c) Will the assert property mentioned in the code be satisfied? Use symbolic model checking to formally prove your answer.

Ans) Let $x \Rightarrow$ grant 0 and $y \Rightarrow$ grant 1

$rx \Rightarrow$ req 0 and $ry \Rightarrow$ req 1

State Variable: $V = \{x, y\}$

$V' = \{x', y'\} \Rightarrow$ next state

Initial State: $I(V) = \bar{x}\, y$

Transition Functions:

$$x' = rx\,(\overline{ry} + \bar{x}y)$$

$$y' = ry\,(\overline{rx} + \bar{y}x)$$

$\therefore$ $xy \Longrightarrow$ bad / error state

transition relation $\tilde{T}(V, rx, ry, V') = (x' \leftrightarrow rx(\overline{ry} + \bar{x}y))$
$(y' \leftrightarrow ry(\overline{rx} + \bar{y}x))$

$\therefore$ $T(V, V') = \exists rx, ry\; \tilde{T}(V, rx, ry, V')$

Set of all reachable states: $R(V) = \bar{x}y \Longrightarrow$ STEP 1

Set reachable from $R(V)$ in one step $\longrightarrow F(V') = \bar{x}'\bar{y}' + \bar{x}'y' + x'\bar{y}'$

$$F(V) = \bar{x}'\bar{y}' + \bar{x}'y' + x'\bar{y}'$$

$$F(V) = \bar{x}\bar{y} + \bar{x}y + x\bar{y}$$

New State discovered. Continue to next iteration

Continuation of Q1 c)

STEP 2 $R(V) = \bar{x}\bar{y} + \bar{x}y + x\bar{y}$

$$F(V') = \bar{x}'\bar{y}' + \bar{x}'y' + x'\bar{y}'$$

$$F(V) = \bar{x}\bar{y} + \bar{x}y + x\bar{y}$$

No new state discovered.

Thus the algorithm "PASSES"

2) Consider set of terms :- as $\langle 2NOR(), A, B, C, a, b, \neg, \vee, \wedge \rangle$

a) Write a set of rules for a 2-input NOR

R1 :- $a \vee b \rightarrow \neg 2NOR(a,b)$

R2 :- $\neg(\neg a) \rightarrow a$

R3 :- $\neg a \rightarrow 2NOR(a,a)$

R4 :- $a \wedge b \rightarrow \neg(\neg a \vee \neg b)$

R5 :- $a \wedge b \wedge C \rightarrow (a \wedge b) \wedge C$

b) Apply above rules to rewrite 3-input NAND $(\neg(A \wedge B \wedge C))$ using only 2NOR()

$\neg(A \wedge B \wedge C)$

R5 :- $\neg((A \wedge B) \wedge C)$

R4 :- $\neg(\neg(\neg A \vee \neg B) \wedge C)$

R1 :- $\neg(\neg(\neg 2NOR(\neg A, \neg B)) \wedge C)$

R2 :- $\neg(2NOR(\neg A, \neg B) \wedge C)$

R4, R2, R1 :- $(\neg 2NOR(\neg 2NOR(\neg A, \neg B), \neg C)$

R2, R3, R3 ___ :-

2NOR(2NOR(2NOR(2NOR(2NOR(A, A), 2NOR(B,B)), 2NOR(C,C), 2NOR(2NOR(A,A), 2NOR(B,B)), 2NOR(C,C))), 2NOR(2NOR(2NOR(2NOR(A,A), 2NOR(B,B)), 2NOR(C,C), 2NOR(2NOR(A,A), 2NOR(B,B)), 2NOR(C,C)))

3) Safety Property = $\bigwedge_{k} \bigwedge_{i} \bigwedge_{j \neq 1} \neg p_{ik} \vee \neg p_{jk}$

Liveness Property = $\bigwedge_{0 \le k < n} \left(\bigvee_{0 \le l < n-1} p_{k,l} \right)$

It is difficult for the SAT solver to find a satisfying interpretation for this problem due to symmetry

4) Write the CNF formulating representing the one-hot condition on the bits of the vector

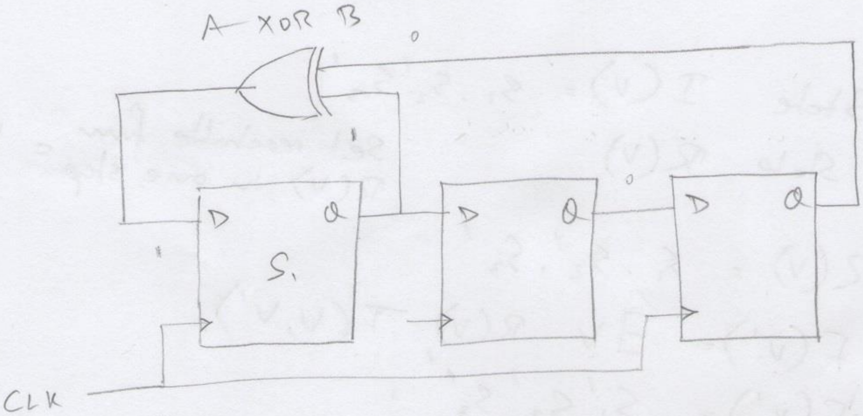
X_1, X_2, X_3, X_4, X_5

$(X_1' \vee X_2') \wedge (X_1' \vee X_3') \wedge (X_1' \vee X_4') \wedge (X_1' \vee X_5') \wedge$
$(X_2' \vee X_3') \wedge (X_2' \vee X_4') \wedge (X_2' \vee X_5') \wedge$
$(X_3' \vee X_4') \wedge (X_3' \vee X_5) \wedge (X_4' \vee X_5') \wedge$
$(X_1 \vee X_2 \vee X_3 \vee X_4 \vee X_5)$

5 Current State :- $V = \langle S_1, S_2, S_3 \rangle$

Next State :- $V' = \langle S_1', S_2', S_3' \rangle$

$I(V) = (S_1 = 1, S_2 = 0, S_3 = 0)$ } Initial State



A XOR B = $AB' + A'B$

a) Transition functions:

$S_1' = S_1 S_3' + S_1' S_3$

$S_2' = S_1$

$S_3' = S_2$

b) Transition Relation, $\tilde{T}(V, V') = (S_1' \leftrightarrow S_1 S_3' + S_1' S_3) \cdot (S_2' \leftrightarrow S_1) \cdot (S_3' \leftrightarrow S_2)$

5c) Which state of the Pseudo-Random Sequence Generator is not reachable. Prove your answer using symbolic model checking.

Ans) The unreachable state is $s_1' s_2' s_3'$.

Given:-

Initial State $I(V) = s_1 . s_2' s_3'$

Reachable State $R(V)$

Set reachable from $R(V)$ in one step $= F(V)$

Step 1:- $R(V) = s_1 . s_2' . s_3'$

$F(V') = \exists V \; R(V) . T(V, V')$

$F(V') = s_1' s_2'' s_3''$

$F(V) = s_1 . s_2 . s_3'$

New State. Continue to next

$R(V) = R(V) \vee F(V)$

Step 2:- $R(V) = s_1 s_2' s_3' + s_1 s_2 s_3'$

$F(V') = \exists V \; R(V) . T(V, V')$

$F(V') = s_1' s_2' s_3' + s_1' s_2' s_3'$

$F(V) = s_1 s_2 s_3' + s_1 s_2 s_3$

New State. Continue on to next state

Continuation of 5c)

Step 7:- $R(V) = s_1 s_2' s_3' + s_1 + s_2 s_3' + s_1 s_2 s_3 + s_1' s_2 s_3 +$
$s_1 s_2' s_3 + s_1' s_2 s_3' + s_1' s_2' s_3$

$F(V') = s_1' s_2' s_3' + s_1' s_2' s_3' + s_1' s_2' s_3' +$
$s_1' s_2' s_3' + s_1' s_2' s_3' + s_1' s_2' s_3' + s_1' s_2' s_3'$

$\therefore F(V) = s_1 s_2' s_3' + s_1 s_2 s_3' + s_1 s_2 s_3 + s_1' s_2 s_3 +$
$s_1 s_2' s_3 + s_1' s_2 s_3' + s_1 s_2' s_3$

No new State.

$\therefore$ $R(V) = F(V)$, hence the state $s_1' s_2' s_3'$ is unreachable

5d) What happens if the circuit is in unreachable state?
Write a System Verilog Assertion for checking this condition.

Ans) assert property (@(posedge clk) s1 + s2 + s3);