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## HOMEWORK #02

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Sak2454

$$1) \quad S(a, b, c) = a \oplus b \oplus c$$

$$\Rightarrow (ab' + a'b) \oplus c$$

$$\Rightarrow (ab' + a'b)'c + (ab' + a'b)c'$$

$$\Rightarrow (ab')' \cdot (a'b)' \cdot c + ab'c' + a'bc'$$

$$\Rightarrow (a' + b)(a + b')c + ab'c' + a'bc'$$

$$\Rightarrow abc + ab'c' + a'bc' + a'b'c$$

$$C(a, b, c) = ab + ac + bc$$

$$a) \quad \forall a: S(a, b, c) \Rightarrow f|_{a=0}, f|_{a=1}$$

$$\Rightarrow (bc' + b'c) \cdot (bc + b'c')$$

$$\Rightarrow \cancel{bc'c} + \cancel{b'b'c'} + \cancel{bb'c} + \cancel{b'cc'}$$

$$\boxed{\forall a: S(a, b, c) \Rightarrow 0}$$

$$b) \quad \exists a: S(a, b, c) = f|_{a=0} + f|_{a=1}$$

$$= (bc' + b'c) + (bc + b'c')$$

$$= b \underbrace{(c + c')}_1 + b' \underbrace{(c + c')}_1$$

$$= b + b'$$

$$\boxed{\exists a: S(a, b, c) = 1}$$

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$$c) \forall a: C(a, b, c) = f|_{a=0} \cdot f|_{a=1}$$

$$= bc \cdot (b+c)$$

$$= bc + bc$$

$$\boxed{\forall a: C(a, b, c) = bc}$$

$$d) \exists a: C(a, b, c) = f|_{a=0} + f|_{a=1}$$

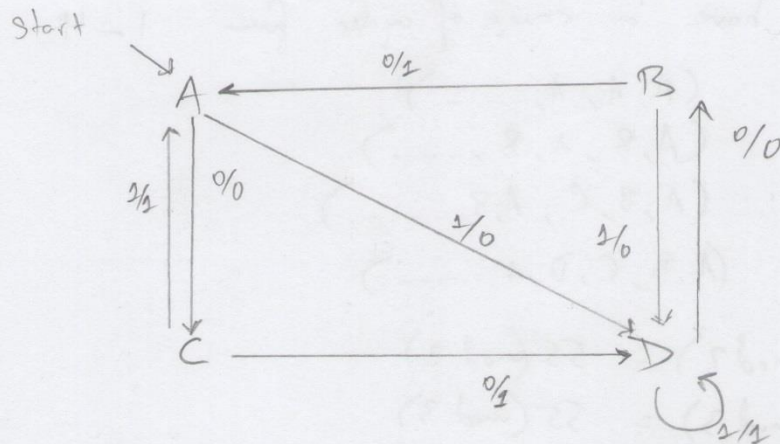
$$= bc + b + c$$

$$= b \underbrace{(c+1)}_1 + c$$

$$\boxed{\exists a: C(a, b, c) = b + c}$$

2 X: 001100110110001

Z: 011101010010101



This description is not unique because the FSM can possibly start at either A, B, C or D. Also, instead of going from  $A \rightarrow C$ , we could easily have gone to B instead.

Since no two states are the same (i.e. inputs + outputs), we can't reduce this to a 3-state machine.



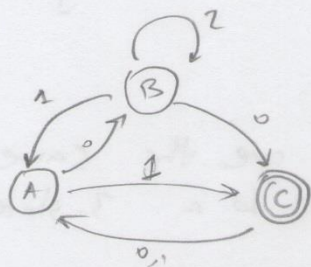
3 Since the FSM has 4 states, the application is bound to repeat a state after 4 transitions.  
 More specifically if we have consecutive 0's, then we can have a range of cycles from 1-4

cycle 1:- (A, A, A, ---)  
 cycle 2:- (A, B, A, B, ---)  
 cycle 3:- (A, B, C, A, B, ---)  
 cycle 4:- (A, B, C, D, A, ---)

Since  $7 \pmod{2} = 55 \pmod{2}$   
 $7 \pmod{3} = 55 \pmod{3}$   
 $7 \pmod{4} = 55 \pmod{4}$

Therefore the FSM will be in the same state after 7 or 55 transitions.

4)



Possible states =  
 AC  
 ABC  
 ABB--C  
 ABABC  
 ABAC

$$\left[ \underbrace{1(0+1) + 02^*0(0+1) + 02^*1}_{\text{STAY IN A}} \right]^* \left( \underbrace{1}_{\substack{\uparrow \\ \text{AC}}} + \underbrace{02^*0}_{\text{ABC}} \right)$$

5

- a) No, can't be recognized by FSM. It needs infinite # of states to identify the set.
- b) Yes, can be recognized by FSM using 5 states
- c) Yes, since  $k$  is a specified number
- d) No, because it needs infinite # of states to recognize
- e) Yes
- f) Yes, if length = 7, then there are  $2^7 = 128$  sequences that can justify this FSM.

6 a)  $(011^* + 01^*0)^*$  and  $(00)^*01(0+1)^* + X$

Not Equal

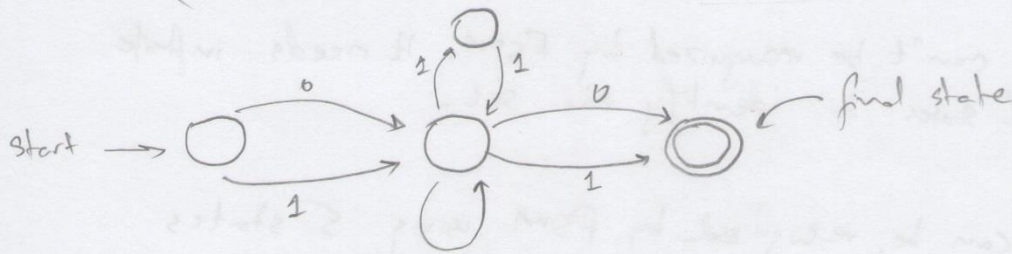
b)  $(1^*0 + 001)^*01$  and  $(1^*001 + 00101)^*$

Not Equal

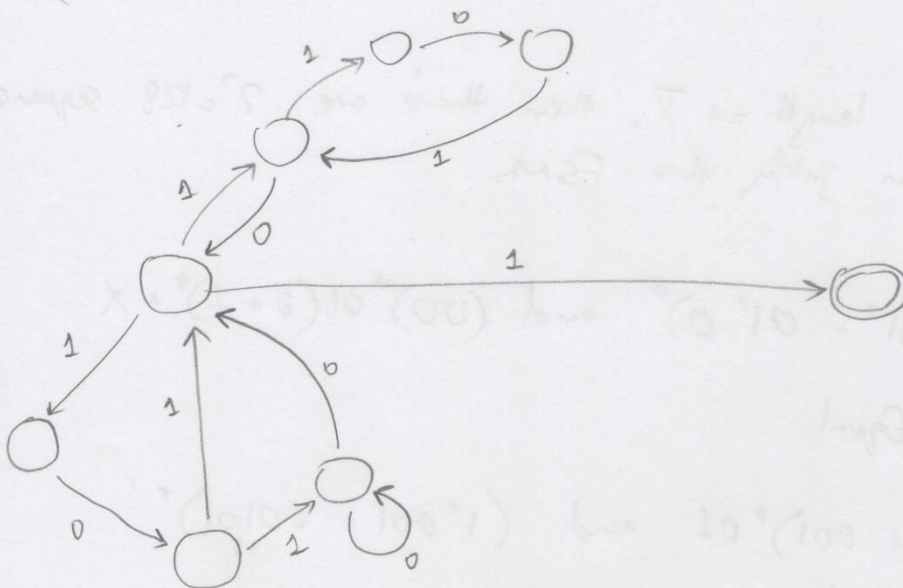
c)  $0^*1(0+10^*1)^*$  and  $(1+00^*1) + (1+00^*1)(0+10^*1)^*(0+10^*1)$

Equal

7) a)  $(0+1)(1+0^*)^*(0+1)$



b)  $(1010^* + 1(101)^*0)^*1$

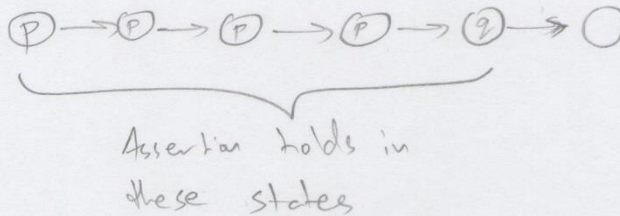




8 a) This technique is not scalable

b) assert property (@posedge clk) disable ff (!rst\_n)  
!(grant0 && grant1));

9) p s-until q



10) \$rose(expression) :- true if the least significant bit of the expression changed to 1;  
false otherwise

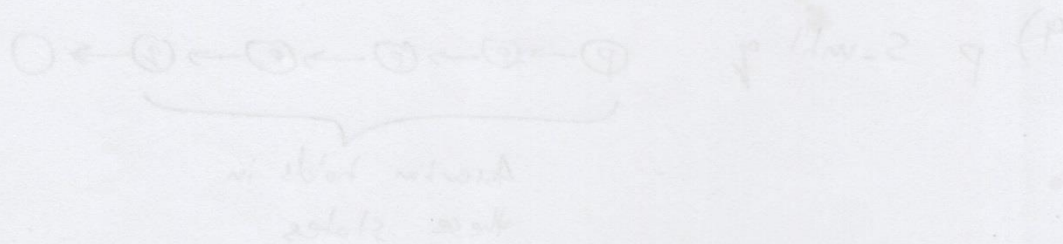
@posedge

:- it is an event that is triggered on the positive edge of the clock (or any expression) and has no returns.

11)

a) property p-start;  
 @(posedge clk) \$rose(sel-bit) | => ##1 tdy  
 ##1 !tdy;  
 endproperty

b) property p-stop;  
 @(posedge clk) \$fell(sel-bit) | => tdy



1) Phase (expression) - true if the last sample of the expression changed to 1.  
 (true when true)

2) Edge (expression) - true if an event has occurred on the rising edge of the clock (implied) and true on falling edge.



