

LAB # 01

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Class: EE 382M Verification of Digital Systems

PART A:

1. A brief report describing the netlist bugs and your solution.

Bug # 1: mem_read_data_r_reg[6]

i_clk was negated before being fed into the dff. I changed that to be a positive input.

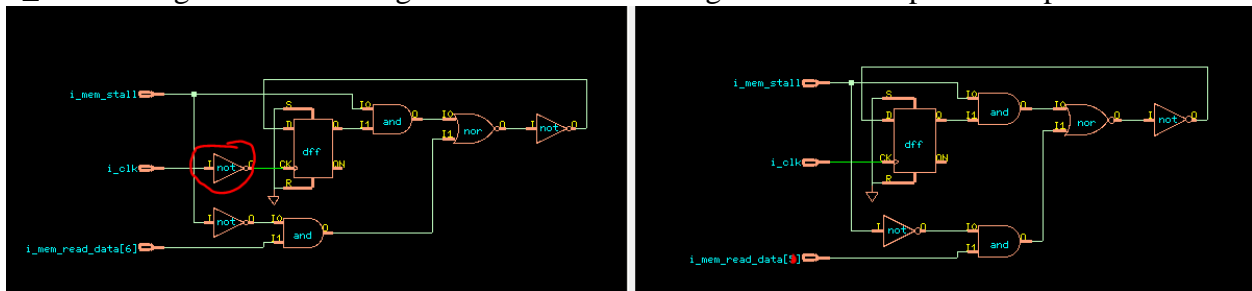


Figure-1 mem_read_data_r_reg[6] before and after the fix

Bug # 2: mem_read_data_r_reg[2]

The MUX inputs A and B were swapped. Flipping the two inputs give us the correct result.

Previous_implementation:

```
MUX2X1 U174 ( .B(o_wb_read_data[2]), .A(i_mem_read_data[2]), .S(i_mem_stall), .Y(n131) );
```

Corrected_implementation:

```
MUX2X1 U174 ( .B(i_mem_read_data[2]), .A(o_wb_read_data[2]), .S(i_mem_stall), .Y(n131) );
```

Bug # 3: mem_load_rd_r_reg[10]

Removed the additional NOT gate in the netlist

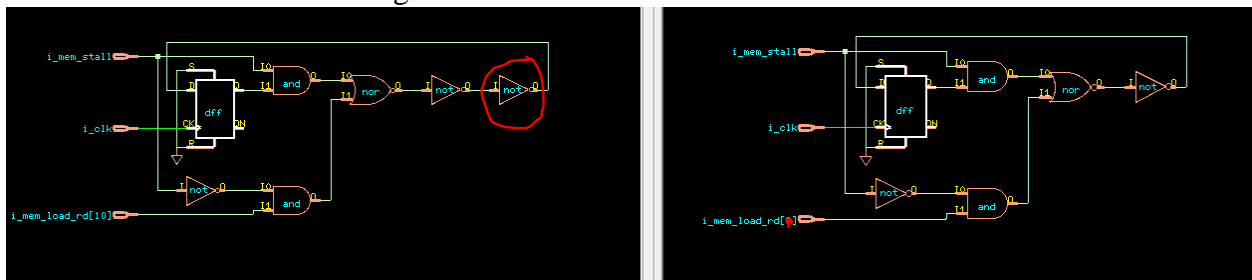


Figure-2 mem_load_rd_r_reg[10] before and after the fix

2. Final snapshot of the mapping manager and lec console.

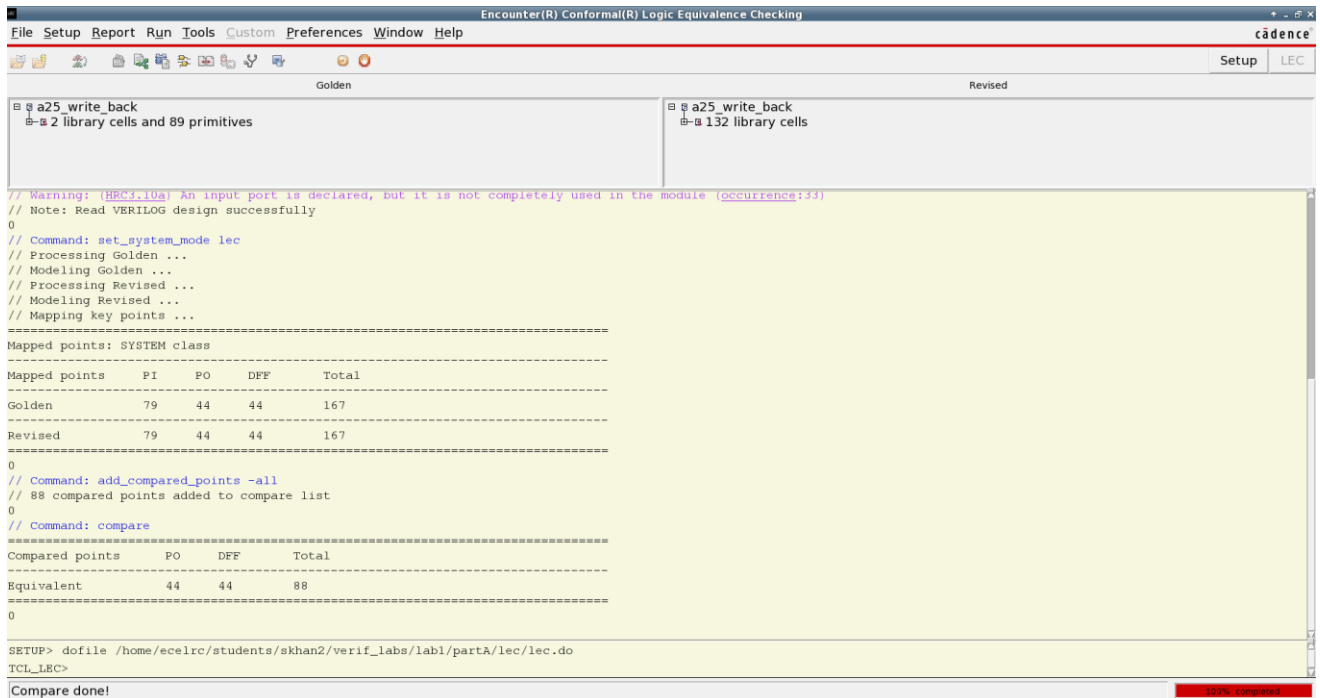


Figure-3 Snapshot of LEC console for Part-A

CONFORMAL-LEC Mapping Manager

OK Refresh Window Schematics Preferences Help

Unmapped Points

Mapped Points

(+)	PI	1	i_clk	(+)	PI	1	i_clk
(+)	PI	2	i_mem_stall	(+)	PI	2	i_mem_stall
(+)	PI	3	i_mem_read_data[31]	(+)	PI	3	i_mem_read_data[31]
(+)	PI	4	i_mem_read_data[30]	(+)	PI	4	i_mem_read_data[30]
(+)	PI	5	i_mem_read_data[29]	(+)	PI	5	i_mem_read_data[29]
(+)	PI	6	i_mem_read_data[28]	(+)	PI	6	i_mem_read_data[28]

Compared Points

Support Size

● (+)	PO	80	o_wb_read_data[31]	(+)	PO	80	o_wb_read_data[31]
● (+)	PO	81	o_wb_read_data[30]	(+)	PO	81	o_wb_read_data[30]
● (+)	PO	82	o_wb_read_data[29]	(+)	PO	82	o_wb_read_data[29]
● (+)	PO	83	o_wb_read_data[28]	(+)	PO	83	o_wb_read_data[28]
● (+)	PO	84	o_wb_read_data[27]	(+)	PO	84	o_wb_read_data[27]
● (+)	PO	85	o_wb_read_data[26]	(+)	PO	85	o_wb_read_data[26]
● (+)	PO	86	o_wb_read_data[25]	(+)	PO	86	o_wb_read_data[25]
● (+)	PO	87	o_wb_read_data[24]	(+)	PO	87	o_wb_read_data[24]
● (+)	PO	88	o_wb_read_data[23]	(+)	PO	88	o_wb_read_data[23]
● (+)	PO	89	o_wb_read_data[22]	(+)	PO	89	o_wb_read_data[22]
● (+)	PO	90	o_wb_read_data[21]	(+)	PO	90	o_wb_read_data[21]

Figure-4 Snapshot of Mapping Manager for Part-A

PART B:

1. Brief description of the scan structure of the SoC.

The scan insertion replaces normal flops with special scan flops that allows us to monitor and control the state of the design using specific ports. It uses the Automatic Test Pattern Generator (ATPG) tool to generate tests for improved fault coverage testing.

The scan structure of the SoC using in this lab includes:

- Minimum number of scan chains set to 4
- Maximum length of scan chains: no_value
- Lock-up element type: preferred_level_sensitive
- Mix clock edges in scan chain: true
- Prefix for unnamed scan objects: DFT_

2. The schematic of a clock gating cell in the netlist. (Search for the module with name 'RC_CG_MOD' in the netlist.

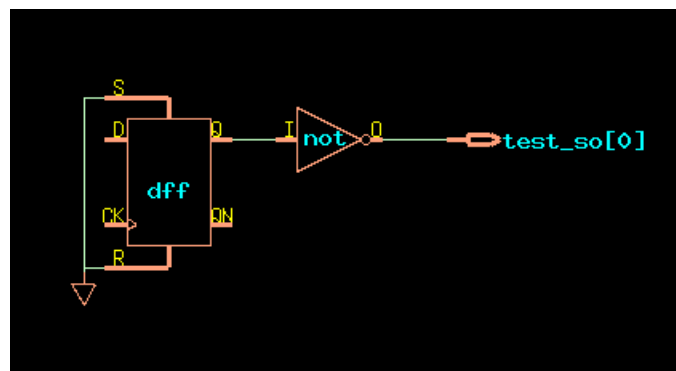


Figure-5 Snapshot of schematic for test_so[0]

3. What is the significance of the following commands in the lec.do file?

set_flatten_model -seq_constant -seq_constant_x_to 0:

- Set_flatten_model command is used to specify the conditions for circuit flattening.
- -seq_constant options is used for instance to convert a flop or latch to 0 or 1
- -seq_constant_x_to 0

set_flatten_model -gated_clock

- -gated_clock the synthesis tool adds clock gating for dynamic power optimization. This can cause issues while performing equivalence checking. “gated_clock” option resolves this problem by remodeling the revised clock gates to the golden model logic.

set_analyze_option -auto

Automatically sets the option for analyzing to on /off

4. Final snapshot of the mapping manager and lec console.

The screenshot shows the Encounter(R) Conformal(R) Logic Equivalence Checking (LEC) console. The interface is divided into two main panes: 'Golden' and 'Revised'. The 'Golden' pane displays a list of components including primitives, boot_mem_wrapper, clocks_resets, eth_top, interrupt_controller, iobuf, test_module, and timer_module. The 'Revised' pane displays a similar list of components, including library cells, boot_mem_wrapper, clocks_resets, eth_top, interrupt_controller, iobuf, test_module, and timer_module. Below these panes, a large text area shows the results of the comparison. The text includes a warning about unmapped key points, a table of compared points, and a summary of the comparison results.

```
// Warning: 5835 non-zero unmapped key points which will not be compared
// 5835 compared points added to compare list
0
// Command: compare
=====
Compared points      PO      DFF      BBOX      Total
-----
Equivalent           59      5759      17         5835
=====
Compare results of instance/output/pin equivalences and/or sequential merge
=====
Compared points      DFF      Total
-----
Equivalent           75         75
=====
// Warning: There are extra POs in Revised
0
// Command: puts "Num of compare points = [get_compare_points -count]"
Num of compare points = 5835
// Command: puts "Num of diff points   = [get_compare_points -NOHequivalent -count]"
Num of diff points   = 0
// Command: puts "Num of abort points  = [get_compare_points -abort -count]"
Num of abort points  = 0
// Command: puts "Num of unknown points = [get_compare_points -unknown -count]"
Num of unknown points = 0

SETUP> dofile /home/ecelrc/students/skhan2/verif_labs/lab1/partB/scripts/lec/lec.do
```

100% completed

Figure-6 Snapshot of LEC console for Part-B

CONFORMAL-LEC Mapping Manager

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Unmapped Points

PI	20	scan_en
PI	21	scan_cg_en
DFF	126	u_amber/u_fetch/u_cach
DFF	127	u_amber/u_fetch/u_cach
DFF	128	u_amber/u_fetch/u_cach
DFF	129	u_amber/u_fetch/u_cach
PI	20	test_si[0]
PI	21	test_si[1]
PI	22	test_si[2]
PI	23	test_si[3]
PO	104	test_so[0]
PO	105	test_so[1]

Mapped Points

(+)	PI	1	quick_n_reset
(+)	PI	2	brd_rst
(+)	PI	3	brd_clk_n
(+)	PI	4	brd_clk_p
(+)	PI	5	i_uart0_rts
(+)	PI	6	i_uart0_tx
(+)	PI	1	quick_n_reset
(+)	PI	2	brd_rst
(+)	PI	3	brd_clk_n
(+)	PI	4	brd_clk_p
(+)	PI	5	i_uart0_rts
(+)	PI	6	i_uart0_tx

Compared Points

(+)	PO	64	o_uart0_rx
(+)	PO	65	o_uart0_cts
(+)	PO	66	o_uart1_rx
(+)	PO	67	o_uart1_cts
(+)	PO	68	ddr3_addr[12]
(+)	PO	69	ddr3_addr[11]
(+)	PO	70	ddr3_addr[10]
(+)	PO	71	ddr3_addr[9]
(+)	PO	72	ddr3_addr[8]
(+)	PO	73	ddr3_addr[7]
(+)	PO	74	ddr3_addr[6]
(+)	PO	66	o_uart0_rx
(+)	PO	67	o_uart0_cts
(+)	PO	68	o_uart1_rx
(+)	PO	69	o_uart1_cts
(+)	PO	70	ddr3_addr[12]
(+)	PO	71	ddr3_addr[11]
(+)	PO	72	ddr3_addr[10]
(+)	PO	73	ddr3_addr[9]
(+)	PO	74	ddr3_addr[8]
(+)	PO	75	ddr3_addr[7]
(+)	PO	76	ddr3_addr[6]

Support Size

Figure-7 Snapshot of Mapping Manager for Part-B