**LAB # 01**

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Class: EE 382M Verification of Digital Systems

# PART A:

1. A brief report describing the netlist bugs and your solution.

**Bug # 1:** mem_read_data_r_reg[6]

i_clk was negated before being fed into the dff. I changed that to be a positive input.

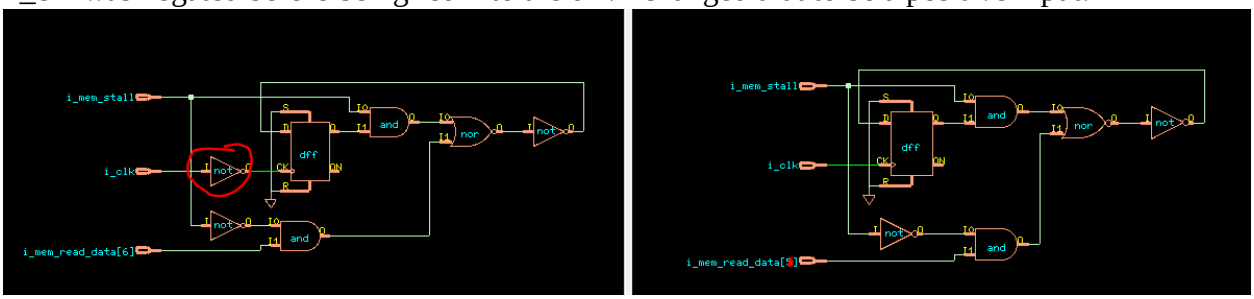


*Figure-1 mem_read_data_r_reg[6] before and after the fix*

**Bug # 2:** mem_read_data_r_reg[2]

The MUX inputs A and B were swapped. Flipping the two inputs give us the correct result.
Previous_implementation:
MUX2X1 U174 ( .B(o_wb_read_data[2]), .A(i_mem_read_data[2]), .S(i_mem_stall), .Y(n131) );
Corrected_implementation:
MUX2X1 U174 ( .B(i_mem_read_data[2]), .A(o_wb_read_data[2]), .S(i_mem_stall), .Y(n131) );

**Bug # 3:** mem_load_rd_r_reg[10]
Removed the additional NOT gate in the netlist

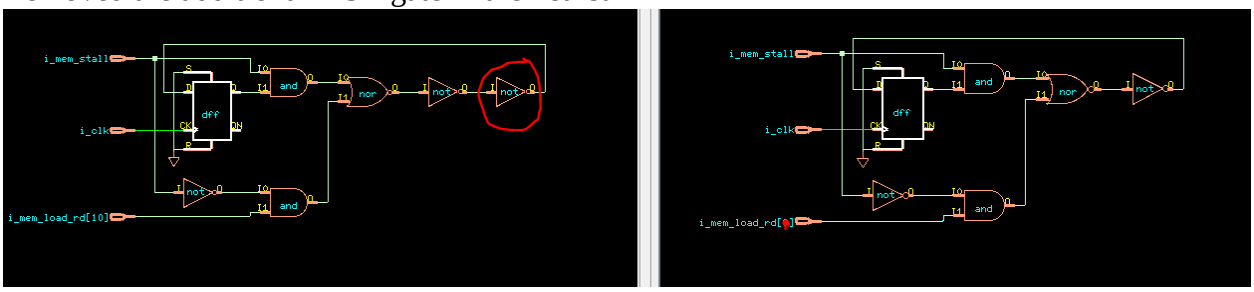


*Figure-2* mem_load_rd_r_reg[10] *before and after the fix*

2. Final snapshot of the mapping manager and lec console.

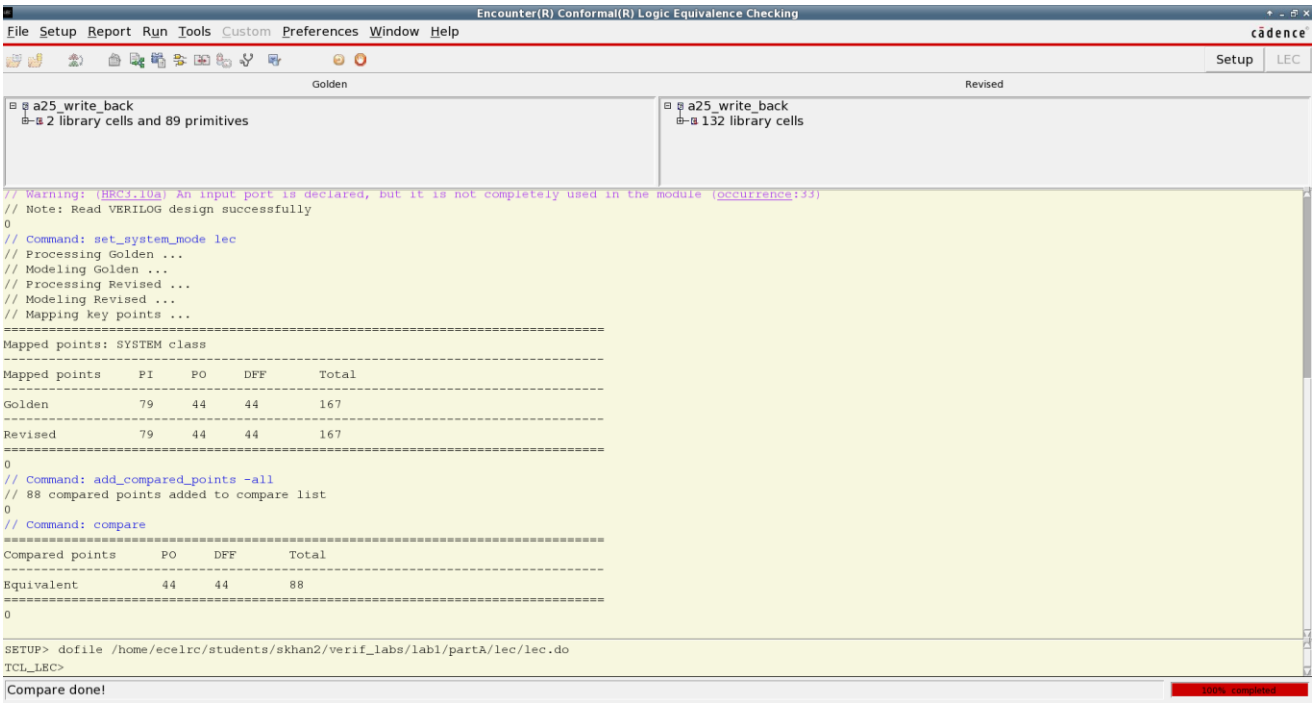


*Figure-3 Snapshot of LEC console for Part-A*

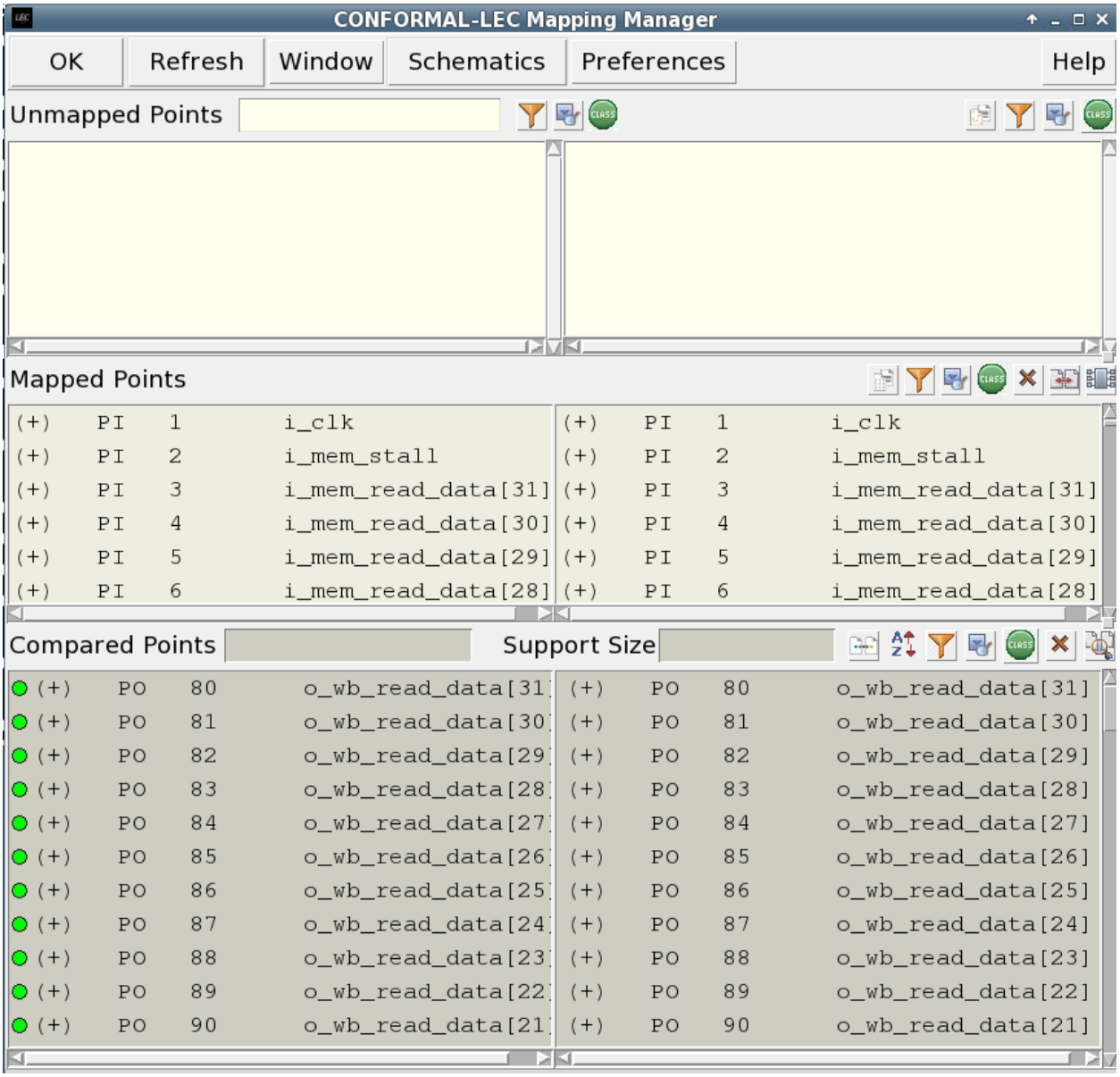


*Figure-4 Snapshot of Mapping Manager for Part-A*

## PART B:

1. Brief description of the scan structure of the SoC.

The scan insertion replaces normal flops with special scan flops that allows us to monitor and control the state of the design using specific ports. It uses the Automatic Test Pattern Generator (ATPG) tool to generate tests for improved fault coverage testing.

The scan structure of the SoC using in this lab includes:

- Minimum number of scan chains set to 4
- Maximum length of scan chains: no_value
- Lock-up element type: preferred_level_sensitive
- Mix clock edges in scan chain: true
- Prefix for unnamed scan objects: DFT_

2. The schematic of a clock gating cell in the netlist. (Search for the module with name 'RC_CG_MOD' in the netlist.

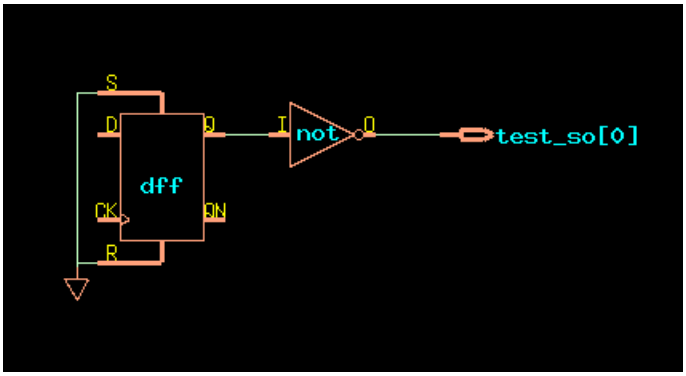


*Figure-5 Snapshot of schematic for test_so[0]*

3. What is the significance of the following commands in the lec.do file?

set_flatten_model -seq_constant -seq_constant_x_to 0:

- Set_flatten_model command is used to specify the conditions for circuit flattening.
- -seq_constant options is used for instance to convert a flop or latch to 0 or 1
- -seq_constant_x_to 0

set_flatten_model -gated_clock

- -gated_clock the synthesis tool adds clock gating for dynamic power optimization. This can cause issues while performing equivalence checking. "gated_clock" option resolves this problem by remodeling the revised clock gates to the golden model logic.

set_analyze_option -auto
Automatically sets the option for analyzing to on /off

4. Final snapshot of the mapping manager and lec console.

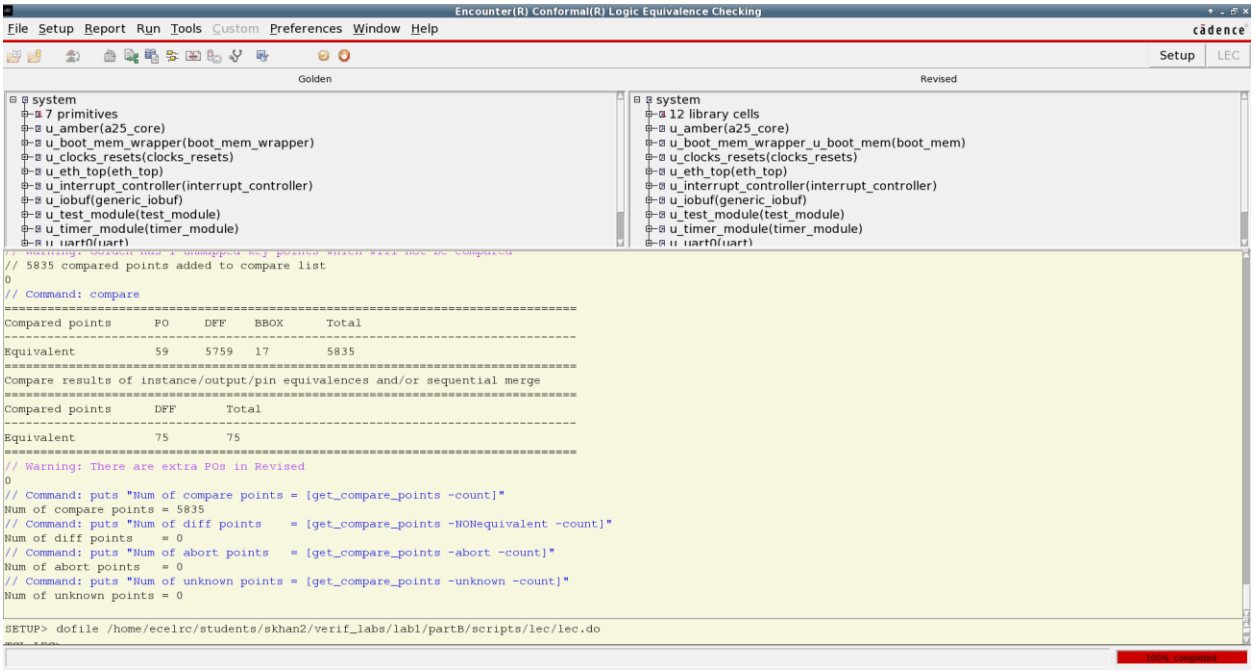


*Figure-6 Snapshot of LEC console for Part-B*

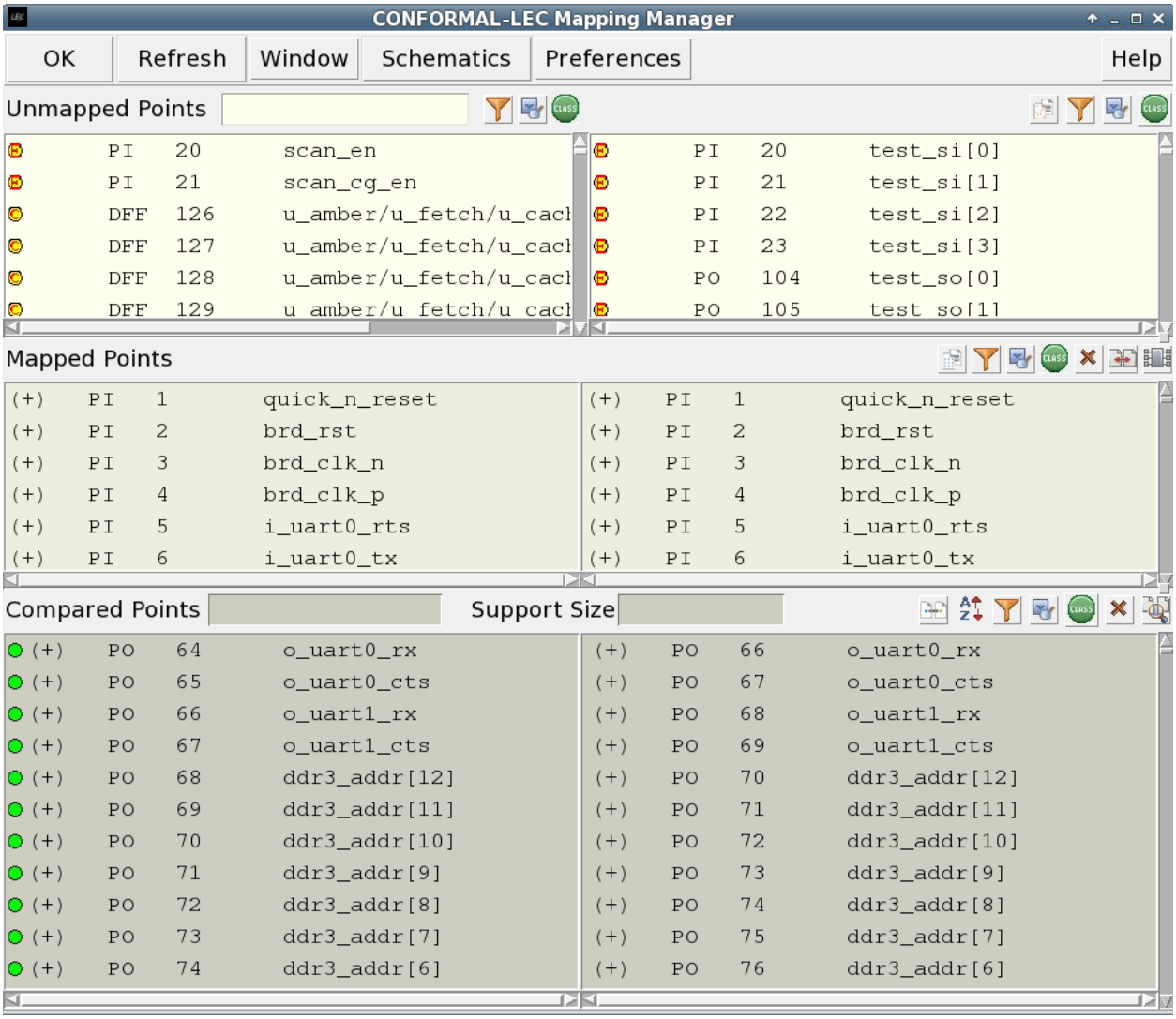


*Figure-7 Snapshot of Mapping Manager for Part-B*