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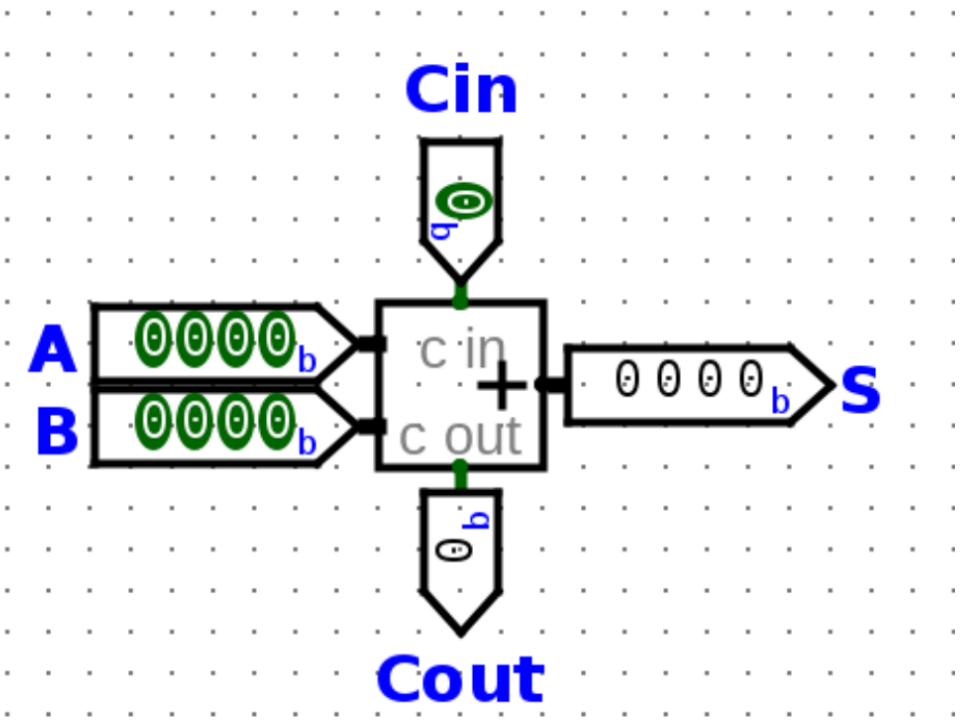
Experiment 3 Post Lab

1. Results of 10 4-bit Additions

A	B	C in	C out	S
0001	1001	1	0	1011
0010	0110	0	0	1000
0011	1111	0	1	0010
0100	1000	0	0	1100
0101	0010	0	0	0111
0111	1000	0	0	1111
1000	0101	0	0	1101
1001	0100	1	0	1110
1010	1010	0	1	0100
1011	0001	0	0	1100

1. Circuit Diagram of the IC chip



2. Results of 5 2-bit additions, and 5 2-bit subtractions

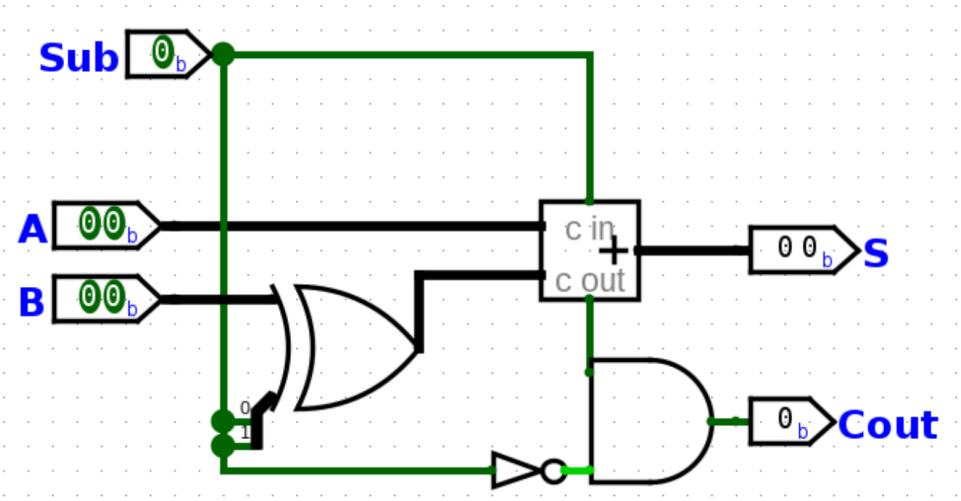
addition

A	B	Sub	C out	S
00	10	0	0	10
01	01	0	0	10
11	01	0	1	00
11	00	0	1	10
00	11	0	0	11

subtraction

A	B	Sub	C out	S
11	10	1	0	01
10	01	1	0	01
01	01	1	0	00
00	01	1	0	11
11	01	1	0	10

2. Circuit Diagram of the 2-bit Adder/Subtractor



3. Truth Table of 0 through 19 for the BCD Adder

A	B	Decimal	BCD Value
0000	0000	0	0000 0000
0000	0001	1	0000 0001
0000	0010	2	0000 0010
0000	0011	3	0000 0011
0000	0100	4	0000 0100
0000	0101	5	0000 0101
0000	0110	6	0000 0110
0000	0111	7	0000 0111
0000	1000	8	0000 1000
0000	1001	9	0000 1001
0000	1010	10	0001 0000
0000	1011	11	0001 0001
0000	1100	12	0001 0010
0000	1101	13	0001 0011
0000	1110	14	0001 0100
0000	1111	15	0001 0101
0001	0000	16	0001 0110
0001	0001	17	0001 0111
0001	0010	18	0001 1000
0001	0011	19	0001 1001

3. Circuit Diagram of the BCD Adder