THE UNIVERSITY OF TEXAS AT DALLAS

CS4341 Digital Logic & Computer Design

Lecture Notes 17

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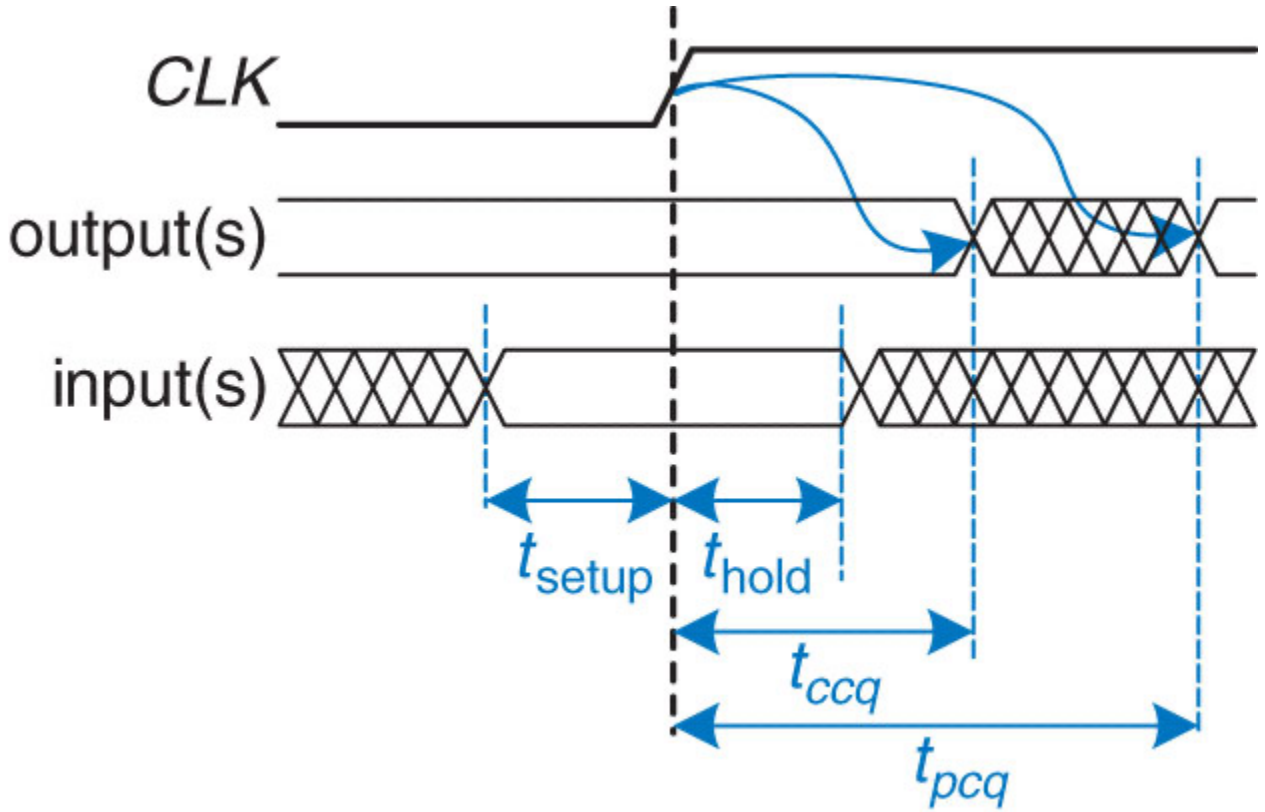
Timing in Sequential Logic

- As discussed before, in flip-flops, the process of copying the input D to the output Q (sampling) happens at the rising-edge of the clock.
- It is assumed that D is stable at that sampling time (either 1 or 0).
- A challenge happens if D changes (or not stable enough) at the time of sampling (at the rising edge of the clock)
- As well, sometimes, the clock signal itself does not reach all flip-flops at the same time, known as clock skew.
- All these issues are addressed through special design considerations and concepts.

The Dynamic Discipline

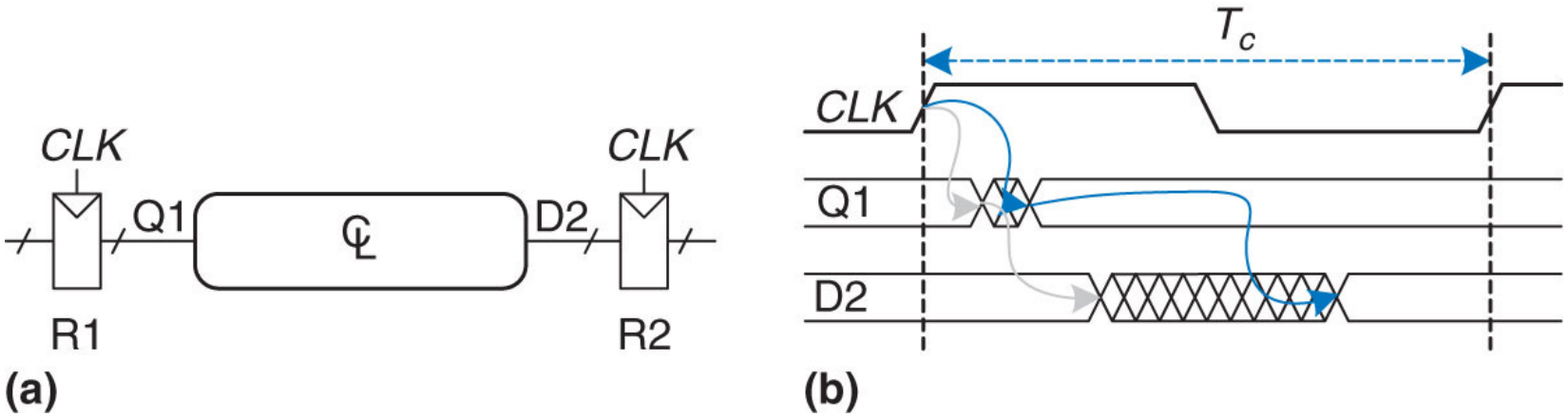
- A synchronous sequential circuit has timing specification defined by:
  - t_{ccq} (clock-to-Q contamination delay): the shortest time when the output starts changing in response to the rising edge of the clock.
  - t_{pcq} (clock-to-Q propagation delay): the longest time allowed before the Q settles to the final value.
- To sample the input value D properly, the input must be stabilized at least:
  - t_{setup}: minimum time the input(s) is stable before the clock rising edge
  - t_{hold}: minimum time the input(s) is stable after the clock rising edge
- The sum of both is called aperture time.
- The dynamic discipline: inputs of a synchronous sequential circuit must be stable during the setup and hold aperture time around the clock edge

The Dynamic Discipline



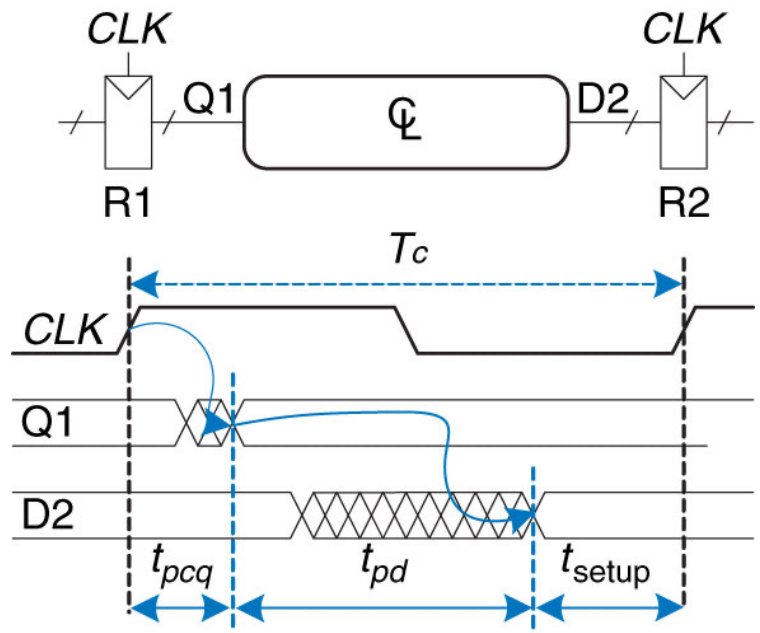
System Timing

- We start with some definitions
  - T_c (cycle/clock time): is the time between rising edges of a repetitive clock signal.
  - $f_c = 1/T_c$ is the clock frequency: increasing the clock frequency increases the work that a digital system can accomplish per unit time
- All the circuit different times need to be aligned, which we call timing constraints



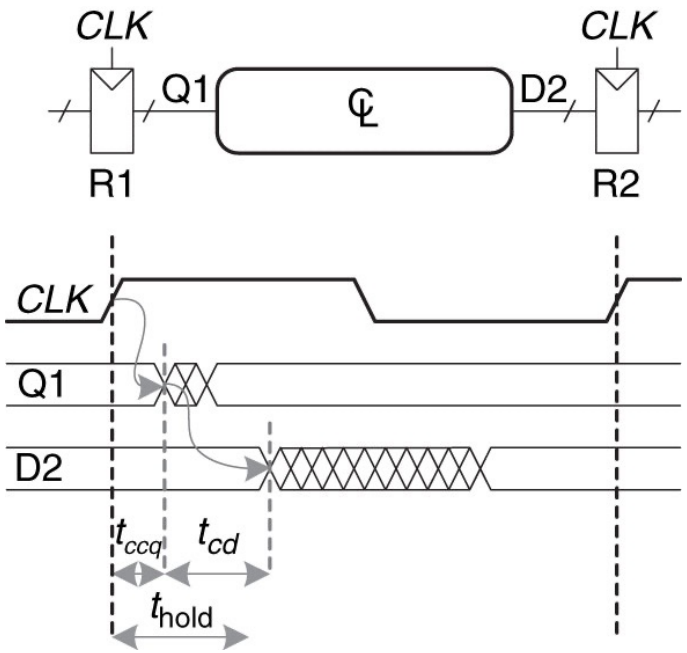
Setup Time Constraint

- Setup time for D2 is bound by the maximum delay in the path (why)?
  - To satisfy the setup time of R2, D2 must settle no later than the setup time before the next clock edge.
  - We can then define the minimum clock period T_c as:
    - $T_c \geq t_{pcq} + t_{pd} + t_{setup}$
  - $t_{pcq} + t_{setup}$ is called sequencing overhead and dictated by the manufacturer.
  - Also, T_c is usually determined by the marketing department
  - Hence, t_{pd} becomes the key parameters designers use to satisfy the time constraint equation
  - $t_{pd} \leq T_c - (t_{pcq} + t_{setup})$
  - This equation is known as setup time or max-delay constraint



Hold Time Constraint

- Hold time for D2 is bound by the minimum delay in the path (why)?
  - To satisfy the hold time of R2, D2 must stay stable at least the hold time after the next clock edge.
  - We can then define: $t_{ccq} + t_{cd} \geq t_{hold}$
  - t_{ccq} and t_{hold} are dictated by the manufacturer.
  - Hence, t_{cd} becomes the key parameters designers use to satisfy the time constraint equation
  - $t_{cd} \geq t_{hold} - t_{ccq}$
  - This equation is known as hold time or min-delay constraint



To Do List

- Review lecture notes
- Continue working on assignment 2