THE UNIVERSITY OF TEXAS AT DALLAS

CS4341 Digital Logic & Computer Design

Setup/Hold Time Special Lecture

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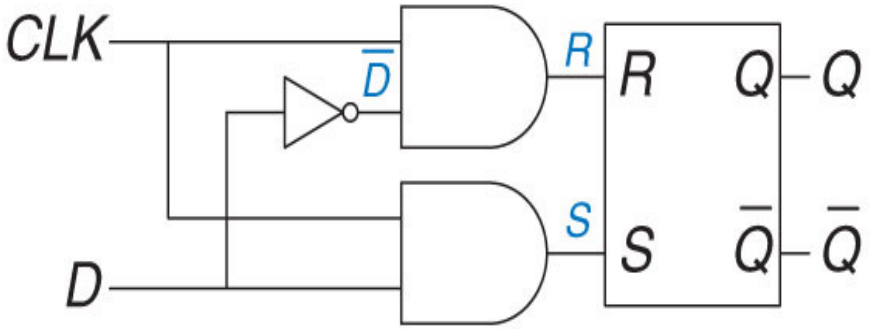
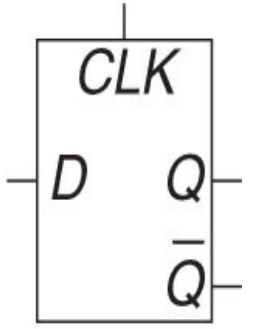
Why Do Flip-Flops Need Setup/Hold Times?

- In previous lectures we discussed the setup and hold times intuitively using the D flip-flop abstraction representation.
- To better understand the setup and hold times in detail, we need to go one or more levels down of abstractions



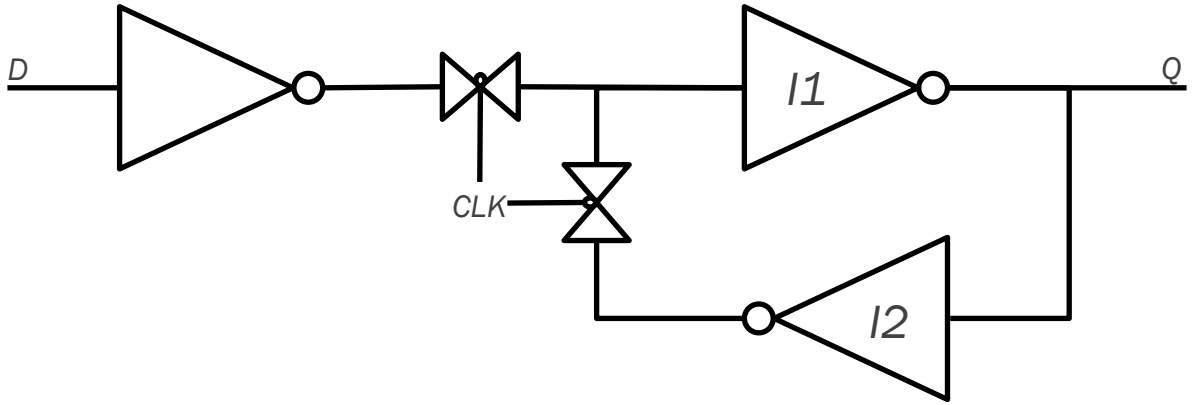
CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0



- Recall when CLK is 0, the D latch is in memory state, otherwise, Q equals the value of D. In other words, CLK is acting like a switching gate.

Simplified Representation of the D Latch

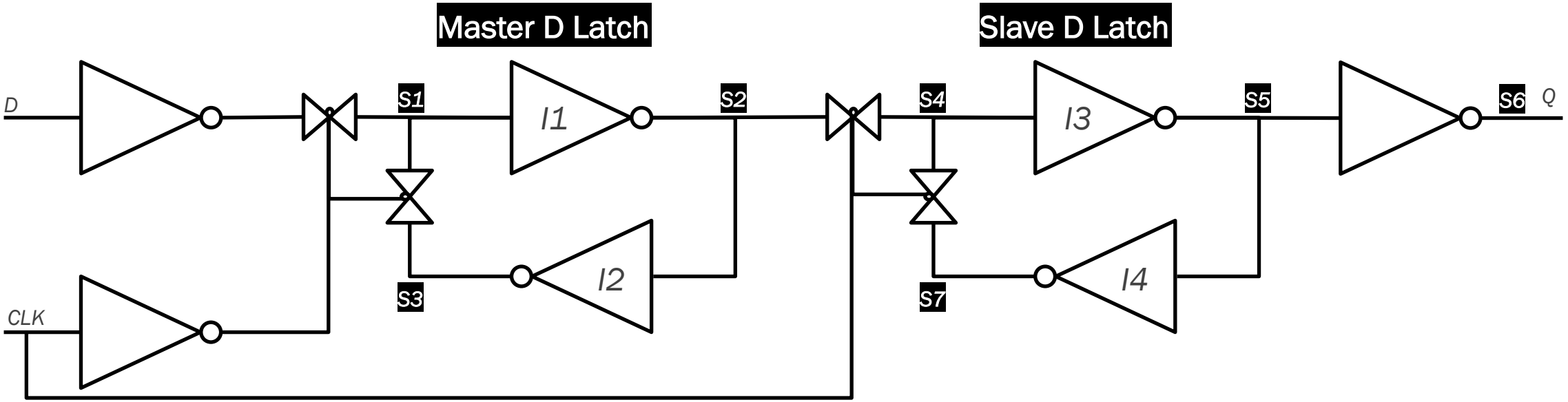
- We can then re-draw the D-Latch diagram to be as below.



- When CLK is 0, then D signal is blocked, and the circuit is in memory state (latching). When CLK is 1, the loop path is cut, and D signal is propagated to the output Q through I1

D Flip-Flop Representation

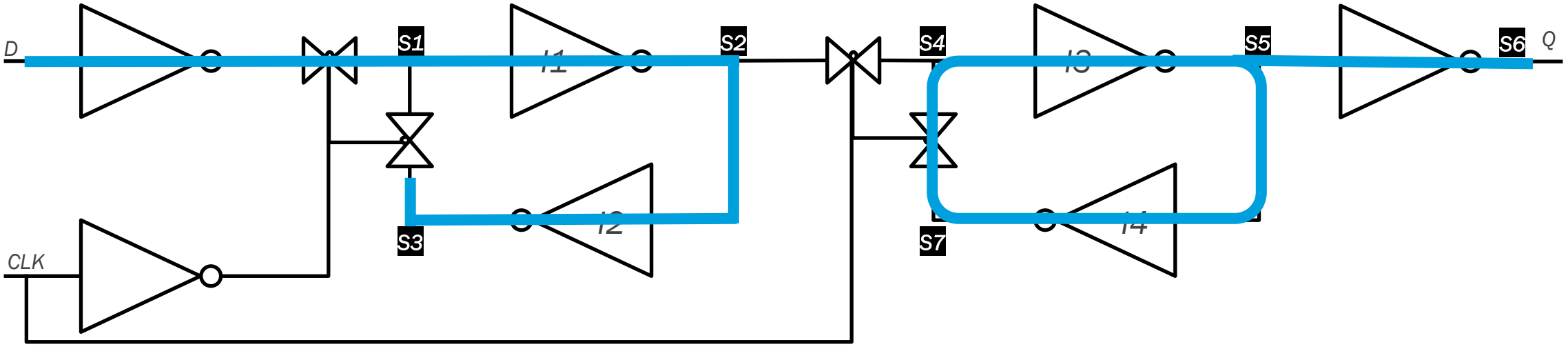
- It follows then the D Flop-Flop representation to be as follows



- When CLK is 0, then D feeds into the first latch, while the second latch is in memory state. When CLK is 1, first latch goes into memory state (latching), and that stored value is then propagated to the output Q through I3

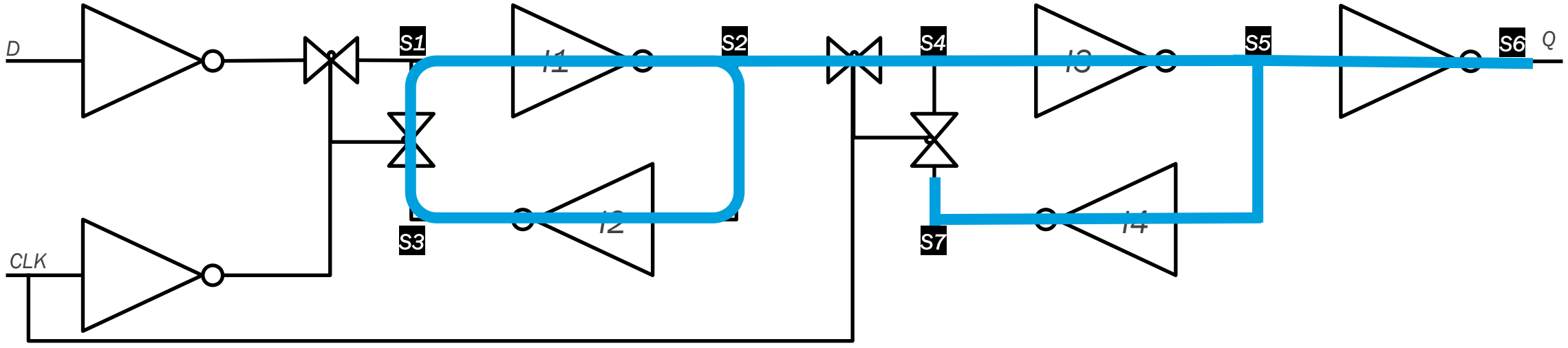
Circuit Different States – CLK 0

- When CLK is 0, The signals in the circuit look as follows



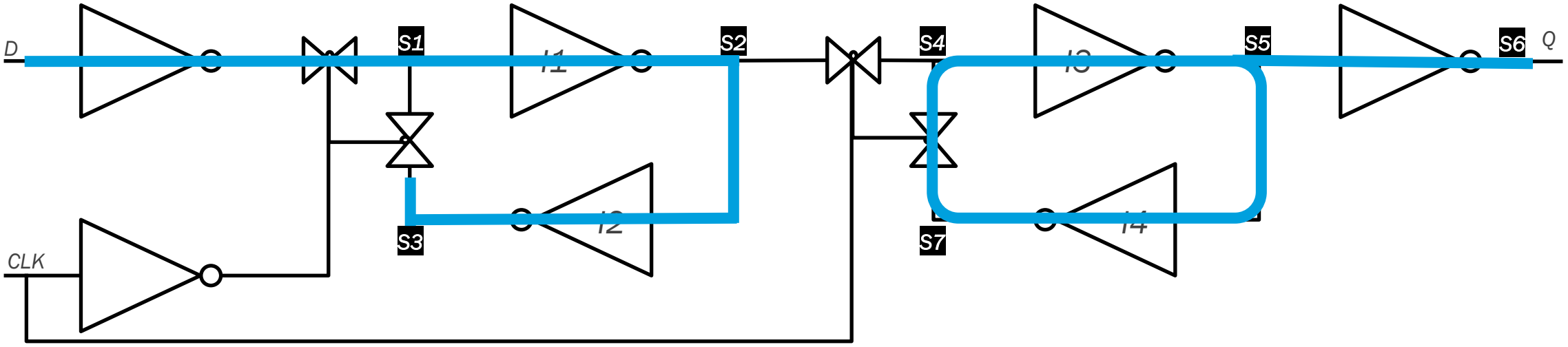
Circuit Different States – CLK 0 ➔ 1

- When CLK changes to 1, The signals in the circuit look as follows



Setup Time and the Need for It

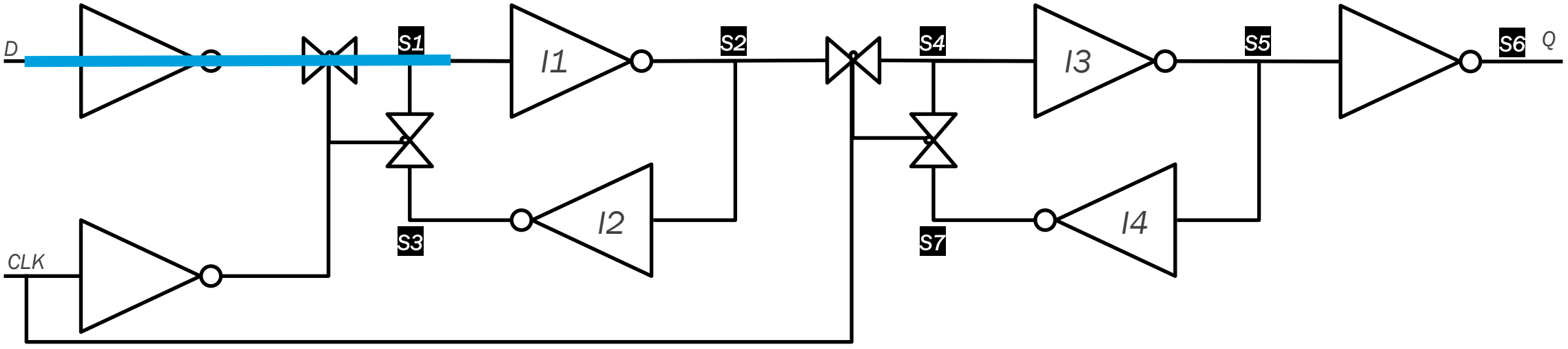
- Setup time is the minimum time the input signal must be stable to be correctly latched (at the CLK rising edge)
- It equals the time **needed** for signal D to travel through the path D ➔ S1 ➔ S2 ➔ S3



The Risk of Violating The Setup Time

Hold Time and the Need for It

- Hold time is the minimum time the input signal must be stable after the clock rising edge.
- It equals the time it take for the Input gate (inverted CLK) to fully shutdown (D is unchanged at S1 until the gate is fully closed)



The Risk of Violating The Hold Time

- The risk is that D value can be altered before the gate is fully closed.