12.) What is the smallest (most negative) 32-bit binary number that can be represented with

(a) unsigned numbers?

0

(b) two's complement numbers?

- (2^{31})

(c) sign/magnitude numbers?

- $(2^{31} – 1)$

16.) Convert the following unsigned binary numbers to hexadecimal. Show your work.

(c) 11010111_2

1101 0111

D 7

$(D7)_{16}$

(d) 011101010100100_2

0011 1010 1010 0100

3 A A 4

$(3AA4)_{16}$

18.) Convert the following hexadecimal numbers to decimal. Show your work.

(c) $ED3A_{16}$

E D 3 A

$(14 \times 16^3) + (13 \times 16^2) + (3 \times 16^1) + (10 \times 16^0)$

$(60730)_{10}$

(d) $403FB001_{16}$

4 0 3 F B 0 0 1

$(4 \times 16^7) + (0 \times 16^6) + (3 \times 16^5) + (15 \times 16^4) + (11 \times 16^3) + (0 \times 16^2) + (0 \times 16^1) + (1 \times 16^0)$

$(1077915649)_{10}$

20.) Convert the following hexadecimal numbers to decimal. Show your work.

(d) $403FB001_{16}$

0100 0000 0011 1111 1011 0000 0000 0001

$(0100\ 0000\ 0011\ 1111\ 1011\ 0000\ 0000\ 0001)_2$

22.) Convert the following two's complement binary numbers to decimal.

(c) 01001110_2

0100 1110

$(4 \times 16^1) + (14 \times 16^0)$

$(78)_{10}$

(d) 10110101_2

10110101

(-) 0100 1011

(-) $(4 \times 16^1) + (10 \times 16^0)$

$(-75)_{10}$

(24) Convert the following sign/magnitude binary numbers to decimal.

(d) 10110101_2

(-) 0011 0101

(-) $(3 \times 16^1) + (5 \times 16^0)$

$(-53)_{10}$

(30) Convert the following decimal numbers to 8-bit two’s complement numbers or indicate that the decimal number would overflow the range.

(c) 128_{10}

$128 > (2^7 – 1)$

Overflow

(d) $−150_{10}$

$-150 < (- 2^7)$

Overflow

(e) 127_{10}

127/2 = 63 r 1

63/2 = 31 r 1

31/2 = 15 r 1

15/2 = 7 r 1

7/2 = 3 r 1

3/2 = 1 r 1

1/2 = 0 r 1

$(01111111)_2$

40.) Convert each of the following octal numbers to binary, hexadecimal, and decimal.

(d) 2560_8

2 5 6 0

010 101 110 000

$(010101110000)_2$

0101 0111 0000 *using the found binary to find hexadecimal

5 7 0

$(570)_{16}$

$(5 \times 16^2) + (7 \times 16^1) + (7 \times 16^0)$ *using the found hexadecimal to find decimal

$(1392)_{10}$

42.) How many 7-bit two's complement numbers are greater than 0? How many are less than 0? How would your answers differ for sign/magnitude numbers?

There are $2^6 – 1$, or 63, numbers greater than 0; while there are 2^6, or 64, numbers less than 0. However, had the answer followed the method of sign/magnitude numbers, there would instead be 63 numbers less than 0; this is a result there being two zeroes by following the sign/magnitude method.

56.) Convert the following decimal numbers to 6-bit two's complement binary numbers and add them. Indicate whether or not the sum overflows a 6-bit result.

(b) $27_{10} + 31_{10}$

011011 + 011111

111010 or -6

Overflow

(d) $3_{10} + −32_{10}$

000011 + 100000

100011 or -29

(e) $−16_{10} + −9_{10}$

110000 + 110111

100111 or -25

(f) $−27_{10} + −31_{10}$

100101 + 100001

000110 or 6

Overflow

73.) A majority gate produces a TRUE output if and only if more than half of its inputs are TRUE. Complete a truth table for the three-input majority gate shown in Figure 1.41.

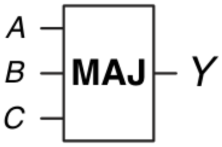
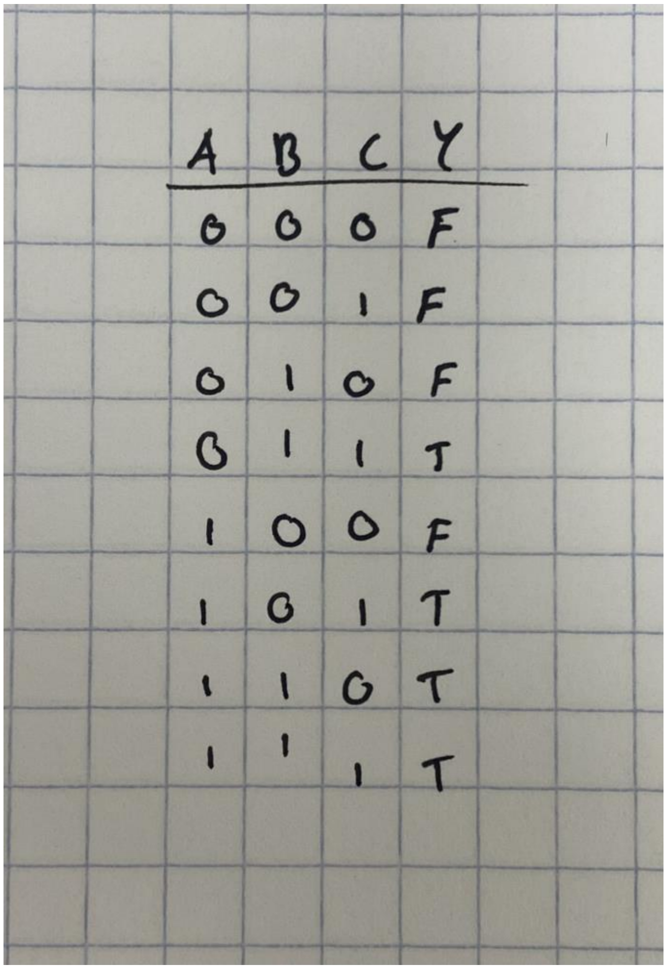


Figure 1.41 Three-input majority gate



A	B	C	Y
0	0	0	F
0	0	1	F
0	1	0	F
0	1	1	T
1	0	0	F
1	0	1	T
1	1	0	T
1	1	1	T

74.) A three-input AND-OR (AO) gate shown in Figure 1.42 produces a TRUE output if both A and B are TRUE, or if C is TRUE. Complete a truth table for the gate.

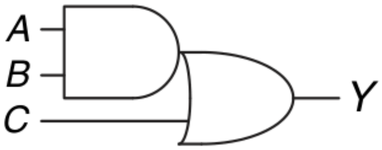
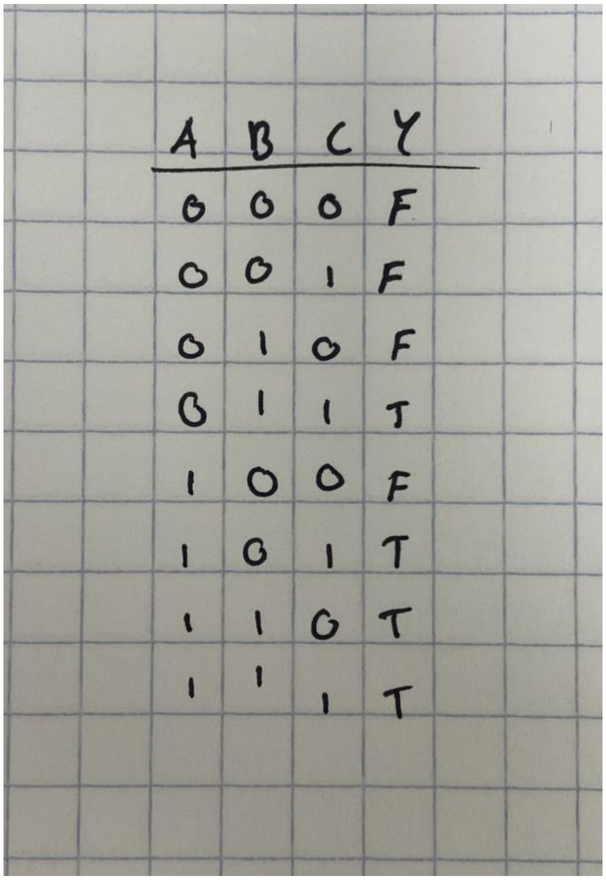


Figure 1.42 **Three-input AND-OR gate**



A	B	C	Y
0	0	0	F
0	0	1	F
0	1	0	F
0	1	1	T
1	0	0	F
1	0	1	T
1	1	0	T
1	1	1	T

82.) While walking down a dark alley, Ben Bitdiddle encounters a two-input gate with the transfer function shown in Figure 1.48. The inputs are A and B and the output is Y.

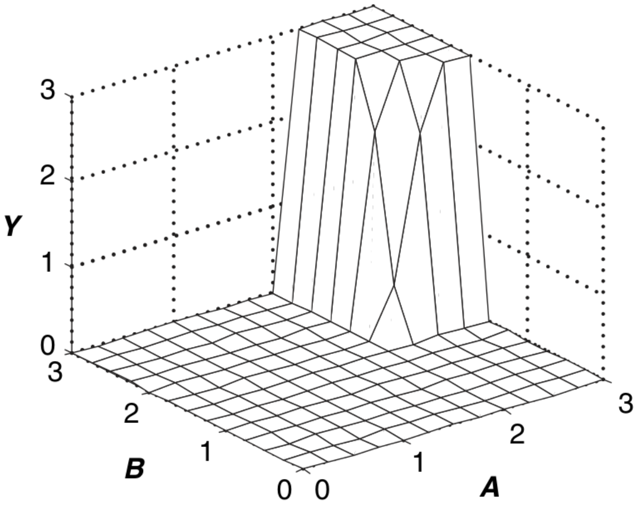
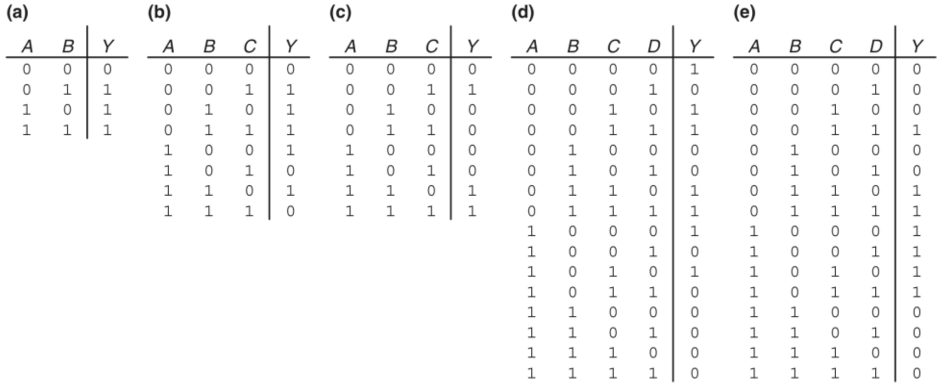


Figure 1.48 Two-input DC transfer characteristics

(a) What kind of logic gate did he find?

(b) What are the approximate high and low logic levels?

2.) Write a Boolean equation in product-of-sums canonical form for the truth tables in Figure 2.81.



(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(c)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(d)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(e)

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 2.81 **Truth tables for Exercises 2.2 and 2.4**

(a) F = A + B

(b) F = (A + B + C) (A’ + B + C’) (A’ + B’ + C’)

(c) F = (A + B + C) (A + B’ + C) (A + B’ + C’) (A’ + B + C) (A’ + B + C’)

(d) F = (A + B + C + D’) (A + B’ + C + D) (A + B’ + C + D’) (A’ + B + C + D’) (A’ + B + C’ + D’) (A’ + B’ + zC + D) (A’ + B’ + C + D’) (A’ + B’ + C’ + D) (A’ + B’ + C’ + D’)

(e) F = (A + B + C + D) (A + B + C + D’) (A + B + C’ + D) (A + B’ + C + D) (A + B’ + C + D’) (A’ + B’ + C + D) (A’ + B’ + C + D’) (A’ + B’ + C’ + D) (A’ + B’ + C’ + D’)

6.) Minimize each of the Boolean equations from Exercise 2.2.

(a) F = A + B

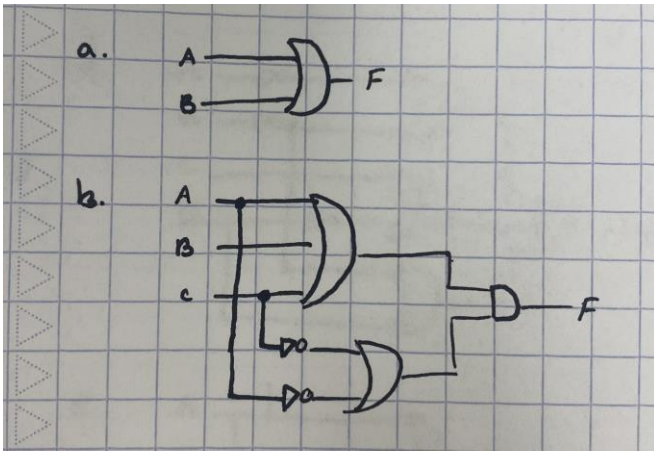
(b) F = (A + B + C) (A’ + C’)

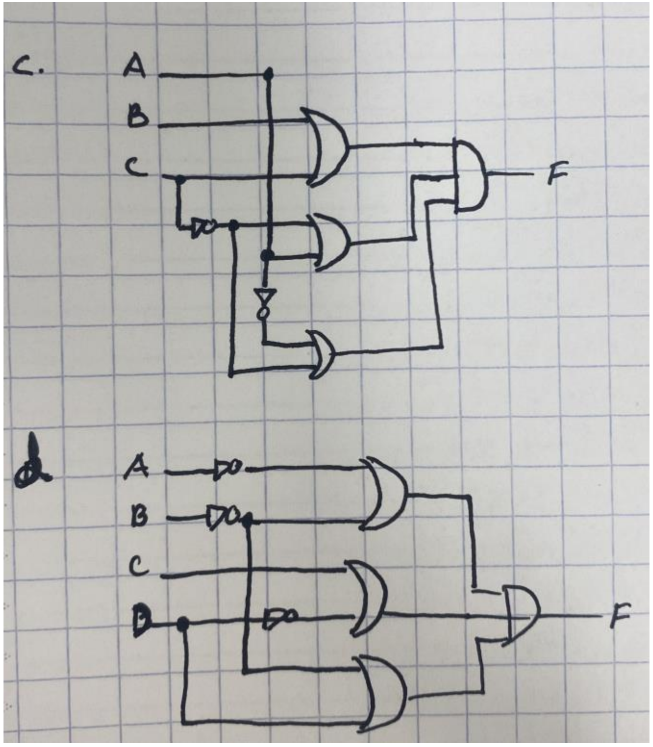
(c) F = (B + C) (A + C’) (A’ + C’)

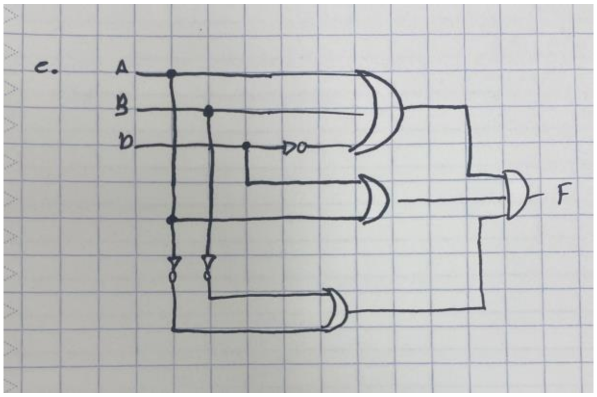
(d) F = (A’ + B’) (C + D’) (B’ + D)

(e) F = (A’ + B’) (A + D) (A + B + D‘)

8.) Sketch a reasonably simple combinational circuit implementing each of the functions from Exercise 2.6.







12.) Repeat Exercise 2.8 using only NOT gates and NAND and NOR gates.

14.) Simplify the following Boolean equations using Boolean theorems. Check for correctness using a truth table or K-map.

(a) $Y = \overline{A}BC + \overline{A}B\overline{C}$

(b) $Y = \overline{ABC} + A\overline{B}$

(c) $Y = ABC\overline{D} + A\overline{BCD} + (\overline{A + B + C + D})$

(a)

Y = A’B(C + C’)

Y = A’B(1)

Y = A’B

(b)

Y = (A’ + B’ + C’) + AB’

Y = A’ + B’ + AB’ + C’

Y = A’ + B’(1 + A) + C’

Y = A’ + B’A + C’

Y = A’ + A’’B + C’

Y = A’ + B’ + C’

(c)

16.) Sketch a reasonably simple combinational circuit implementing each of the functions from Exercise 2.14.

24.) Write Boolean equations for the circuit in Figure 2.82. You need not minimize the equations.

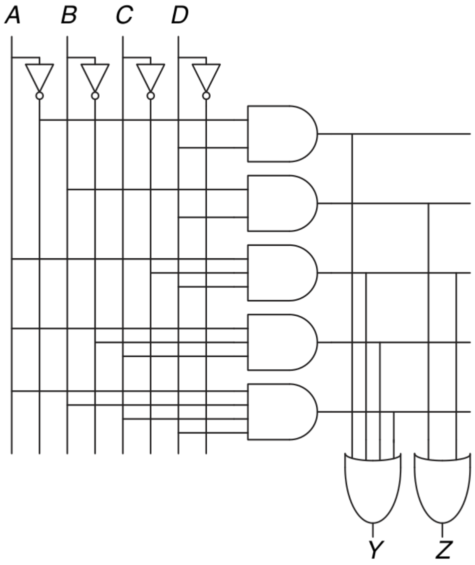


Figure 2.82 **Circuit schematic**

Y = (A’D) + (AC’D) + (AB’C) + (ABCD)

Z = (BD) + (AC’D)

26.) Using De Morgan equivalent gates and bubble pushing methods, redraw the circuit in Figure 2.83 so that you can find the Boolean equation by inspection. Write the Boolean equation.

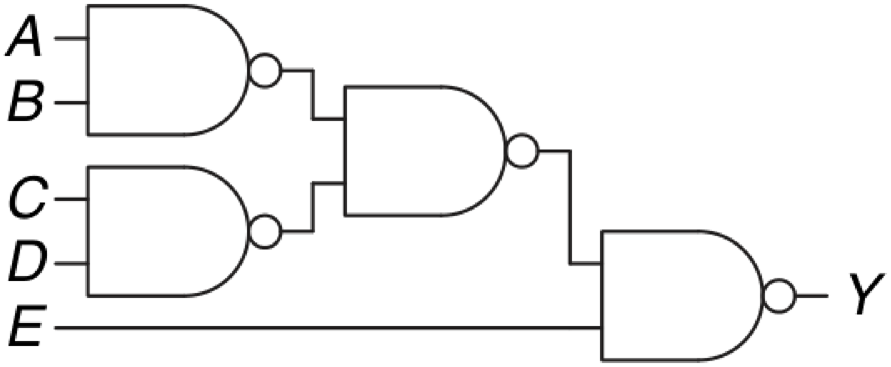
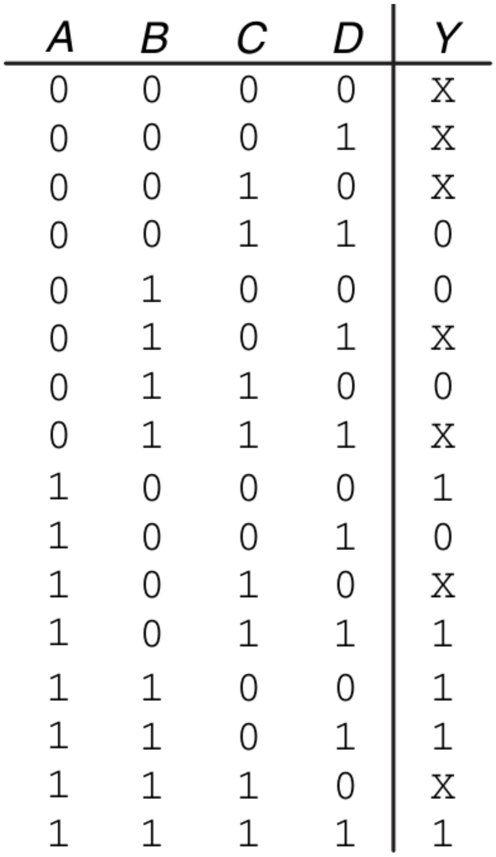


Figure 2.83 **Circuit schematic**

28.) Find a minimal Boolean equation for the function in Figure 2.85. Remember to take advantage of the don’t care entries.



A	B	C	D	Y
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

Figure 2.85 **Truth table for Exercise 2.28**

Y = (C’D’) + (AB) + (AC)

36.) A priority encoder has 2N inputs. It produces an N-bit binary output indicating the most significant bit of the input that is TRUE, or 0 if none of the inputs are TRUE. It also produces an output NONE that is TRUE if none of the inputs are TRUE. Design an eight-input priority encoder with inputs A7:0 and outputs Y2.0 and NONE. For example, if the input is 00100000, the output Y should be 101 and NONE should be 0. Give a simplified Boolean equation for each output, and sketch a schematic.

40.) Write a minimized Boolean equation for the function performed by the circuit in Figure 2.88.

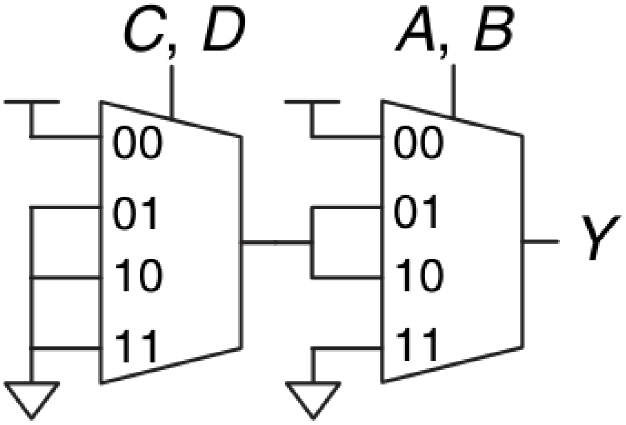


Figure 2.88 Multiplexer circuit

42.) Implement the function from Exercise 2.17(a) using

(a) an 8:1 multiplexer

(b) a 4:1 multiplexer and no other gates

44.) Determine the propagation delay and contamination delay of the circuit in Figure 2.84. Use the gate delays given in Table 2.8.

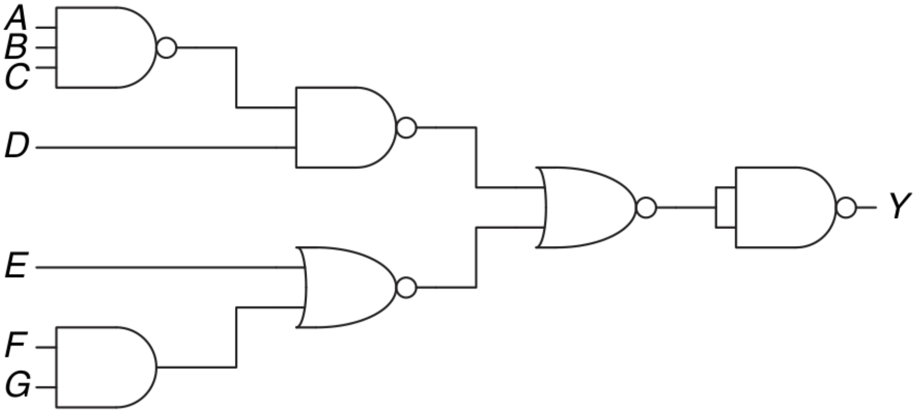


Figure 2.84 Circuit schematic

Table 2.8 Gate delays for Exercises 2.43–2.47

Gate	t_{pd} (ps)	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40