THE UNIVERSITY OF TEXAS AT DALLAS

CS4341 Digital Logic & Computer Design

Lecture Notes 14

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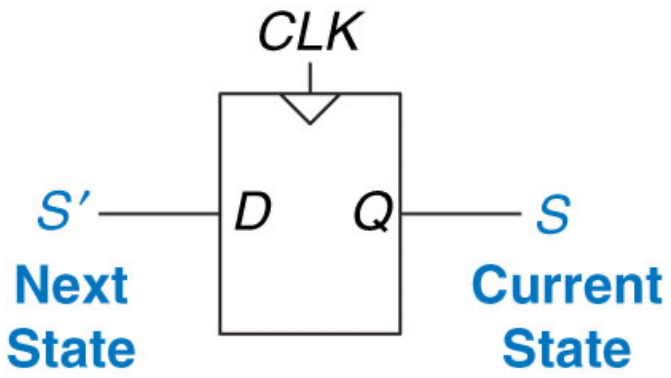
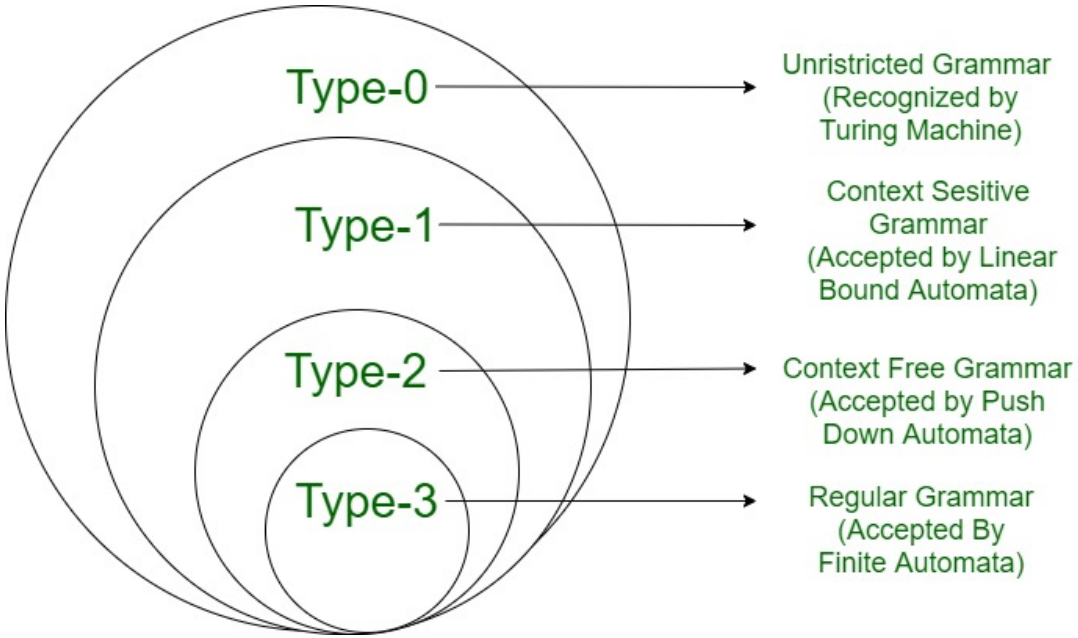
Review: Synchronous Sequential Circuits

- Synchronous sequential circuits mean:
  - Only at the rising edge of the clock, registers values along with other inputs can change “the state” of the circuit (values stored in registers).
  - There are finite number of states the circuit can be in {S_0, S_1, …, S_{k-1}}
  - Every circuit element is either a register or a combinational circuit
  - At least one circuit element is a register
  - All registers receive the same clock signal
  - Every cyclic path contains at least one register



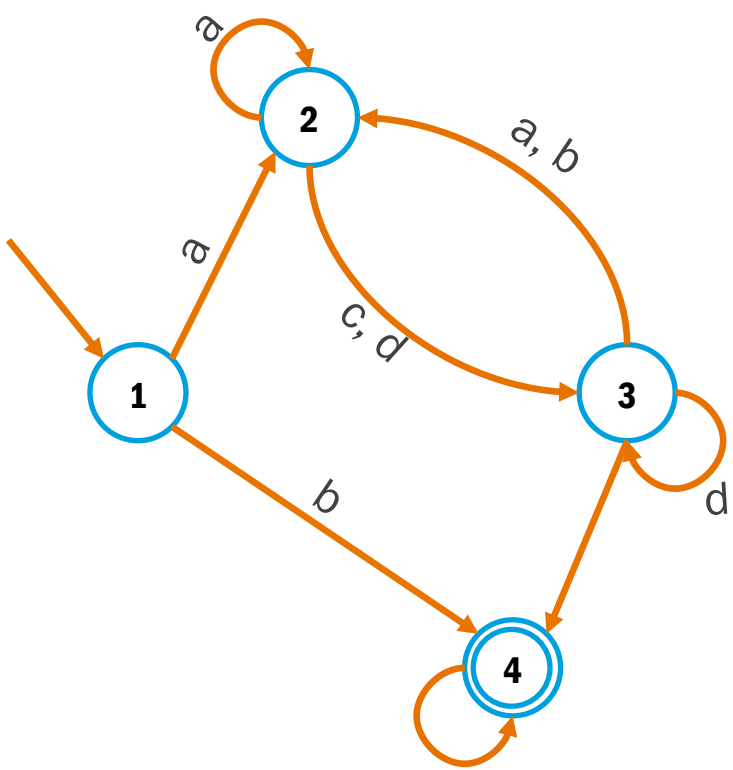
Finite State Machines

- Finite state machine is a mathematical model of computation to describe the system different states.
- FSM can be in exactly one state out of “finite” number of states at any given time.
- FSM is part of the automata theory, which deals with the logic of computation with respect to simple machines.



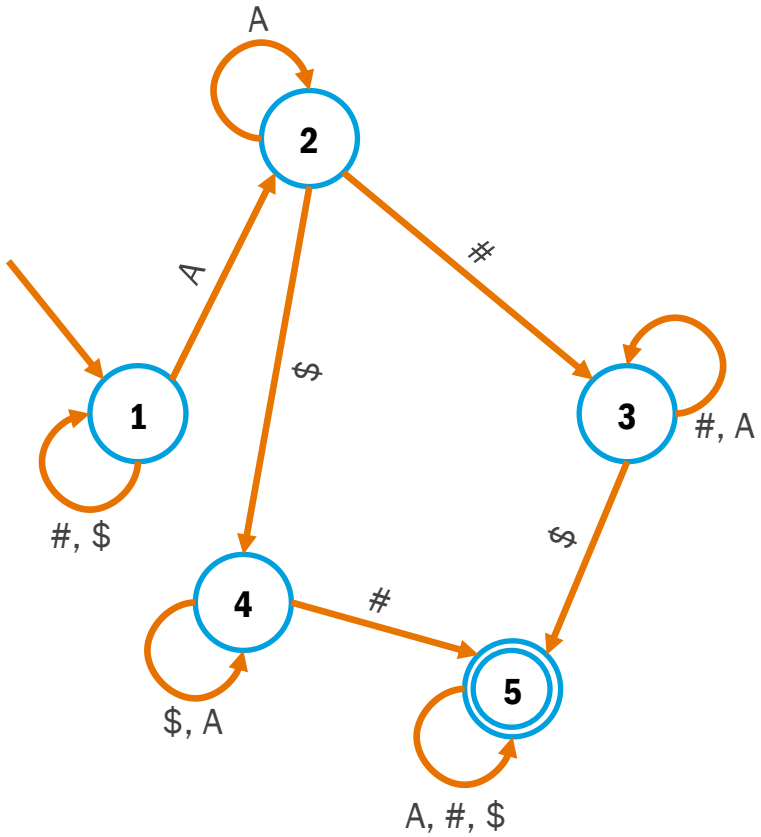
Finite State Machines

- Finite state machine is composed of a known (finite) number of states
- One of them is special and known as the start state
- It has set of transitions which determines how to move from one state to the next
- Conditions (inputs) that tells the machine how to move from one state to the next
- Accepting state (in some types of FSM)



FSM Example

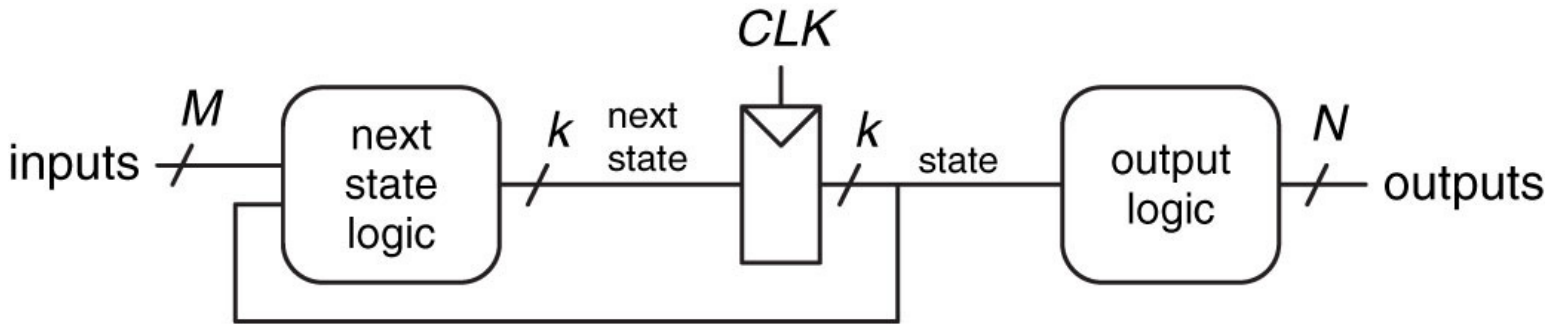
- Design an FSM that validates that a password meets the following criteria:
  - The password must have a sequence in it which:
    - Starts with an alphabet (A)
    - Has at least one number (#)
    - Has at least one symbol ($)



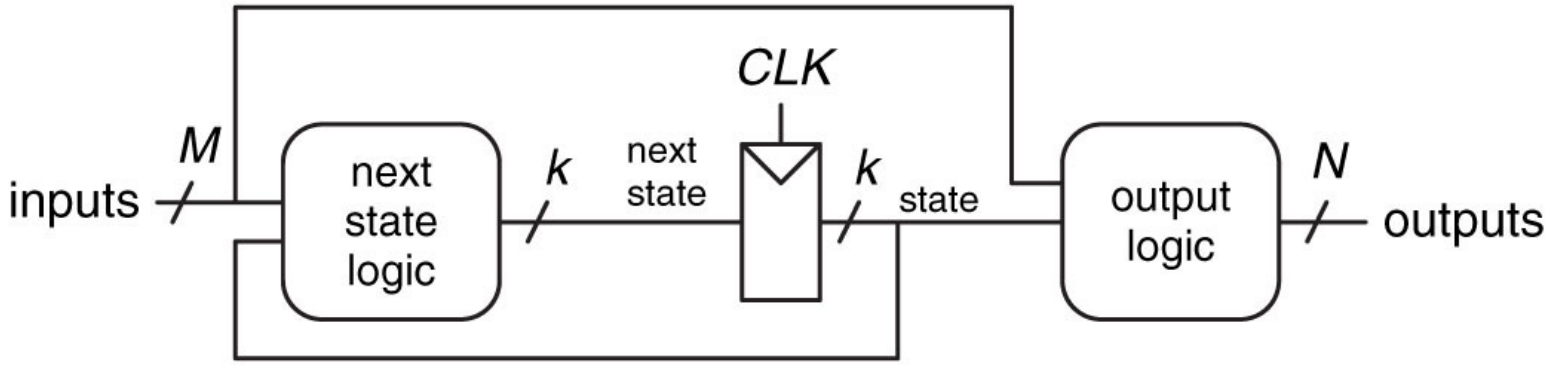
FSM Sequential Circuits Representation

- Synchronous sequential circuits can be represented in the form of finite state machines:
  - The machine has M inputs, N outputs, k registers, a clock and optionally a reset signal
  - k registers means the machine has 2^k unique states it could be in.
  - The machine can be represented using:
    - Two combinational logic blocks: next state logic and output logic
    - Register block to store the state
  - There are two classes of FSM:
    - Moore machines: output depends only on current state
    - Mealy machines: output depends on both current state and current input

FSM Sequential Circuits Representation



Moore machine



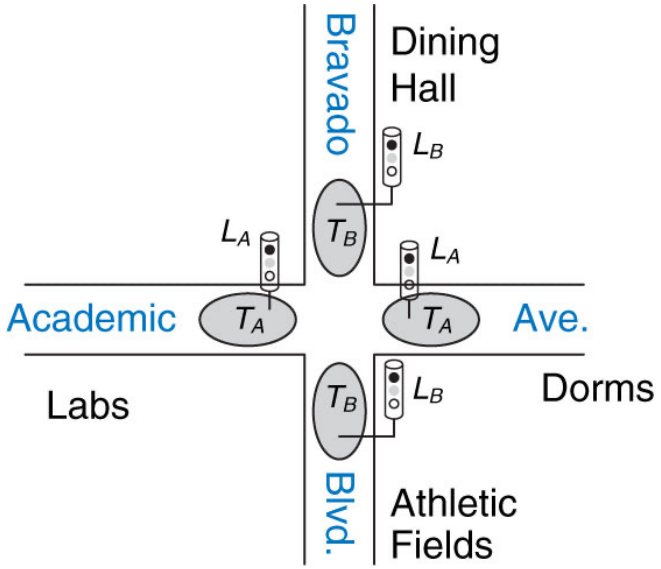
Mealy machine

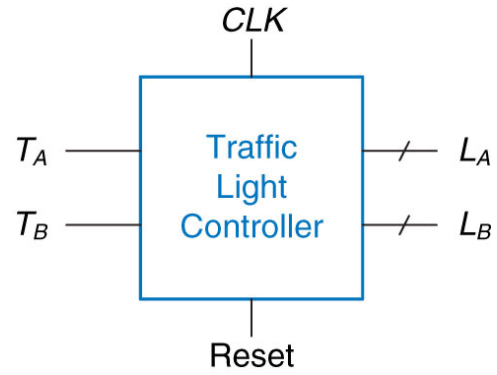
FSM Design Process

- The design of an FSM includes the following steps:
  - System level design: a high-level description of the systems including inputs, outputs and operations
  - State transition diagram: description of all the states the system can be at with the possible transitions and transition conditions.
  - Assign numbers to all the states. This is crucial because it will tell how many memory cells are needed for the system.
  - Create Truth tables
  - Design the logic using K-Map

Example: Traffic Light Design

- Design a system to control two traffic lights L_A and L_B.
- The traffic lights are connected to two sensors T_A and T_B, where each sensor is TRUE if a car is present, and FALSE if the street is empty (inputs)
- Each traffic light receives digital input specifying the color it should display: R, Y, G (outputs)
- Rule is simple: a green light stays green as long as there are cars on that street. Otherwise, it switches to the other light.
- The system is linked to a 5-second clock, where at each rising edge of the clock, the output might change based on the input and the current state.
- The system has a reset button. When pressed, it resets the outputs to L_A = Green and L_B = Red
- So, what is the system-level design looks like?

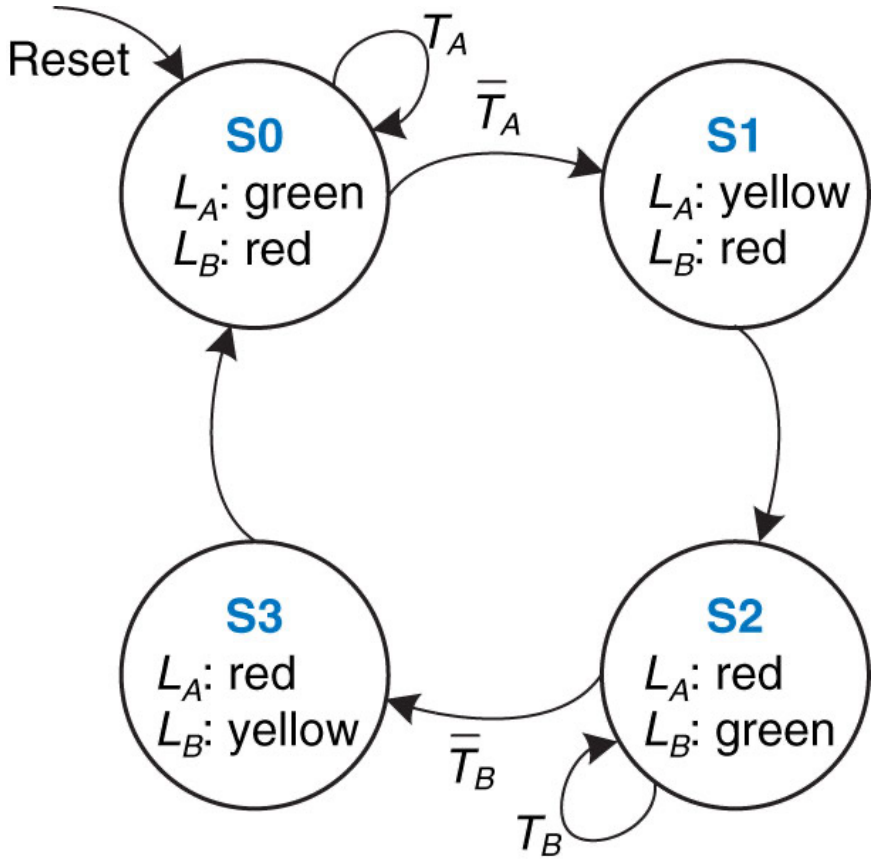




Traffic Light: State Transition Diagram

- How do we determine a state?
  - Using the different possible (legal) outputs the system produces
- How many states do we have?

State	L_A	L_B
S0	Green	Red
S1	Yellow	Red
S2	Red	Green
S3	Red	Yellow



- What are the transitioning conditions?
- How many bits of memory are needed?

To Do List

- Review lecture notes
- Study chapter 3