THE UNIVERSITY OF TEXAS AT DALLAS

CS4341 Digital Logic & Computer Design

Lecture Notes 9

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Review: Karnaugh Map (K-Map)

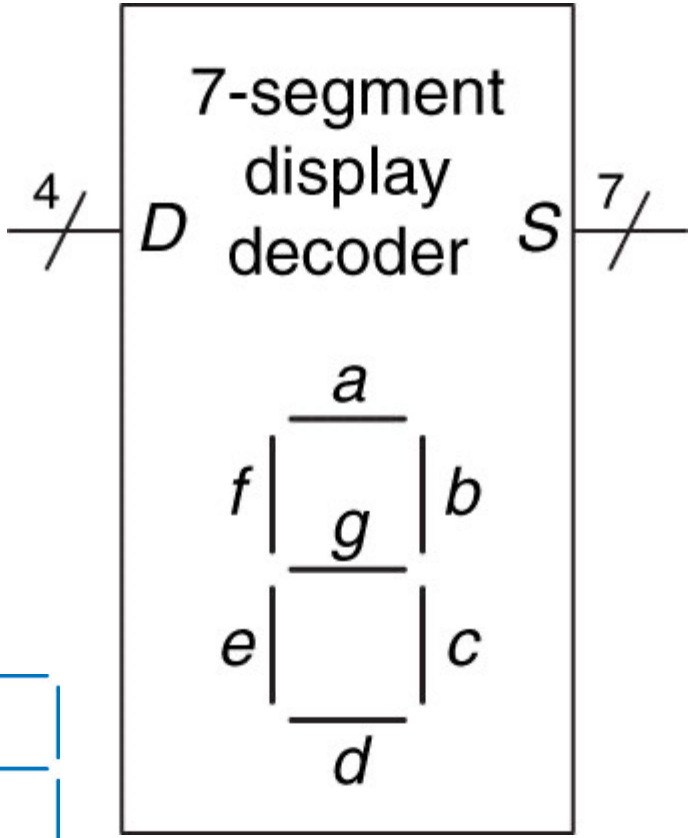
- A K-map is a diagram made of a collection of adjacent squares each representing a minterm.:
- Adjacent squares differ in the value of **one** variable only
- K-Map identifies and removes redundancies by:
  - forming largest possible 2^n squares that produce 1 (prime implicants)
  - removing ineffective literals from these prime-implicants.
- The size of the prime implicants determines the number of redundant literals that can be removed.

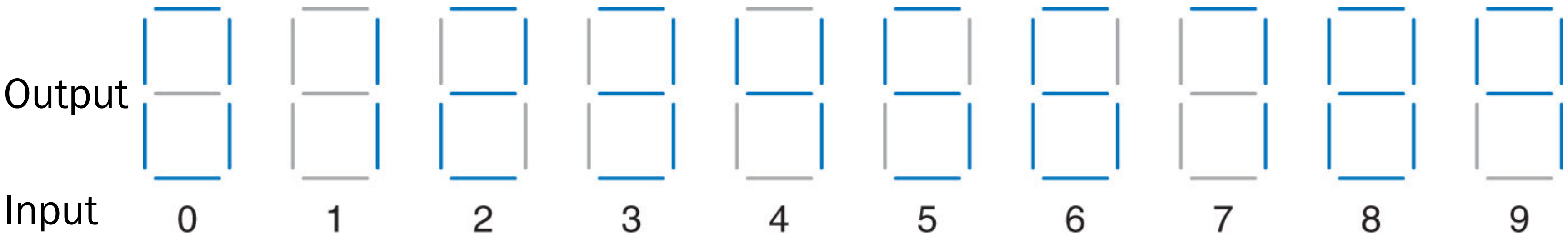
4-Variable K-Map

		$\bar{Y}$		Y		
	wx \ yz	00	01	11	10	
$\bar{W}$	00	0 $m_0 = \bar{w}\,\bar{x}\,\bar{y}\,\bar{z}$	1 $m_1 = \bar{w}\,\bar{x}\,\bar{y}\,z$	3 $m_3 = \bar{w}\,\bar{x}\,y\,z$	2 $m_2 = \bar{w}\,\bar{x}\,y\,\bar{z}$	$\bar{X}$
	01	4 $m_4 = \bar{w}\,x\,\bar{y}\,\bar{z}$	5 $m_5 = \bar{w}\,x\,\bar{y}\,z$	7 $m_7 = \bar{w}\,x\,y\,z$	6 $m_6 = \bar{w}\,x\,y\,\bar{z}$	X
W	11	12 $m_{12} = w\,x\,\bar{y}\,\bar{z}$	13 $m_{13} = w\,x\,\bar{y}\,z$	15 $m_{15} = w\,x\,y\,z$	14 $m_{14} = w\,x\,y\,\bar{z}$	
	10	8 $m_8 = w\,\bar{x}\,\bar{y}\,\bar{z}$	9 $m_9 = w\,\bar{x}\,\bar{y}\,z$	11 $m_{11} = w\,\bar{x}\,y\,z$	10 $m_{10} = w\,\bar{x}\,y\,\bar{z}$	$\bar{X}$
		$\bar{Z}$	Z		$\bar{Z}$	

Example: 7-Segment Display Decoder

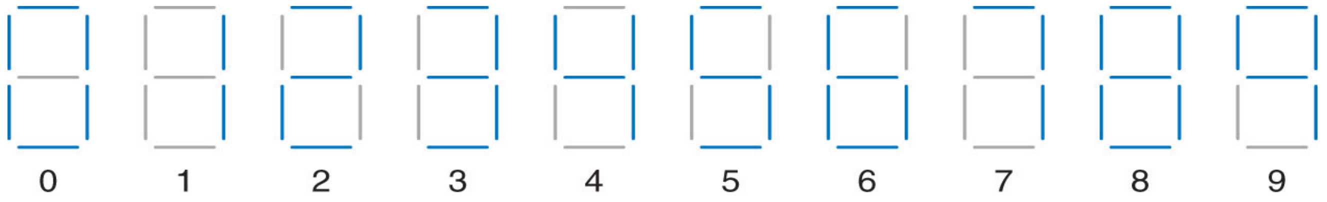
- A seven-segment display decoder takes a 4-bit data input (variables), D3:0, and produces seven outputs to control light-emitting diodes to display a digit from 0 to 9
- The seven outputs are often called segments a through g, or S_a–S_g

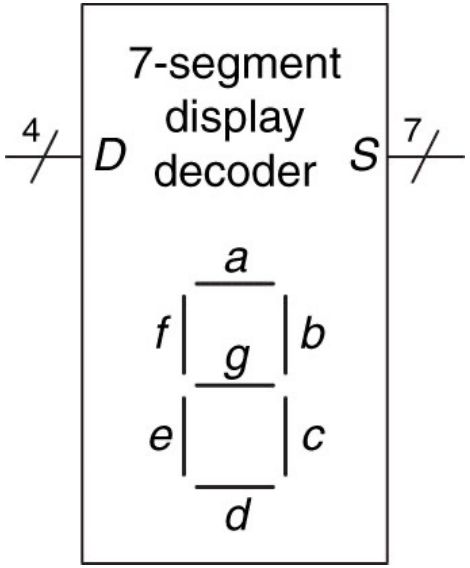




Solution Step 1: Truth Table

D_3	D_2	D_1	D_0	S_a	S_b	S_c	S_d	S_e	S_f	S_g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0





Solution Step 2: K-Map

S_a	minterm
1	m_0
0	
1	m_2
1	m_3
0	
1	m_5
1	m_6
1	m_7
1	m_8
1	m_9
0	
0	
0	
0	
0	
0	

S_a: $D_{1:0}$ \ $D_{3:2}$	00	01	11	10
00	1	0	0	1
01	0	1	0	1
11	1	1	0	0
10	1	1	0	0

S_b: $D_{1:0}$ \ $D_{3:2}$	00	01	11	10
00	1	1	0	1
01	1	0	0	1
11	1	1	0	0
10	1	0	0	0

S_b	minterm
1	m_0
1	m_1
1	m_2
1	m_3
1	m_4
0	
0	m_6
1	m_7
1	m_8
1	m_9
0	
0	
0	
0	
0	
0	

Solution Step 3: Find Prime Implicants

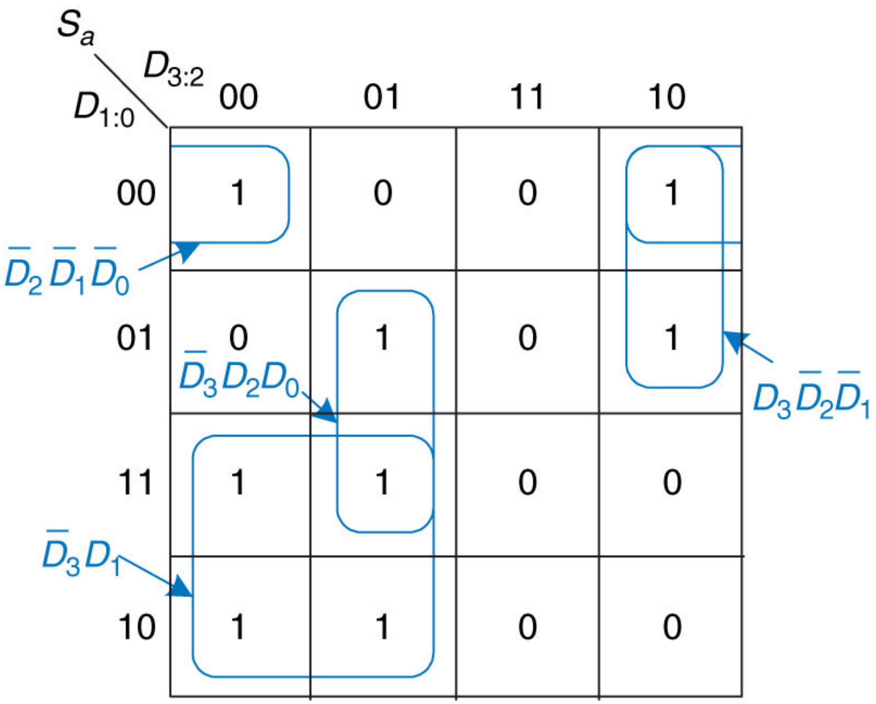
S_a

$D_{1:0}$ \ $D_{3:2}$	00	01	11	10
00	1	0	0	1
01	0	1	0	1
11	1	1	0	0
10	1	1	0	0

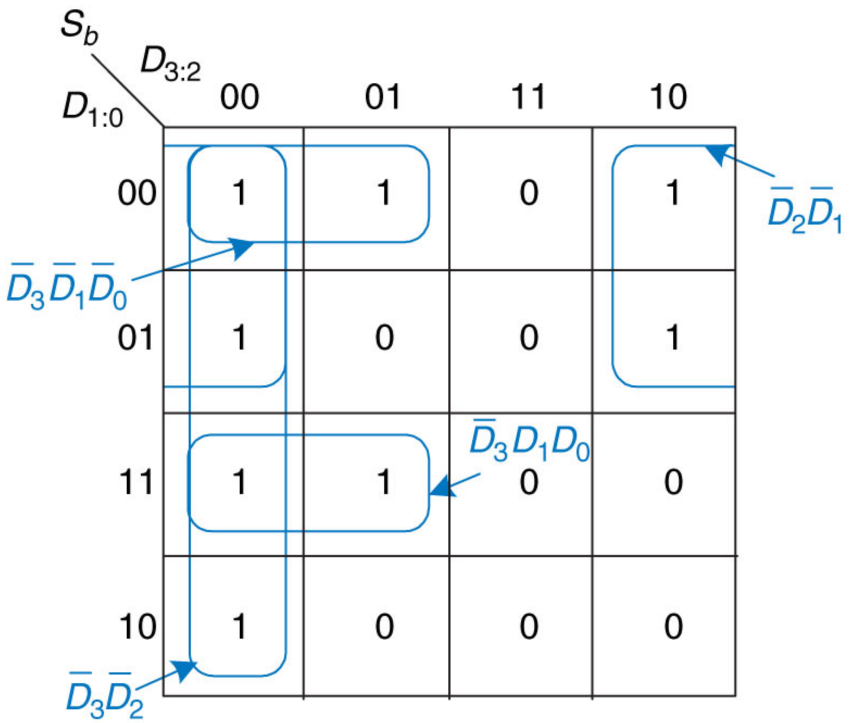
S_b

$D_{1:0}$ \ $D_{3:2}$	00	01	11	10
00	1	1	0	1
01	1	0	0	1
11	1	1	0	0
10	1	0	0	0

Solution Step 4: Prime Implicants & SOP

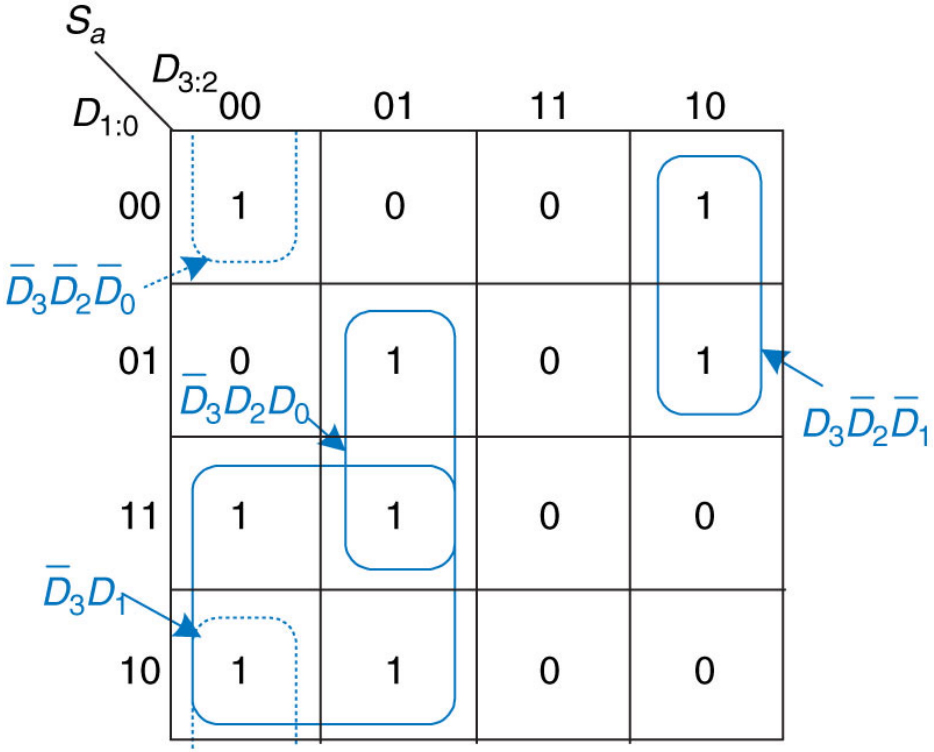


$$S_a = \overline{D}_3D_1 + \overline{D}_3D_2D_0 + D_3\overline{D}_2\overline{D}_1 + \overline{D}_2\overline{D}_1\overline{D}_0$$



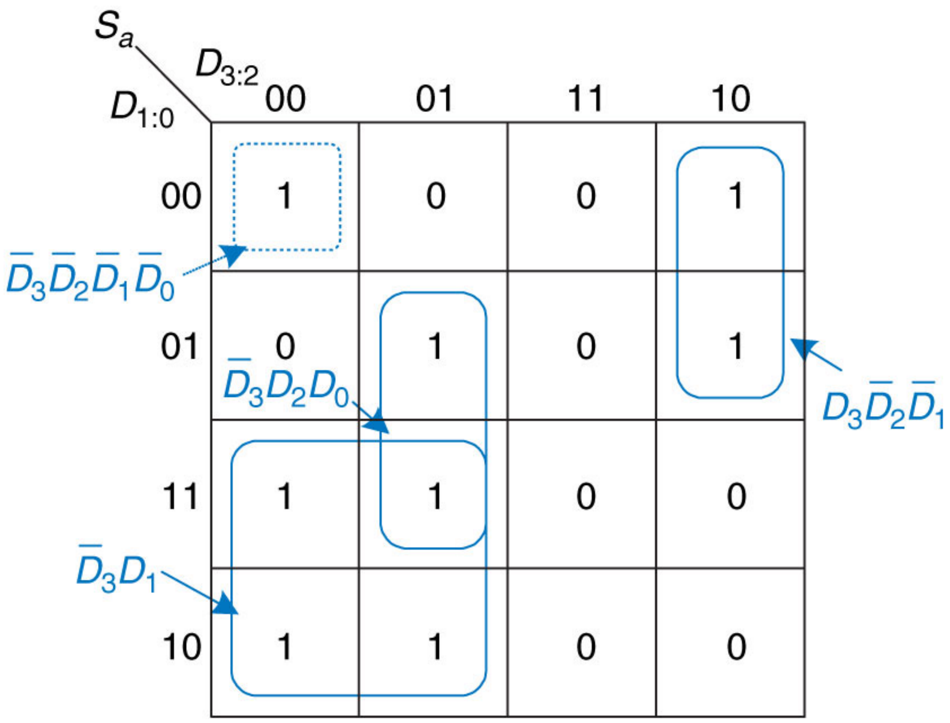
$$S_b = \overline{D}_3\overline{D}_2 + \overline{D}_2\overline{D}_1 + \overline{D}_3D_1D_0 + \overline{D}_3\overline{D}_1\overline{D}_0$$

Prime Implicant Variations



$$S_a = \overline{D}_3D_1 + \overline{D}_3D_2D_0 + D_3\overline{D}_2\overline{D}_1 + \overline{D}_3\overline{D}_2\overline{D}_0$$

Correct Variation

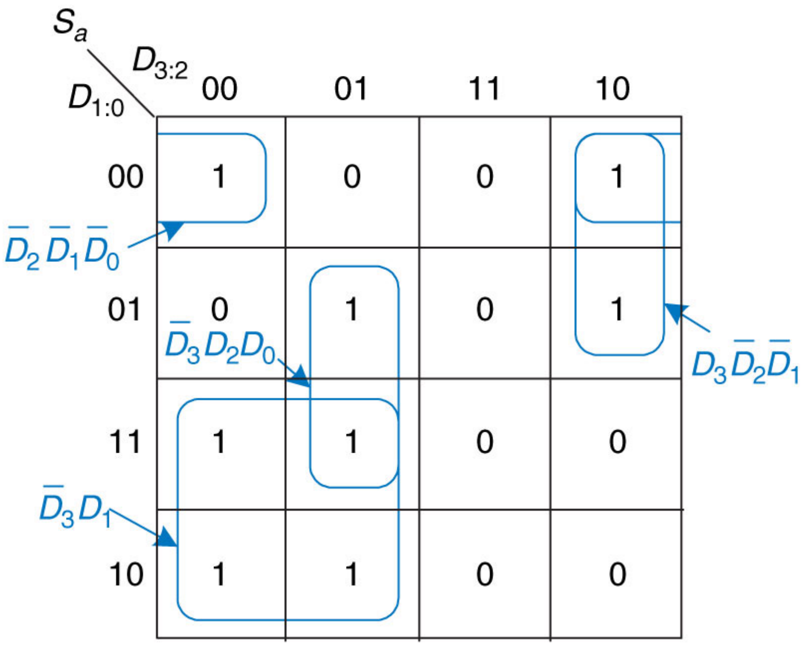


$$S_a = \overline{D}_3D_1 + \overline{D}_3D_2D_0 + D_3\overline{D}_2\overline{D}_1 + \overline{D}_3\overline{D}_2\overline{D}_1\overline{D}_0$$

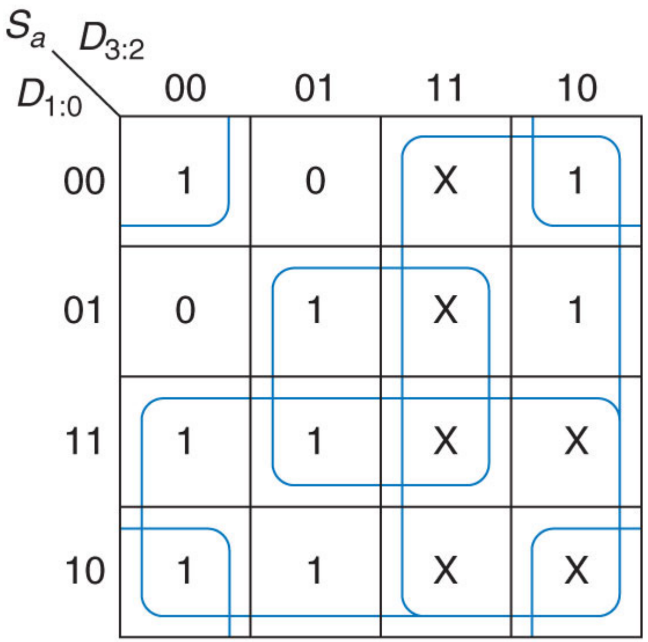
Wrong Variation

Don’t Care in Outputs

- Don’t cares can appear in truth table outputs where the output value is unimportant, or the corresponding input combination can never happen.
- They can be treated as 1s or 0s in the truth table and the K-map.
- They could then help cover larger prime implicants if treated as 1s.

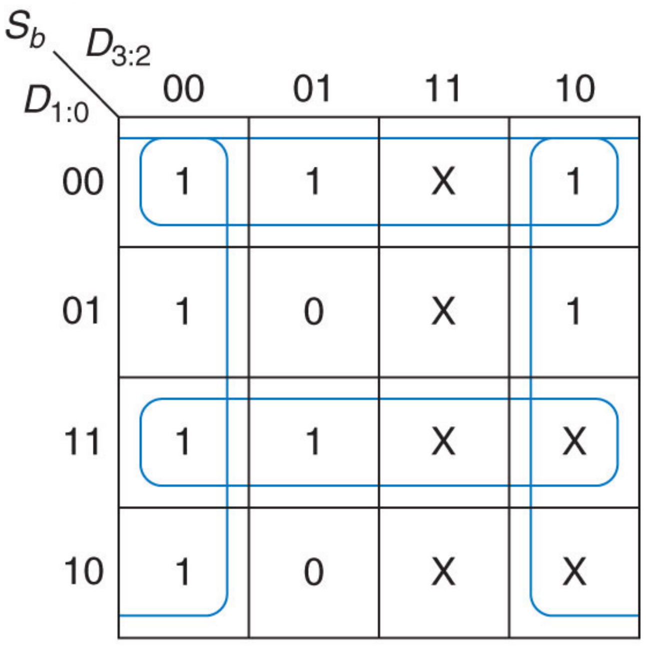


$S_a = \overline{D}_3D_1 + \overline{D}_3D_2D_0 + D_3\overline{D}_2\overline{D}_1 + \overline{D}_2\overline{D}_1\overline{D}_0$

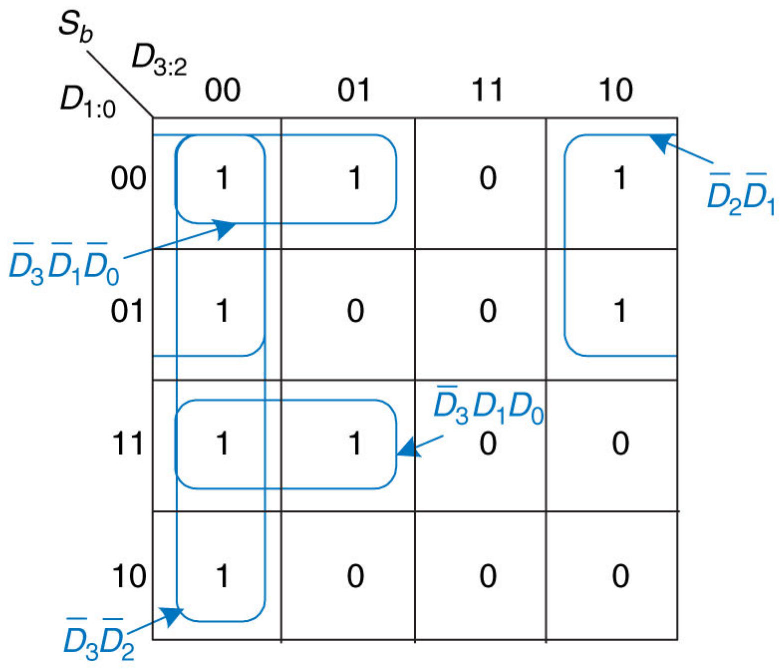


$S_a = D_3 + D_2D_0 + \overline{D}_2\overline{D}_0 + D_1$

Don’t Care in Outputs



$S_b = \overline{D}_2 + D_1D_0 + \overline{D}_1\overline{D}_0$



$S_b = \overline{D}_3\overline{D}_2 + \overline{D}_2\overline{D}_1 + \overline{D}_3D_1D_0 + \overline{D}_3\overline{D}_1\overline{D}_0$

Multiplexers

- Combinational logic is often grouped into larger building blocks to build more complex systems such as the priority circuit and the 7-segment display decoder.
- Two famous combinational circuits are multiplexers and decoders.
- Multiplexers (MUX) choose an output from among several possible inputs (usually 2^n) based on the value of a select signal.
- In other words, a 2^n x 1 **multiplexer (MUX)** is a device that selects binary information from one of 2^n input terminals and routes these data to a single output line

To Do List

- Review lecture notes, and try the examples yourself
- Work on Assignment 1