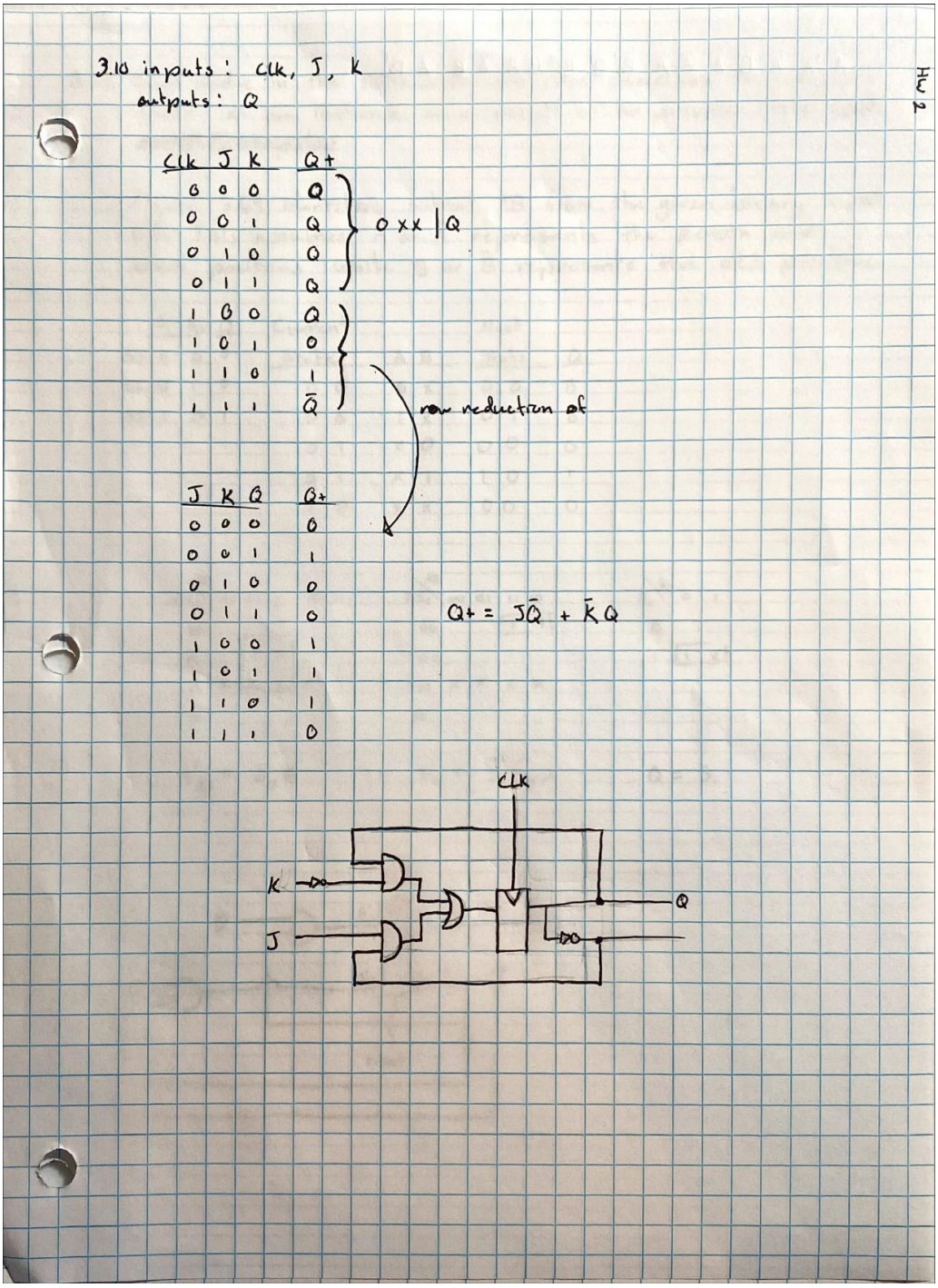
[CS 4341.503] Luke Le lbl190001

3.10 A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state.

(a) Construct a JK flip-flop using a D flip-flop and some combinational logic.



3.22 Describe in words what the state machine in Figure 3.69 does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

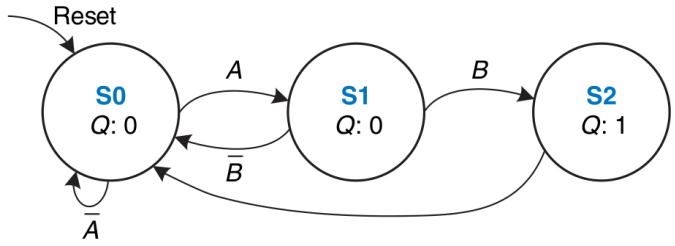


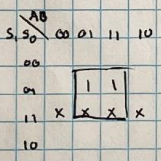
Figure 3.69 State transition diagram

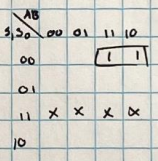
3.22 Each node in the finite state machine describes the circuit's state at an instance as a result of the previous state.

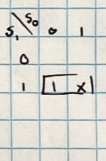
Figure 3.69 identifies subset AB from the given binary input set. This assumes A or $\bar{A}$ represents the zeroth and even positions while B or $\bar{B}$ represents the odd positions.

	S_1	S_0	Q
S0	0	0	0
S1	0	1	0
S2	1	0	1

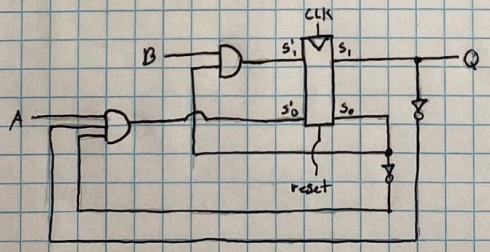
Current State		A	B	Next State		Q
0	0	0	x	0	0	0
0	0	1	x	0	1	0
0	1	x	0	0	0	0
0	1	x	1	1	0	1
1	0	x	x	0	0	0







$S'_1 = S_0 B$ $\quad S'_0 = \bar{S}_1 \bar{S}_0 A$ $\quad Q = S_1$



3.23 Describe in words what the state machine in Figure 3.70 does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

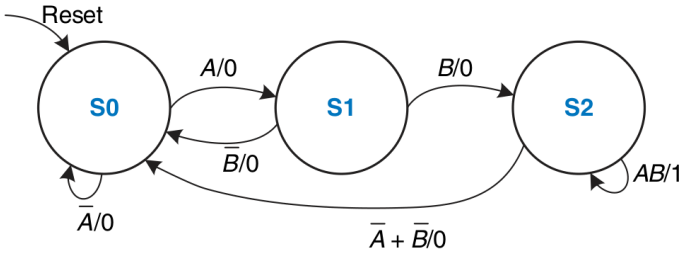
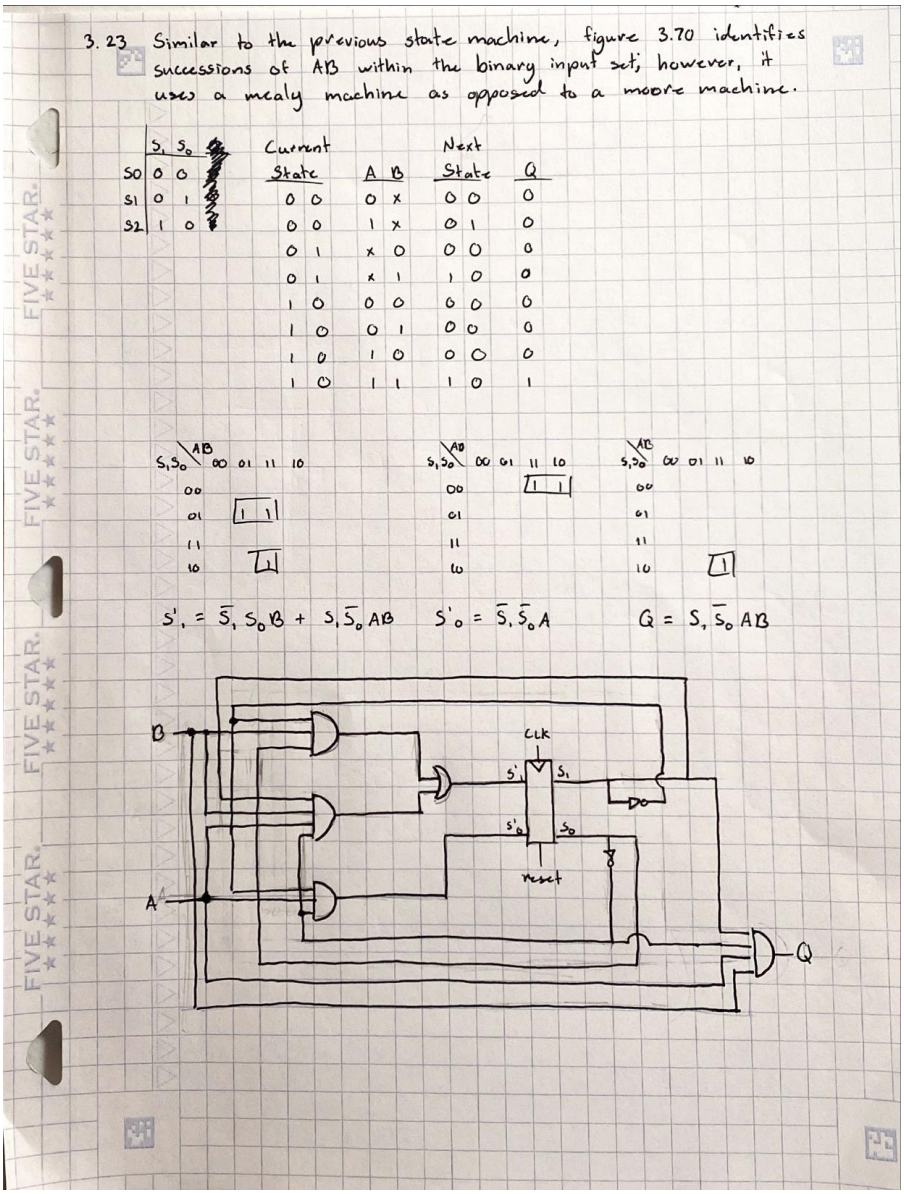
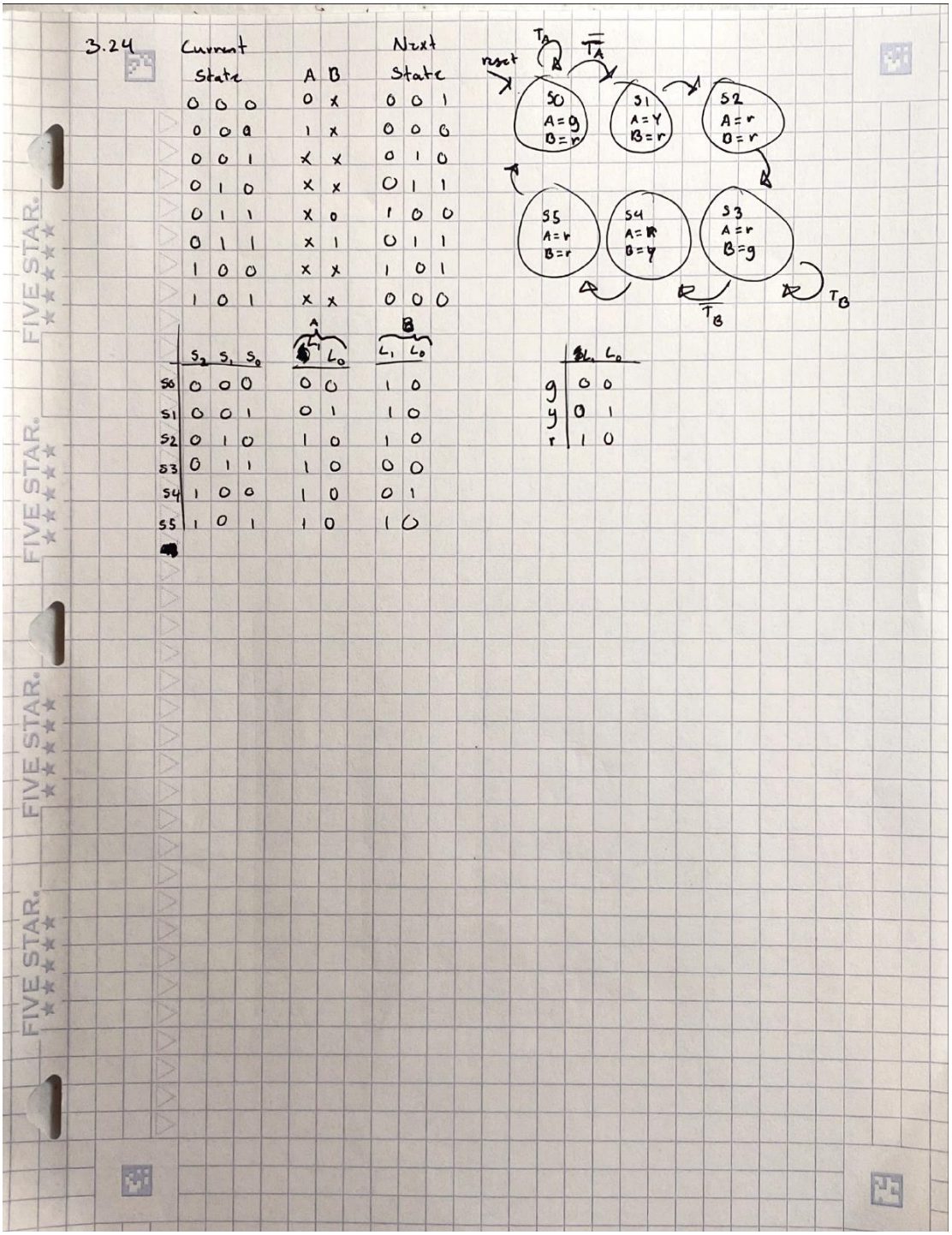


Figure 3.70 State transition diagram



3.24 Accidents are still occurring at the intersection of Academic Avenue and Bravado Boulevard. The football team is rushing into the intersection the moment light B turns green. They are colliding with sleep-deprived CS majors who stagger into the intersection just before light A turns red. Extend the traffic light controller from Section 3.4.1 so that both lights are red for 5 seconds before either light turns green again. Sketch your improved Moore machine state transition diagram, state encodings, state transition table, output table, next state and output equations, and your FSM schematic.



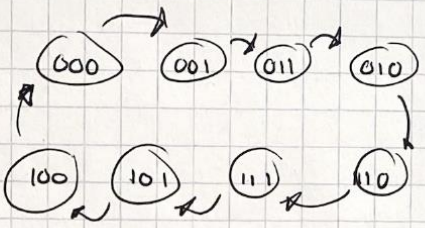
3.27 Gray codes have a useful property in that consecutive numbers differ in only a single bit position. Table 3.23 lists a 3-bit Gray code representing the numbers 0 to 7. Design a 3-bit modulo 8 Gray code counter FSM with no inputs and three outputs. (A modulo N counter counts from 0 to N − 1, then repeats. For example, a watch uses a modulo 60 counter for the minutes and seconds that counts from 0 to 59.) When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000.

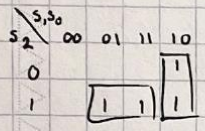
Table 3.23 3-bit Gray code

Number	Gray code		
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

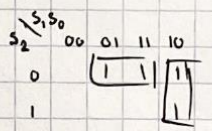
3.27

current state			Next state		
S_2	S_1	S_0	S'_2	S'_1	S'_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

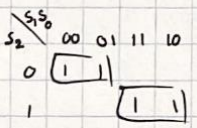




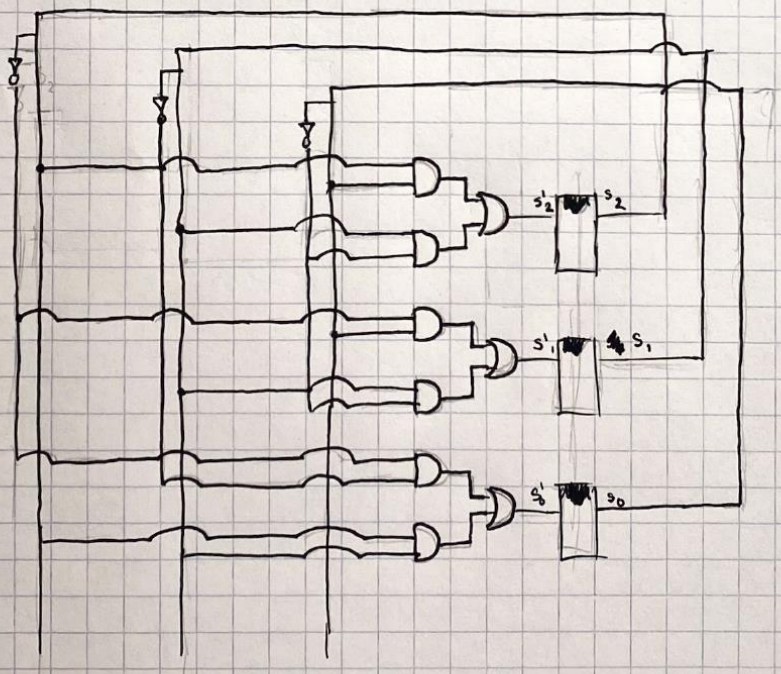
$S'_2 = S_2 S_0 + S_1 \overline{S_0}$



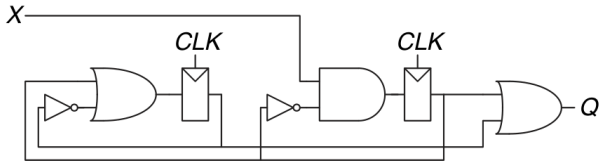
$S'_1 = \overline{S_2} S_0 + S_1 \overline{S_0}$



$S'_0 = \overline{S_2}\,\overline{S_1} + S_2 S_1$



3.31 Analyze the FSM shown in Figure 3.72. Write the state transition and output tables and sketch the state transition diagram. Describe in words what the FSM does.



3.31 $Q = S_1 + S_0$

$S_1' = X\bar{S}_1$

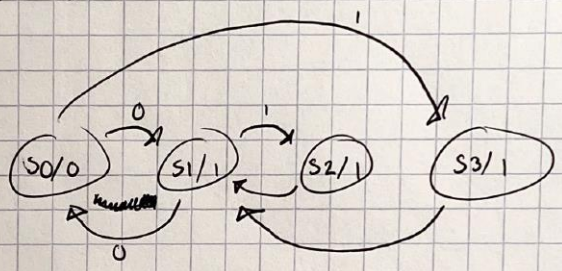
$S_0' = S_1 + \bar{S}_0$

* because Q depends only on states, it is a moore machine

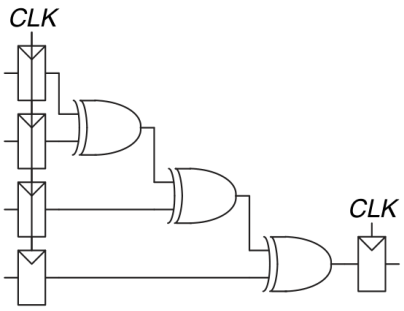
S_1	S_0	X	S_1'	S_0'	Q
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	1

	S_1	S_0
S_0	0	0
S_1	0	1
S_2	1	0
S_3	1	1

given a binary input set, the state machine identifies substrings that contain a minimum of two elements in which the last element is not a 0.



3.33 Ben Bitdiddle has designed the circuit in Figure 3.74 to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps.



(a) If there is no clock skew, what is the maximum operating frequency of the circuit?

t_{pd} = 3 x (100 ps) = 300 ps

$T_c \geq t_{pcq} + t_{pd} + t_{setup}$ = (70 ps) + (300 ps) + (60 ps) = 430 ps

f = 1 / T_c = 1 / 430 = 2.33 GHz

(b) How much clock skew can the circuit tolerate if it must operate at 2 GHz?

$t_{skew} \leq T_c - (t_{pcq} + t_{pd} + t_{setup})$ = (1 / (2 Ghz)) - (430 ps) = 70 ps

(c) How much clock skew can the circuit tolerate before it might experience a hold time violation?

$t_{skew} < (t_{ccq} + t_c) - t_{hold}$ = (50 ps - 50 ps) - 20 ps = 85 ps

(d) Alyssa P. Hacker points out that she can redesign the combinational logic between the registers to be faster and tolerate more clock skew. Her improved circuit also uses three two-input XORs, but they are arranged differently. What is her circuit? What is its maximum frequency if there is no clock skew? How much clock skew can the circuit tolerate before it might experience a hold time violation?