

Hamming encoder/decoder

ARQUITETURAS DE ALTO DESEMPENHO

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Abordagem

► Encoder:

- Control Unit -> 4 bit counter + ROM

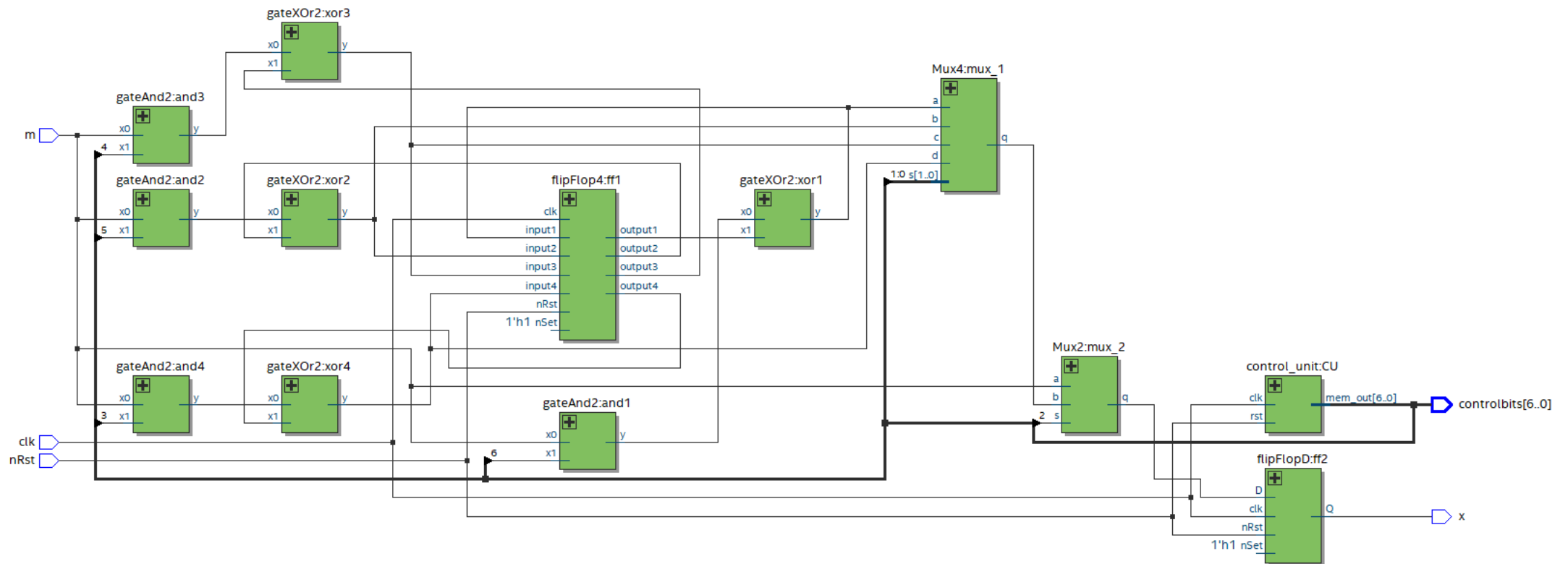
► Decoder:

- ParityBits = (matriz H) * (matriz transposta da mensagem recebida)
- 15 bits de comprimento -> 4 Parity Bits

$$\mathbf{H} = \|\mathbf{A} \mid \mathbf{I}_4\| =$$

$$= \left\| \underbrace{\begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}}_{\mathbf{I}_4} \right\|$$

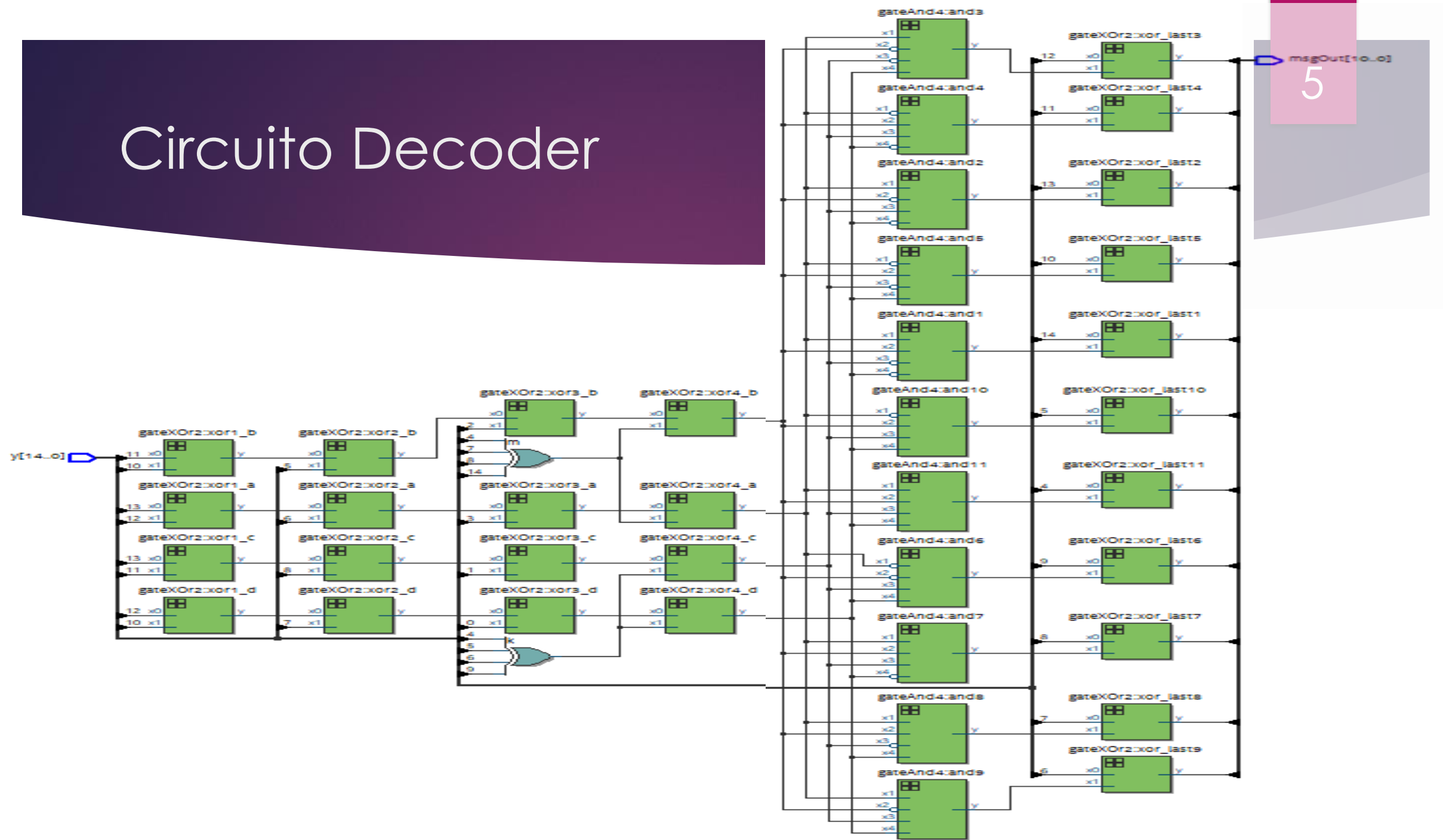
Circuito Encoder



Equações Decoder

- ▶ $M = y_1 \oplus y_7 \oplus y_8 \oplus y_{11}$
- ▶ $K = y_6 \oplus y_9 \oplus y_{10} \oplus y_{11}$
- ▶ $P_1 = y_2 \oplus y_3 \oplus y_9 \oplus y_{12} \oplus M$
- ▶ $P_2 = y_4 \oplus y_5 \oplus y_{10} \oplus y_{13} \oplus M$
- ▶ $P_3 = y_2 \oplus y_4 \oplus y_7 \oplus y_{14} \oplus K$
- ▶ $P_4 = y_3 \oplus y_5 \oplus y_8 \oplus y_{15} \oplus K$

Circuito Decoder



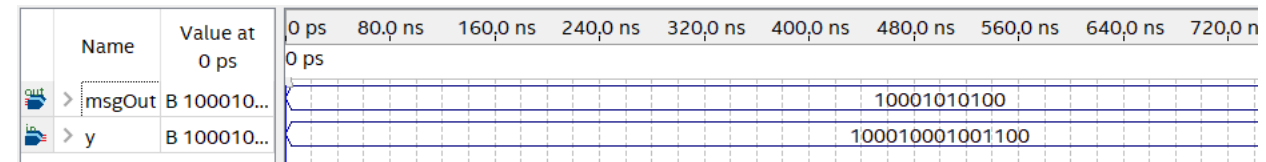
Conclusão

► $H * y^T$ -> detecta a transmissão de erros

► 4 bits a 0 -> não tem erros

► 1 ou mais bits a 1 -> 1 ou mais erros

Decoder:



Encoder:

