The CPU09IDE provides:

- full DMA at 4 MHz bus clock with no wait states.
- single-word DMA and multi-word DMA.
- PIO mode.
- can serve up to 2 IDE drives.
- 16 bit data in DMA mode.
- end of command interrupt capability.

Functional description:

The CPU09IDE card serves as a DMA driven interface for the CPU09 system with a IDE/PATA disk. 4 22V10 GAL's serve as glue logic.
It has a 40 pin connector that directly interfaces to the disk drive. The memory map of the card is 32 bytes of which the first 16 correspond to the 8 registers that an IDE/PATA disk exposes. The access is 16 bits, but in PIO mode the upper 8 bits are discarded.
The upper 16 bytes hold the 16 bit address register, the extended address and control register, a status register and disk status registers.
The card format is Eurocard (160x100mm) and has a DIN41612 a-c connector.

System bus decoder:

The GAL G3 (U9) does most of the address decoding on the system-bus side. The address lines A0--A6 and SEL- are combined to determine the address of the IDE and all registers. (both in the IDE and controller card)
The jumpers A/B determine the board base address. With all jumpers placed the address is $XX00. As the address size of the board is $20 the IDE board can occupy addresses XX00/XX20/XX40/XX60. UniFLEX, as the kernel sources are at this moment, expects the board to respond at $F100.
So all jumpers A/B should be placed and DIV5 as SEL- to bus-line C23. (See data on back-panel)

GAL G3 also controls counters U3 and U2. These counters with parallel load generate the address for data transport from the IDE unit to the system bus. Address U2=>$XX10 for lower 8 bits and U3=>$XX11 for the upper 8 bits. (64K range)

Address A16—-A19 and some control signals are latched by U10, that gets it’s clock from G3 at address $XX13.

Status buffer U17 is also controlled by G3 at address $XX18

Led D1 is activated by access to the IDE controller address range.
Led D2 signals DMA activity of the controller.

IDE control decoder:

Gal G4 decodes the signals for the IDE control.
IDE_CS1FX is active at addresses $XX00--$XX0F.
IDE_CS3FX is active at addresses $XX1C--$XX1F.
IDE_A0/IDE_A1/IDE_A2 are connected to bus signals A1/A2/A3 at the appropriate moment, e.g if DACK for GAL G2 is active.
The enable and direction signals for buffer U5 are also decoded by G4.

IRQ and DMA control:

GAL G2 decodes the signals to control the access mode, PIO or DMA and generates the clock signal for the state machine counter U12. It provides a clock for U1B. When DMA is enabled via the latch and the input conditions are valid a clock pulse is generated. When U1B is set, it halts the CPU and signals G1 and G4 that a cycle has to be generated. When the input conditions stop, U1B is reset from G2.

The IRQ signal is buffered by U16D in open drain. Depending on the setting of J6, the back-panel gets a signal on FIRQ or IRQ. Current firmware assumes connection between pin 1-2. E.g. IRQ.
Jumper J5 should be put between 2-3 to enable DMA control.

State machine control:

This task befalls GAL G1 (U6) and counter U12.
The counter is preset to 1 by signal R161. This activates the preset input, after a reset or reaching state 3 if DMA request is not still active.
The latches/buffers U11/U13/U14/U15 are controlled by G1 as well.
G1 also decodes the IDE signals IOR and IOW to the IDE-port J2.

Status buffer:
This buffer is located at address $XX18.

- Bit D0 is connected to IDE_IOCS16.
- Bit D1 is IDE IORDY.
- Bit D2 is IRQ.
- Bits D3—-D5 are always 0.
- Bit D6 is IDE DMA Request.
- Bit D7 is IDE INT Request.

Latch U10:
This latch is located at address $XX13.
A reset signal sets all bits to 0, this happens also at power-up.

- Bits 0—-3 are A16 to A19 used during DMA transfers.
- Bit 4 is CSEL.
- Bit 5 is Interrupt enable.
- Bit 6 is DMA enable.
- Bit 7 is DMA direction.

G.A.,C.S.