CPU09SR4

Provides:

- up to 4 serial ports, HD63B50 at 4MHz busclock with no wait states
- each port has a programmable baudrate setting
  38k4,19k2,9k6,4k8,2k4,1k2,0k6,0k3
- full interrupt capability
- LED which signals on board selection
- RTS output, CTS input handshake

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The address decoding of the board is handled by two components, the GAL U29 and the comparator U5.
It starts with the input on C23, IOSEL-. This signal is entered from the back-panel and offers an address range.
Within this range, the setting of the jumpers (input to the comparator U5) determine the final address of the four ACIA-channels and the registers for baud rate and handshake.

About Jumpers:

```
    J6
[o][o][o][o]
[o][o][o][o]
    J7
 A  B  C  D  (position)
```

These are for board select, e.g.where the board should appear in the address range. Assume we wired the /sel pin of the board to DIV3 (F008-F07F). Jumpers are to be placed between the J6 and J7 strip, thus 4 max.
(Pull-up resistors R1-4 make sure that a 1 is present for no jumper)

```
D  C  B  A     Address select
Where 'V' is jumper present and '-' jumper absent

V  V  V  V     XX00        should not be used on the main CPU side, as it
                           conflicts with ACIA on MON board.
V  V  V  -     XX10
V  V  -  V     XX20
V  V  -  -     XX30
V  -  V  V     XX40
V  -  V  -     XX50
V  -  -  V     XX60
V  -  -  -     XX70
-  X  X  X     XX80...XXFF      only for use with the CPU09IOP board.
```

With the UniBug monitor it is easy to check if you did the right selection, e f000-f07f. You should see the MONitor ACIA and the PIA and the ACIA's on the SR4 board(s).

Address decoding for the channels:

The GAL generates the Chip Select lines for the ACIA's 1=U2, 2=U12, 3=U18 and 4=U24.
It also generated the clock signals for the latches U27 and U28.
(You can check the GAL design file for this as well.)

	Address	Latch	Address	
ACIA 1	xx00-xx01	U27 D0-D3	xx03-xx04	xx06-xx07
ACIA 2	xx05-xx05	U27 D4-D7	xx03-xx04	xx06-xx07
ACIA 3	xx08-xx08	U28 D0-D3	xx08-xx09	xx0E-xx0F
ACIA 4	xx0C-xx0D	U28 D4-D7	xx0E-xx0F	xx0E-xx0F

Note that the latch can be accessed on 4 addresses per latch but there's physically only one latch available.
Data bits D0-D3 and D4-D7 have a identical layout for each ACIA.
The bits D0-D1-D2 determine the baud rate, as do D4-D5-D6.

All 0 selects 300 baud and all 1's 38K8. The selection is done by multiplexers U4, U13, U19 and U25. (See schematic diagram for more details)
Bits D3 and D7 will pull the respective CTS line low, thus disabling hardware handshake.

IRQ:
All open drain outputs of the ACIA's are connected to a buffer U8A and pull-up resistor R7.

Clock signal:
The clock signal for the baud rate is taken from the back-panel signal EXTSIG1. The safety components R14, C5, D7 and D8 prevent damage from incorrect voltages to this input. The clock is fed to the divider chain U30A and U30B to generate 8 baud rates.

MRDY:
The GAL also generates the MRDY signal. This signal is connected to the back panel in C24 and signals the processor that the device is ready. A value for C4 determines a possible delay for slower devices.

And the LED D5 gives a visual signal of activity.

G.A., C.S.