Provides

- MC68B54 ADLC controller
- wide clockrate selection, 1.228MHz...9K6
- dual connectors CAT8
- dipswitches for line termination disable/enable
- dipswitches for clock source disable/enable
- collision detection
- hardware Econet (R) compatible
- CPU09GPP IO compatible (max GPP bus frequency 8...10MHz)
- CPU09FLX IO compatible

This interface is suitable for simple network applications. The ADLC is capable to transfer a data packet with minimal code/overhead and maximum flexibility.

Functional description:

The 68B54 ADLC (Advanced Data Link Controller) looks in a way to the 68B50 ACIA, but can detect start and/of end of dataframes while maintaining a CRC of all data passing and checking that at the end of frame(s). While sending fames, it accumulates the CRC over the data and appeding that after the last data has been sent. It also has DMA capabilities, they are not used in this design.

The Chip select is connected to the SEL1 signal, provided by the GPP or FLX card. This gives access to the 4 addressable locations in the chip.
The ALDC internal registers which or more than 4 can be selected by address select bits in one register.

Data transfer clock:

The BCLK signal of 1.2288Mhz (4.9142/4) is fed to the divider chain of the HC4040 (U7).
With ONE jumper on J3-J4, a baud-rate can be selected, between 9K6 and 11M2 can be selected. This clock is fed into the driver U1B passed on to the bus connectors.

Signal conditioning:

The components U1, U2, U3, U4 and U5 are responsible for all signal conditioning that’s needed to reliably drive the communication line. Care is taken to adapt to the transmission line to the correct impedance of the connection cables.
The handshake signals CTS (Clear To Send) and DCD (Data Carrier Detect) are also made by these circuits.

Switches:

Dipswitches SW1 takes care of line termination.
SW2 offers the possibility to determine the source of the transfer line clock signal.

G.A.,C.S.