The CPU09GPP provides:

- local HD63C09 CPU at 4MHz clocks
- 1Kx8 dual port RAM between host CPU and local CPU with interrupt flags and * up to 32KB of local RAM
- up to 8KB of (E)EPROM with 28 pin socket for 32K capacity
- up to 1K Bytes of dedicated IO space (A0...A9)
- local periodic timer interrupt circuitry (6.7, 13, 26 mS)
- LED's which show host CPU access and local CPU access
- local CPU can be individually reset from assigned bus pin (A3)
- the CPU09GPP has it own address decoding for the system bus. (Page select for F8,F9,FA,FB or FE (default)) Cardselect 0...3
- 40 pin IO expansion connector with local Data, Address and Control signals. Can handle DMA from appropriate IO devices.

Functional description:

The card contains it’s own CPU with 64k addressing capacity.
There’s 8K of program space in the (E)Prom visible for the processor.
(Changing the GAL can increase this space to 32K)
The logic in the GAL’s take care of all addressing tasks.

A 1Kx8 dual port ram is used for exchange of data between this processor and the system-bus.
An interrupt mechanism flags data availability to either side of the dual port ram.

System bus decoder:

The GAL G1 (U2) takes care of the decoding of the page and card selection.
Placing the correct jumpers on J3 and J4 selects the page and card.
No jumpers defaults to page FE and card select 0, because of the pull-up array RA2.

Data exchange:

The system bus can only see this 1K page and has no direct access to other area's in the GPP memory map. By writing to the dual-port (internal) ram address $3FF, the IRQ line to the GPP-CPU is set, signaling that data is available from the system-bus side. If a ram location is accessed by both the system-bus and the GPP-CPU at the same time, arbitration logic in the dual-port ram pulls /busy on one side. Therefore it is **mandatory** that the links L1 and L2 are present.

N.B. The actual address in the system-bus is determined by the choice of page and card address.

CPU led:

Active if the system-bus accesses the dual-port ram.

GPP address decoder:

The GAL G2 (U10) takes care of all address decoding. It also combines the System reset B_RES- and the card reset A3- signals. Either the system bus reset (A21) or the GPP-card reset (A3) will reset the GPP processor.

The dual-port ram is mapped to $0000-$03FF. Like on the system-bus side, the GPP can signal data present by writing to an address in the ram. This is $3FE and a write operation to this address signals an IRQ to the system-bus.

RAM:

Location U4 is intended for the system ram. The layout is a narrow 28 pin, intended for a 32k ram. This is mapped to $0400-$7FFF.

(E)Prom:

Location U5 is intended for system rom. The layout is a 28 pin, intended for a maximum of 32K Rom. The current GAL decoding is set for $E000-$FFFF. This is a 8 K area that can be expanded by changing the logic of GAL2.

SEL1 and SEL2:

These signals select the access to devices connected to the 40 pin header J5.

SEL1 = $8000-$80F7
SEL2 = $8080-$80FF

NB: A8 and A9 are not used in the decoding. This means the same physical locations will be accessed multiple time in the area $8000-$83FF

LCLIO:

Interrupt timer register. Address $8400-$847F. Also multiple locations in $8400-$87FF.

IOLED:

Active in area $8000-$83FF

Interrupt timer:

The divider U10 processes the SIG30 clock signal 1.2288Mhz (4.9142/4)into pulses of 3.3mS, 6,6mS of 13,3mS. Placing only ONE of R7, R4 or R5 selects an interrupt timing signal.
The input to U10 is actually protected by R6, C11, D3 and D4. This makes sure that the input will not be damaged if a supply voltage is accidentally fed to this bus signal (e.g. +/-12V)

Connector J5:

This connector carries Data Bus D0—-D7, Address Lines A0—-A9, SEL1/2, and the control signals R/W, E, Q, BS, AB, HALT, IRQ and FIRQ. Also a buffered 1.2288Mhz signal.

Still some spare pins available.

G.A.,C.S.