CPU09MON

Provides:

- Two 32 pin sockets for U4 and U5, for up to 992KB of user RAM
- One 28 pin socket for U6 for up to 8 KB of (E)PROM, in 2K pages FF800-FFFFF
- A serial console port (ACIA), (HD63B50 running at 4MHz busclock with no waitstates) baud rates 19k2,9k6,4k8,2k4,1k2
- Hardware BLACKHOLE and WHITEHOLE memory detection and generation
- Central baudrate generator for the whole system, 1.2288MHz over the system bus
- 8 status LED's for kernel flagging, the 'LIGHTS' feature as coded in the kernel
- Periodic timer interrupt, 100 Hz
- IO decoding for most devices in the area FF000-FF3FF
- Dual interrupt vectors, depending on supervisor/user state



Functional description:

The MM3 CPU board has address lines A0 to A19 and can access a total maximum of 1024 kB of memory and I/O. The 63C09 processor has A0 to A15 and can access a maximum of 64kb. For the MM3-CPU to access all, dynamic memory mapping is used, where memory is handled in 4K pages. See the documentation for the MM3 card and the memory map (CPU09MON_map) for more information on this.

Memory functions:
The 09MON board facilitates the full use of all memory area that the MM3 board can access. All decoding of this address area is done by the GALS.
These are G1, G2 and G3 (U11, U12, U9) The address lines A15 to A18 are combined by the Nand-gate U14A and fed into G1. (This frees some pins on the GAL)
A19 is handled by G1. This effectively divides the memory in two area's of 512 kb each.

RAM:
The CE-signal of socket U4 (32 pins) is connected to the signal RAME1-.
This signal is active in the lower 512 kb part of the memory area.
The upper 512 kb is divided between Ram U5, the I/O, (E)Prom U6, the black- and white-hole and the DATBOX (Decoded on the MM3)

The CE-signal of socket U5 (32 pins) is connected to the signal RAME2- and covers the whole 512 KB of the device. Both Ram sockets are intended to hold 512k x 8 chips with 32 pins. A 128k x 8 chip may also work, UniBUG is clever enough to, detect and avoid, mirror memory.

When you applying smaller memory chips check carefuly the pin functions. Where the 512Kx8 chip has A17, a smaller device may have i.e. a second CS. To use such a chip you need measures to have such a pin to a proper level. (i.e. KM681000 128Kx8 has CS2 on pin 30, keep that pin out of the socket and connect it with pin 32) Be aware that working with 128K will cause a LOT of swapping actions!

ROM:
The CE  (and OE) signal of socket U6 (28 pins) is connected to the signal ROME-
This socket can hold an 8k x 8 (E)Prom. However, the decoding only provides a 2k area to be selected. Using the Rom-page select jumpers, 4 blocks of 2k can be selected. The (E)Prom select jumpers J4 (R-A12)and J5 (R-A11) are used for this. Pull-up resistors R1 and R6 provide a high signal if no jumper is set. (E)Prom A11 and A12 are high.

If jumpers are set to position 2-3, these lines are connected to GND.

Setting the jumpers to position 1-2, connects the A11 and A12 line of the (E)Prom to PA2 and PA3 of the PIA, thus facilitating selection of 2k blocks by the PIA. (under program control)
The top part of either 2k area is used for CPU-vectors. This area is 512 bytes in size and it is decoded by the MM3 card and handled by G1. Signal XFEXX.

White-hole and Black-hole:
This area is decoded by G1 and the signal BHSELB-
When active, it selects the enable signal of the buffer U7. The input of this buffer is hard coded by means of A12 connected to D0-D5 and D6-D7 to GND.
This way, the bus will always see 3F if A12 is high for the Black-hole (FDXXX).
And if A12 is low, the bus will see 00, White-hole (FCXXX).

I/O:
This area is mainly decoded by G1 to the addresses FF000 to FF3FF and is 1K in size.
By means of G2 and G3 it is divided in smaller parts to accommodate I/O chips and areas.

ACIA:
The serial port ACIA is at the bottom of the I/O area. (FF000-FF003)
The chip select is decoded by G3, that has A2 as lowest address line.
The chip has 1 address line that's connected to A0.
As the A1 line is missing, the ACIA is mirrored and can be accessed on two addresses.
The baud rate clock is provided by the X1 oscillator and divider U13.
The serial port has a line driver U17 (MAX232) to convert the 5V signals to the RS232 levels. To prevent a "latch-up" on this chip, diodes D9 and D10 are added.

PIA:
In the memory map, just above the ACIA, the PIA can be found.
It's addressed on locations FF004 to FF007.
The PIA has A0 and A1 connected.

The PIA has led's connected to it's B-port. These are useful for debugging and status indication. For UniFLEX they reflect the 'lights' location as coded in TSC's versions.
The A-port is used for the (E)Prom page selection, enabling the RTC and the RTC signals. (100Hz--800Hz)
PIA lines PA1, CA2 and CB2 are currently not used.

DIV #3—-#7 (parts of FF000-FF3FF)
These area's are also decoded by G2 and G3.
They are connected to the Din41612 connector and fed to the bus.
So they can be used by various other cards, by connecting the signals from the back-panel to other cards as needed. The software assumes a configuration as is shown in the memory map.

Miscellaneous:

IRQ:
Both IRQ from the ACIA and PIA are combined and fed to the input of buffer U8A.
Because the outputs are open drain, they need the pull-up R7.

MRDY:
This signal is generated by G2 and fed to the buffer U8B. Using C1, this signal can be stretched. (See schematics for details)

Clock signal:
The baud rate clock and RTC signals are generated by X1 and dividers U13 and U10. U13 divides by 2 times 16. U13 thus gives clock signals for baud rates of 19200 down to 1200, selected by ONE jumper on the H1 jumper block.

X1 delivers 4,9152Mhz and this is divided by 4 to get the SIG30 signal, buffered by U8D and connected to the back panel. This signal is protected using R16 and C15, together with D12 and D13.

X1 divided by 64 is fed to U10A. This divides by 12, to give 1600Hz.
Then, U10B delivers 800Hz, 400Hz, 200Hz and 100Hz, all of which are fed to the PIA port A. The 100Hz is also fed to PIA CA1 and used as RTC signal for the operating system.

G.A, C.S