Here is the CPU09FLX board Rev 0.2

Provides:

- address decoding for FEXXX / XEXXX
- 2K RAM socket
- 2K (EP)ROM socket
- 40 pole connector with CPU09GPP layout
- flexible IO decoding due to GAL
- Interval timer, interrupt capable

This board allows a very compact FLEX system to be build. With the CPUXXCMI you would have:

2K Monitor ROM, 68X02/68X09/63X09 CPU, 64K RAM, Console ACIA, baud clock generator fully buffered bus signals.

The mini-backplane CPU09BP3 would be more then plenty for such a system.

Functional description:

Address decoder:

This function is performed by the GAL G1 (U2) and the nand-gates of U1.
The upper address lines A19-A16 are combined by U1A and the lines A15-A13 by U1B.
Contrary to a PCB or a fixed function circuit, a GAL can be changed with ease, offering flexibility for this board.

See the schematic diagram and the GAL-design file for more details.
The GAL decodes the address space for the 24 pin sockets intended for a Ram (U4) and an (E)Prom (U5).

Both SEL1 and SEL2 signals to the 40 pin connector are also generated.

Lastly, it generates the control addresses for the interrupt and timer, to select Gal G2 (U10) This Gal in turn enables activation or deactivation of the timer and interrupt control.

Timer:

The divider U7 is fed with the SIG30 signal of 1.2288Mhz (4.9142/4) and divides this down to pulses of 3.3mS, 6.6mS and 13.2mS. Either signal can be used by placing a 0 Ohm resistor on position R3, R4 or R5 respectively.
Components R1, C1, D2 and D3 make sure that a wrong signal level will not harm U7. The buffered output of U7 is used to put the 1.2288 Mhz signal to pin 35 of the IO connector.

The TIMER signal is fed to the CLK of the latch U8B. The output of this latch is connected to the buffer U9B. U8, U9 and U10 make a interval timer, which can create an IRQ interrupt and status of the hardware. If enabled by the GAL G2, this buffer will pass an interrupt to D7 on the data bus. D6 will reflect the IRQ- signal, D0 if the interrupt from the interval timer has interrupt enabled. Writing to U8A with D0 set enables IRQ from the timer, if D0 was clear the interrupt is disabled. Reading U9 shows the timer interrupt on bit 7, the board IRQ on bit 6 and the interrupt enable/disable status on D0.

Some IO cards may use IRQ, some don’t use it.

For very minimalistic purposes, the CPU09FLX card can be populated as FLXMIN files show. You need to put 3 wires on the board, but on the whole the board has few components. Address decoding needs to be done externally is such case, i.e. from a CPUXXCMI.

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