The 09FLP support board provides:

- WD2793 controller, which has clock divider and 5″/8″ mode
- 50 pin connector for 8" drives, 36 pin connector for 5.25" / 3.5" drives
- control latch: drive select, side select, SD/DD select, 8"/5" mode select
- status port: FDC DRQ, FDC INT,
- motor-on timer
- test jumper, variable capacitor and 2 potentiometers to adjust various settings for the WD2793
- local 2MHz oscillator for the WD2793
- 40 pin IO connector and form factor that fits on a CPU09GPP/CPU09FLX
- 125 kBit/250kBit and 500 kBit data rate

The schematic is the final version of the design.

Description of functions:

The board is based on the WD2793 controller. It performs most functions that have to do with signal handling to the floppy disk. It gets some setting inputs from a latch U13. U13 also selects 1 of the 4 individual Floppy-drives signals using SEL0...3.
The clock signal to the 2793 is 2Mhz, so it can handle 5/8 inch formats in Single and Double Density.

U13 data:

D0-D3 selects respective Sel...3 drive selects. On the Shugard-bus side, these signals are active low, so inverter-buffer U7B is used. Be aware that only one drive should be active at any time!

D4= side select, to buffer U7A and Shugard-bus. (1 = side 1)
D5= Density select to the 2793 controller. (1 = single)
D6= Mode signal to buffer U7A and the Shugard-bus. Sets the WD2791 in 8″ mode or in 5″ mode, also switches T1 to change filter in the pump circuit for the 2793. The signal is also used by some older 5″ drives to change speed and filters.
D7= Head load delay to the 2793, normally controlled by the HLD signal from the 2793. Pulsing D7 will re-trigger te one-shot for the head load delay.

2793 to floppy:

Step, Direction, Write Data and Write gate signals are also active low on the Shugard-bus side, so they are buffered and inverted by U4A.
TG43 (Track greater than 43) is only used for 8″ drives. It’s inverted and buffered by U4B.

Floppy to 2793:

Track zero (TR00), Index pulse (IP), Write Protect (WPTR) are buffered by U5B and fed to the 2793.
The Read Data (RD) is fed to the one-shot U6B and then to the 2793.

Motor-on signal:

This is generated by U19. This timer circuit is set as re-triggerable and is activated by the GAL U2. The logic in there makes sure that any access to the 2973 or the registers also activates the motor-on signal.

RDY-signal:

This signal is buffered and inverted by U4B and fed to the ready input of the 2793.

Controller status:

There's a status signal buffer that gives access to signals FDCINT (Floppy Disk Controller Interrupt) on bit D6 and FDCDRQ (Date Request) on bit D7.

GAL (U2) functions:

This programmable logic device has two primary tasks. It decodes all address locations for the chips on the control board and also the reset signals for the 2793 and the latch U13. The design file contains all information on this. The 40 pin header offers the address data SEL1 and SEL2, Address lines A2-A3, the CPURES, clocks Q-E and Read/Write signals. All of these are used to provide the control signals for the board.

Addresses:

xx00--xx03 = Floppy controller 2793 registers.
xx04--xx07 = Latch U13.
xx08--xx0B = Status port U1.
xx0C--xx0F = Trigger helper. (Debugging with Oscilloscope, pin 12 of U2)
(Any access to the above addresses will trigger the motor on signal.)

G.A.,C.S.