

Pin definities van systeem backplane 64 polig

Pin	A-rij	Pin	C-rij
1	0 VOLT	1	0 VOLT
2	0 VOLT	2	0 VOLT
3	DIV1 #	3	DIV2 #
4	DIV3 #	4	DIV4 #
5	DATA 0	5	DATA 1
6	DATA 2	6	DATA 3
7	DATA 4	7	DATA 5
8	DATA 6	8	DATA 7
9	ADRES 0	9	ADRES 1
10	ADRES 2	10	ADRES 3
11	ADRES 4	11	ADRES 5
12	ADRES 6	12	ADRES 7
13	ADRES 8	13	ADRES 9
14	ADRES 10	14	ADRES 11
15	ADRES 12	15	ADRES 13
16	ADRES 14	16	ADRES 15
17	ADRES 16	17	ADRES 17
18	ADRES 18	18	ADRES 19
19	0 VOLT	19	0 VOLT
20	E CLOCK	20	R/W
21	/RESET	21	/VMA
22	BS	22	BA
23	Q CLOCK	23	DIV5 # (SELECT)
24	R/W DMA(IN)	24	MRDY
25	/HALT	25	/DMA-/BREQ
26	/FIRQ	26	/IRQ
27	/NMI	27	/VMA(DMA) (IN)
28	DIV6 #	28	DIV7 #
29	+12 VOLT	29	+12 VOLT
30	-12 VOLT	30	-12 VOLT
31	+5 VOLT	31	+5 VOLT
32	+5 VOLT	32	+5 VOLT

DIV5 IS BANKSELECT VOOR MEMORY BOARDS
 DIV6 IS BUS ENABLE INPUT VOOR DMA
 DIV7 IS BUS ENABLE OUTPUT VOOR DMA

Pin definities van IO backplane 64 polig

Pin	A-rij	Pin	C-rij
1	0 VOLT	1	0 VOLT
2	0 VOLT	2	0 VOLT
3	>56K #	3	100HZ #
4	/BANKSEL #	4	/XFFXX #
5	DATA 0	5	DATA 1
6	DATA 2	6	DATA 3
7	DATA 4	7	DATA 5
8	DATA 6	8	DATA 7
9	ADRES 0	9	ADRES 1
10	ADRES 2	10	ADRES 3
11	ADRES 4	11	ADRES 5
12	ADRES 6	12	ADRES 7
13	ADRES 8	13	ADRES 9
14	ADRES 10	14	BUF'D E CLOCK
15	BUF'D R/W	15	BUF'D /RESET
16	ADRES 11	16	ADRES 12
17	0 VOLT	17	0 VOLT
18	E CLOCK	18	R/W
19	/RESET	19	/FE0XX
20	DISDEC	20	/IRQ
21	/FF0XX #	21	/FE080 #
22	/FE070 #	22	/FE050 #
23	/FE040 #	23	/FE030 #
24	/FE020 #	24	/FE010 #
25	BAUD 3	25	BAUD 2
26	BAUD 1	26	BAUD 0
27	BUF'D ADR 3	27	BUF'D ADR 2
28	BUF'D ADR 1	28	BUF'D ADR 0
29	+12 VOLT	29	+12 VOLT
30	-12 VOLT	30	-12 VOLT
31	+5 VOLT	31	+5 VOLT
32	+5 VOLT	32	+5 VOLT

Pin definities van IO backplane 31 polig

Pin

1	0 VOLT
2	0 VOLT
3	ANALOG 0 VOLT
4	DATA 0
5	DATA 1
6	DATA 2
7	DATA 3
8	DATA 4
9	DATA 5
10	DATA 6
11	DATA 7
12	CARD SELECT #
13	E CLOCK (BUF'D)
14	R/W (BUF'D) #
15	/RESET (BUF'D)
16	/IRQ
17	DIV1 #
18	DIV2 #
19	BAUD 3
20	BAUD 2
21	BAUD 1
22	BAUD 0
23	ADRES 3 (BUF'D)
24	ADRES 2 (BUF'D)
25	ADRES 1 (BUF'D)
26	ADRES 0 (BUF'D)
27	DIV3 #
28	+12 VOLT
29	-12 VOLT
30	+5 VOLT
31	+5 VOLT

/RESET BETEKENT 'NOT RESET' = AKTIEF LAAG

DUIDT EEN NIET DOORLOPENDE BUSVERBINDING AAN

DIV1 is de clock voor floppy card

AANSLUITINGEN VOOR HET [CS] 6809 SYSTEEM

Lijst van alle apart aan te brengen draden.

Allereerst moeten alle datalijnen tussen de beide backplanes worden doorverbonden (zie bus specs). Vervolgens alle overeenkomende adressen dus A0 t/m A10, A11 en A12. Ook 'E', R/W /RESET, /IRQ en de voedingsspanningen moeten worden gedaan.

De volgende verbindingen dienen om wat extra controle signalen tussen de diverse printen door te geven.

processor kaart:

- pin c-4 output /XFFXX naar io kaart
- pin a-4 output 16 Mhz clock voor ram- en video boards
- pin c-23 input voor /reset signaal van reset schak.

64k dyn. ram kaart:

- pin a-4 input 16 Mhz clock van processor kaart
- pin c-23 input bank select van decoder

io-control kaart:

- pin a-3 input >56K signaal van bank decoder
- pin c-3 input 100hz blokgolf van voedings eenheid
- pin a-4 input select /FXXXX van bank decoder
- pin c-4 input /XFFXX van processor kaart
- pin a-20 output disdec naar bank decoder
- pin a-21 output /FF0XX voor dma floppy
- pin c-21 output /FE080 card select (parallel printer)
- pin a-22 output /FE070 card select (vrij)
- pin c-22 output /FE050 card select (vrij)
- pin a-23 output /FE040 card select (vrij)
- pin c-23 output /FE030 card select (vrij)
- pin a-24 output /FE020 card select (vrij)
- pin c-24 output /FE010 card select (floppy kaart)

floppy kaart:

- pin 17 verbinden met a-23 van systeem backplane (Q clock)
- pin 12 card select input van io-control card

bank decoder:

-74154- (middelste ic)

pin 1	output bank 0XXXX (naar ram kaart)
pin 2	output bank 1XXXX
pin 3	output bank 2XXXX
pin 4	output bank 3XXXX
pin 5	output bank 4XXXX
pin 6	output bank 5XXXX
pin 7	output bank 6XXXX
pin 8	output bank 7XXXX
pin 9	output bank 8XXXX
pin 10	output bank 9XXXX
pin 11	output bank AXXXX
pin 13	output bank BXXXX
pin 14	output bank CXXXX
pin 15	output bank DXXXX
pin 16	output bank EXXXX
pin 17	output bank FXXXX (naar IO kaart)
pin 18	input /vma (buslijn)
pin 19	input disdec van io control kaart
pin 20	input adres 19 (buslijn)
pin 21	input adres 18 (buslijn)
pin 22	input adres 17 (buslijn)
pin 23	input adres 16 (buslijn)

-74ls21- (onderste ic)

pin 12	input adres 15 (buslijn)
pin 10	input adres 14 (buslijn)
pin 9	input adres 13 (buslijn)
pin 8	output >56K naar io control kaart

-74ls74- (bovenste ic)

pin 11	input clock 16 Mhz van processor kaart
pin 9	output clock 8 Mhz voor diverse doeleinden

/vma betekent 'not vma' = actief laag

aansluitingen voor het ECSI 6809 systeem

21 nov 1982 rev 1.0

Modifications for CPU-814a card.

a) (2MHz system)

Component side:

- cut trace small trace between 74LS04 and 74LS74 (16MHz).
- cut trace above 74LS74 between pin-3 and pin-9 from 74LS74.
- cut trace below 74LS74 between thru-hole and pin-5 from 74LS74.
- place wire from trace pin-9 74LS74 to thru-hole below 74LS74 (EXTAL).

Solder side:

- place wire between pin-12 from 74LS08 and pin-14 from 74LS08.

b) (make /XFEXX signal)

Remove 74LS30 above the 74LS08.

Component side:

- cut trace above 74LS30 between thru-hole and pin-13 from 74LS30.

Solder side:

- cut trace pin-9 from 74LS02.
- place wire between pin-13 and pin-14 from 74LS30.
- place wire between pin-9 and pin-7 from 74LS02.

c) (address pullup's)

Component side:

- place R 4K7 between pin-14 from 74LS30 and thru-hole from 6809 pin-22 (A14).
- place R 4K7 between pin-14 from 74LS30 and thru-hole from 6809 pin-23 (A15).

Solder side:

- place wire pin-11 from 74LS157 to pin-6 from Rnet-3 (A12).
- place wire pin-14 from 74LS157 to pin-6 from Rnet-4 (A13).

d) (DATRAM timing)

Component side:

- cut trace above 74LS08 between thru-hole and pin-5 from 74LS08.
- cut trace below 74LS08 between thru-hole and pin-5 from 74LS08.
- place wire between the two thru-holes.

Solder side:

- place wire from pin-5 74LS08 to thru-hole below the 74LS08 (Q from 6809).

e) (bus termination)

Solder side:

- place wire from AC64 pin-c20 to Rnet-1 pin-7 (R/W).
- place wire from AC64 pin-a21 to Rnet-1 pin-2 and Rnet-2 pin-2 (/res).

f) (DMA)

Component side:

- cut trace above 74LS244 from pin-15.
- cut trace above 74LS32 from pin-13.
- place wire between pin-5 from 74LS74 and pin-13 from 74LS32.

Solder side:

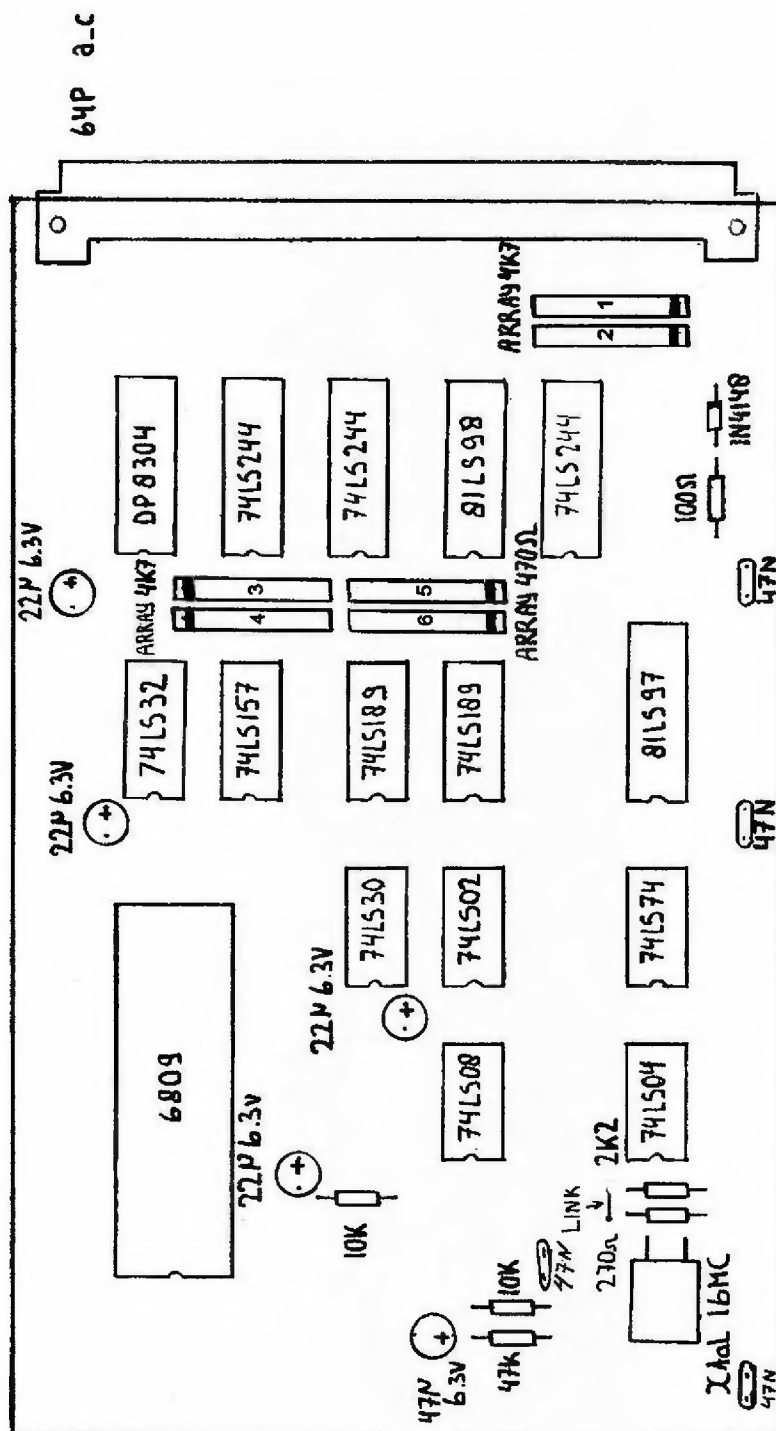
- cut trace between pin-2 and pin-6 from 74LS74.
- place wire between pin-6 from 6809 and pin-2 from 74LS74.
- place wire between pin-2 from 74LS74 and pin-15 from 74LS244.
- place wire between pin-2 from 74LS244 and pin-8 from 74LS98.
- place wire between pin-8 from 74LS98 and pin-3 from 74LS74.

g) (hard reset)

Replace 74LS04 by 74ACT14

Solder side:

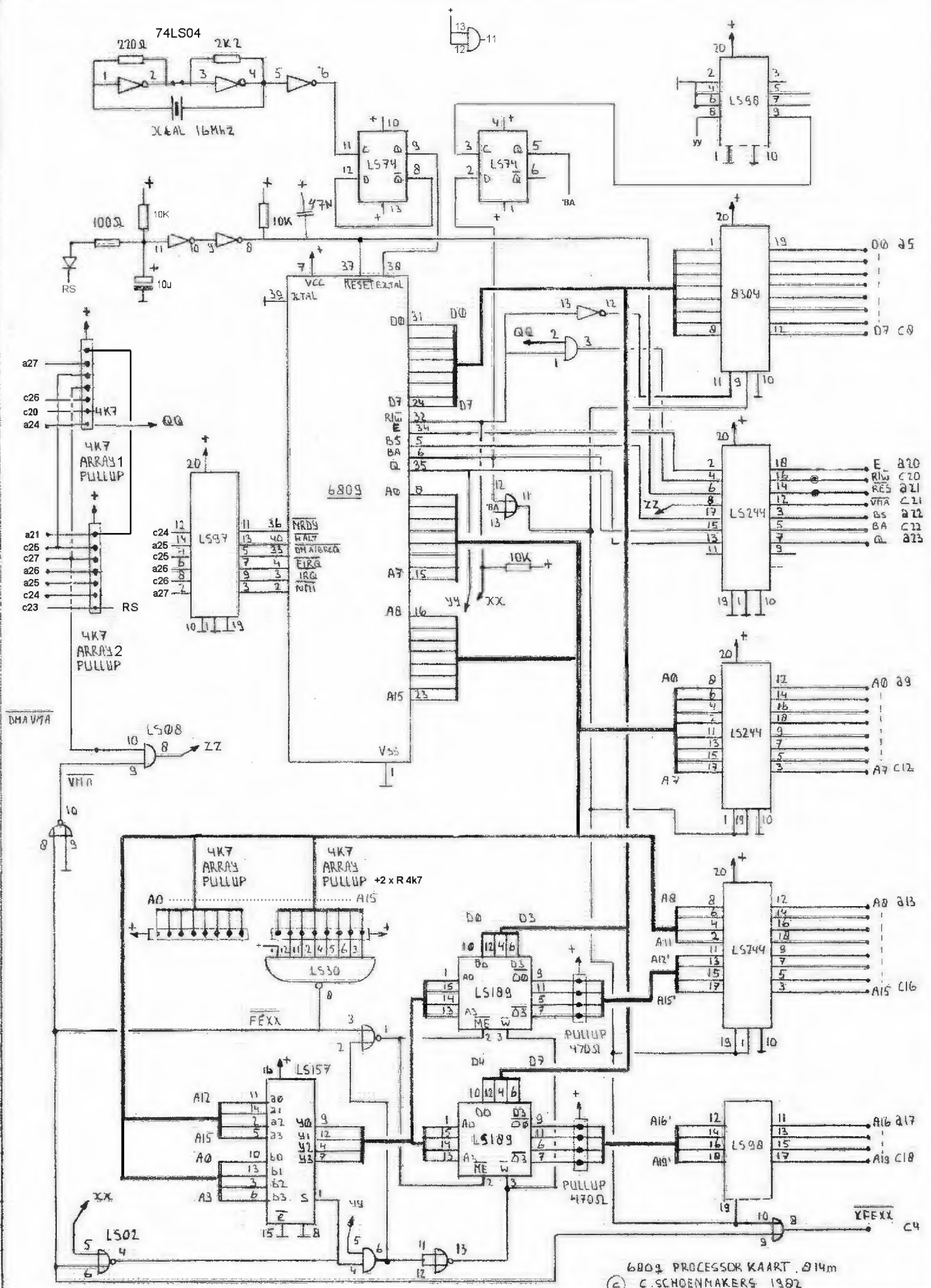
- cut trace to pin-14 from 74LS244 (/res).
- place wire between AC64 pin-a21 and pin-3, pin-5, pin-7 from 74LS98.
- place wire from pin-6 from 74LS244 to pin-2, pin-4, pin-6 from 74LS98.

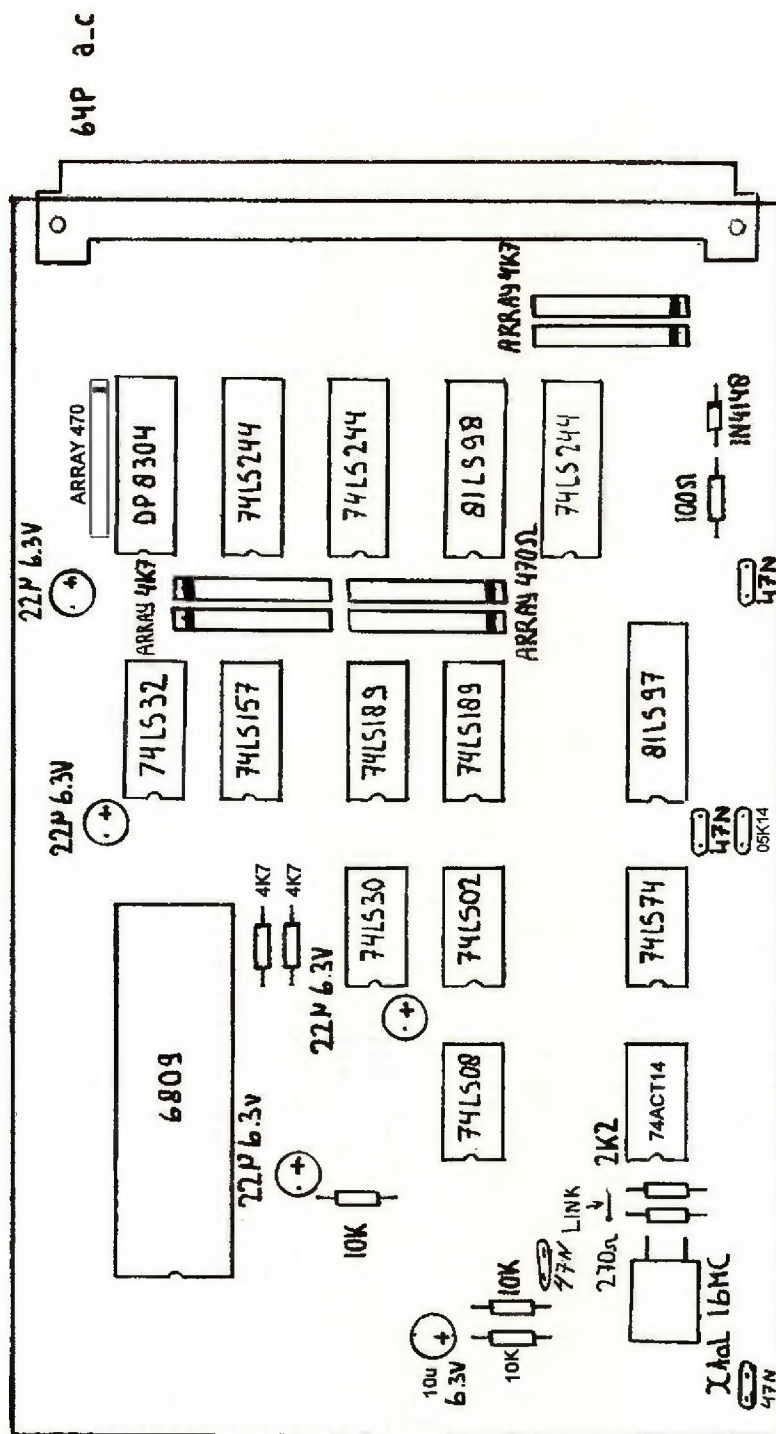


ARRAY 7 WEEKST 1 COMMON

ALLEEN IC VOETEN VOOR
6809 - 7415189

CPU 814m

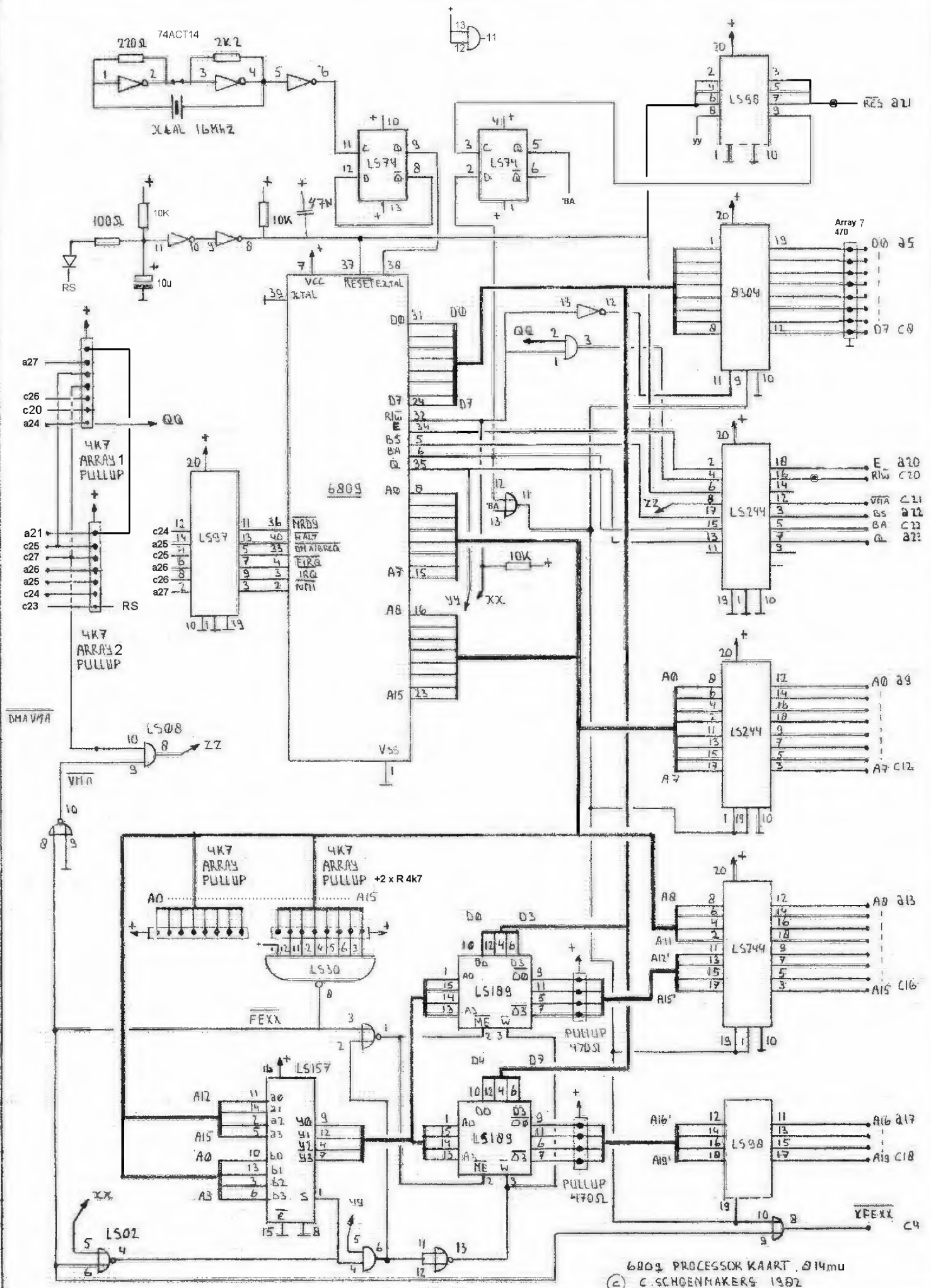




ARRAY 7 WEEKST 1 COMMON

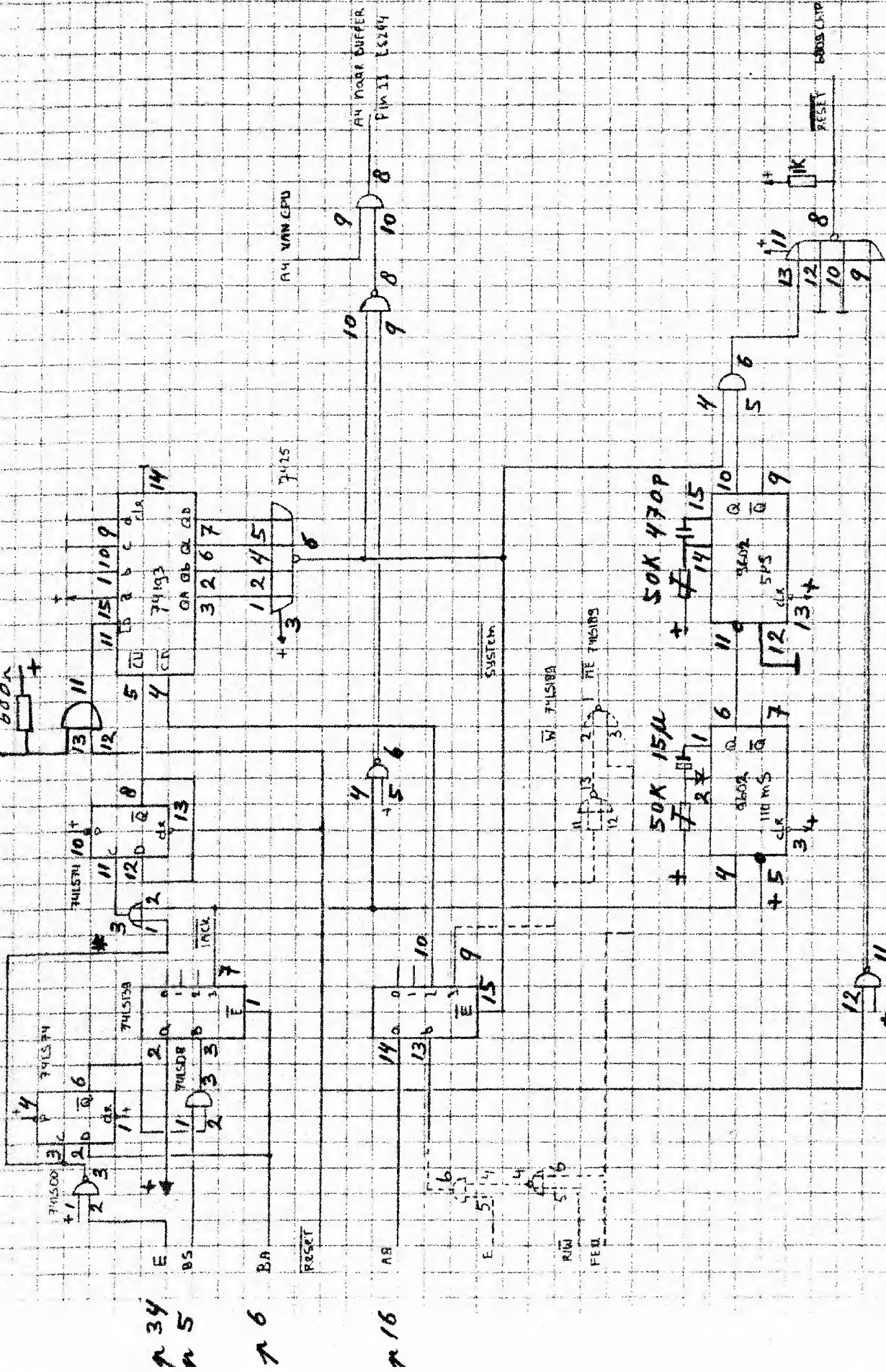
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65809 - 7415189

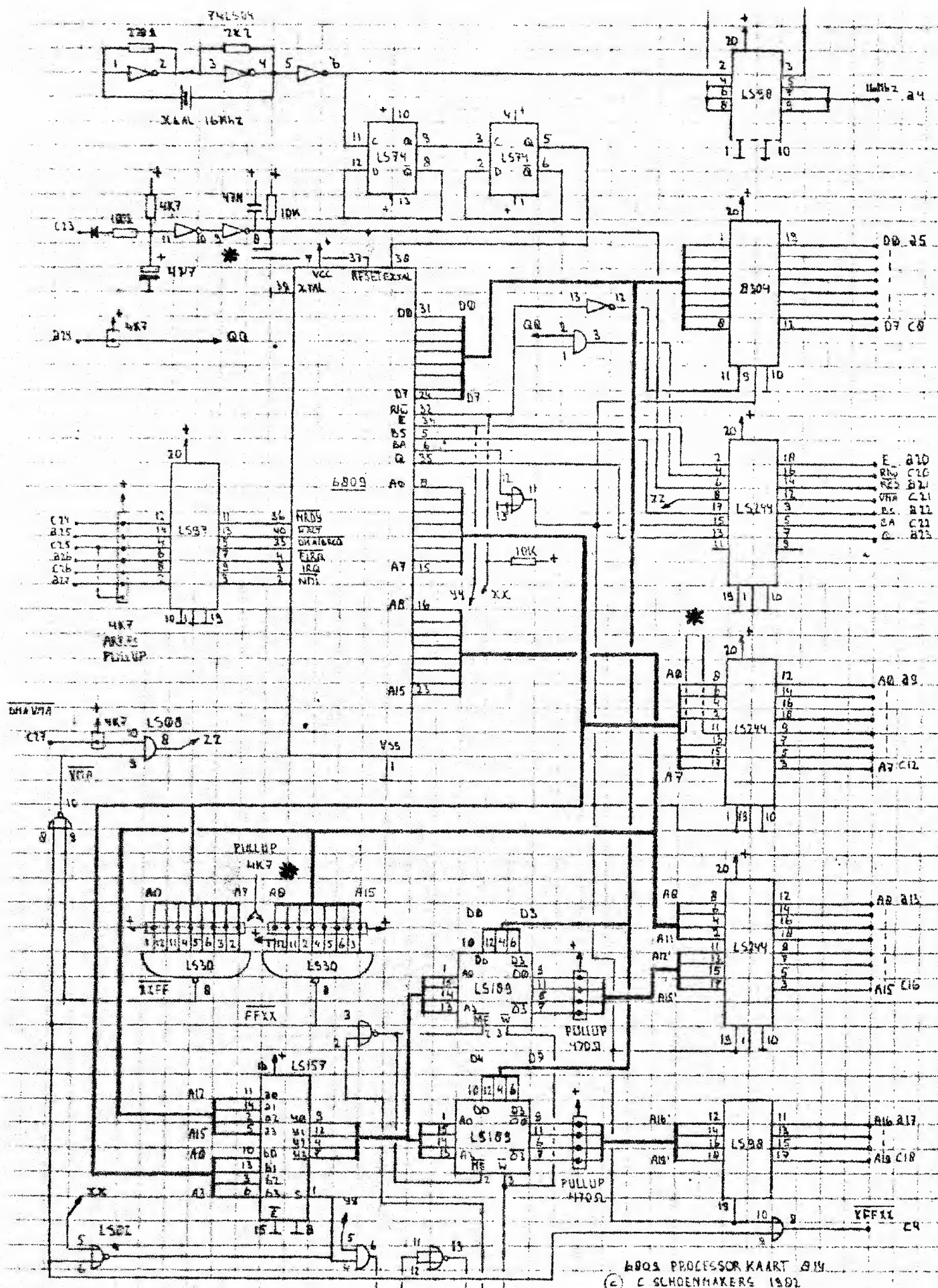
CPU 814mu



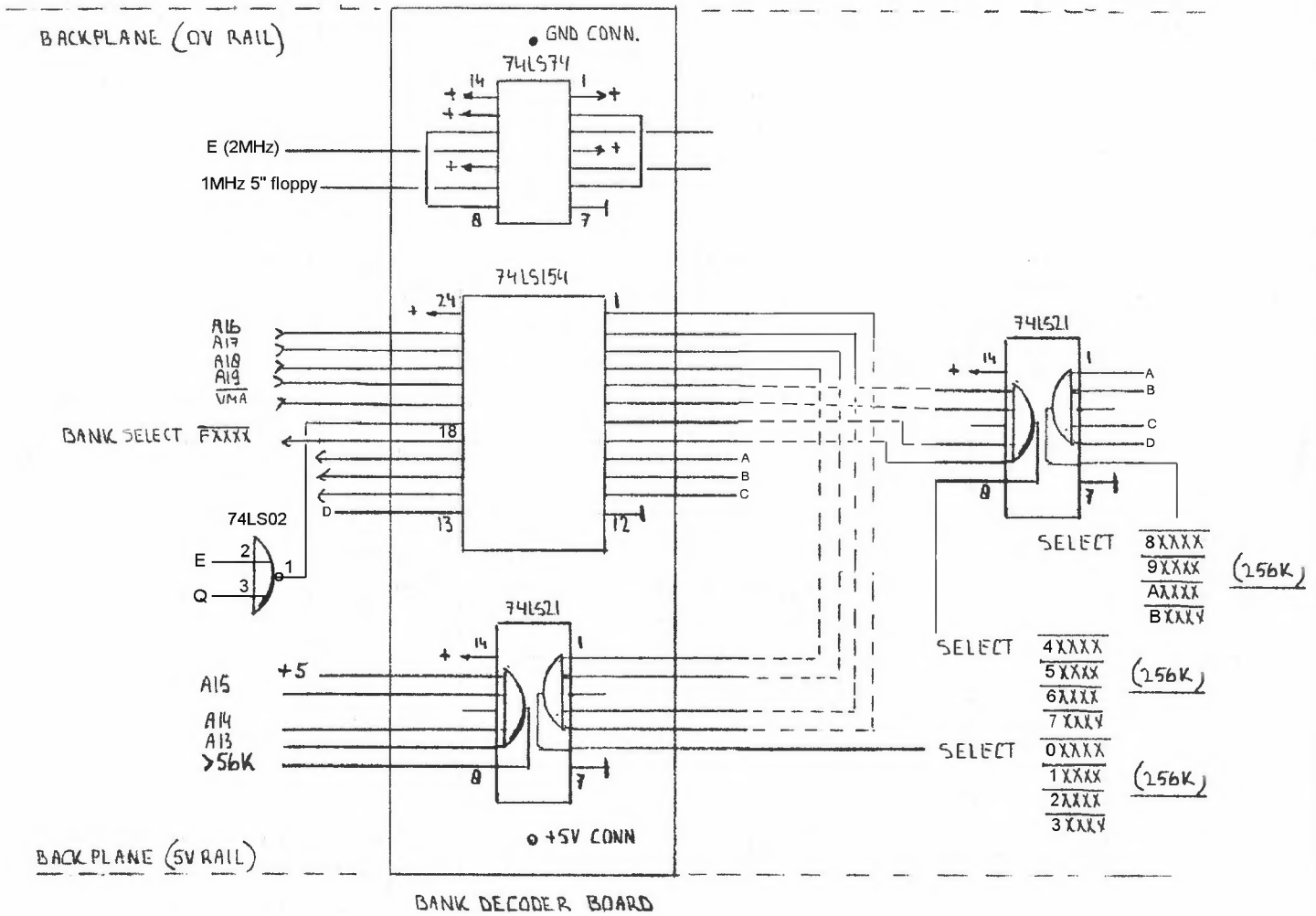
* CPU

on/off





4809 PROCESSOR KAART 811
(c) C. SCHOENMAKERS 1982



Bank Decoder - μ

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```
CUPL(WM)      5.0a Serial# 60008009
Name          Decoder; /* Replace 74LS154 & 3x 74LS21 & 74LS74 & 74LS02 */
Partno       CS0001; /* Select 4 Banks of 256K, 1MHz clock floppy */
Revision     00;
Date         10/16/19;
Designer     JAC;
Company      PKS;
Location     None;
Assembly     None;
Device       q20v8a;
```

```

/**** INPUT PINS ****/
Pin 1 = Clk; /* = Q */
Pin 2 = Q;
Pin 3 = E;
Pin 4 = A13;
Pin 5 = A14;
Pin 6 = A15;
Pin 7 = A16;
Pin 8 = A17;
Pin 9 = A18;
Pin 10 = A19;
Pin 11 = VMA;
Pin 12 = GND;

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/**** OUTPUT PINS ****/
Pin 13 = 0V; /* enable */
Pin 14 = nc0;
Pin 15 = 56K;
Pin 16 = FXXXX;
Pin 17 = BANK0;
Pin 18 = BANK1;
Pin 19 = BANK2;
Pin 20 = BANK3;
Pin 21 = Q2; /* 1MHz */
Pin 22 = 2Q; /* 4MHz */
Pin 23 = nc1;
Pin 24 = VCC;

```

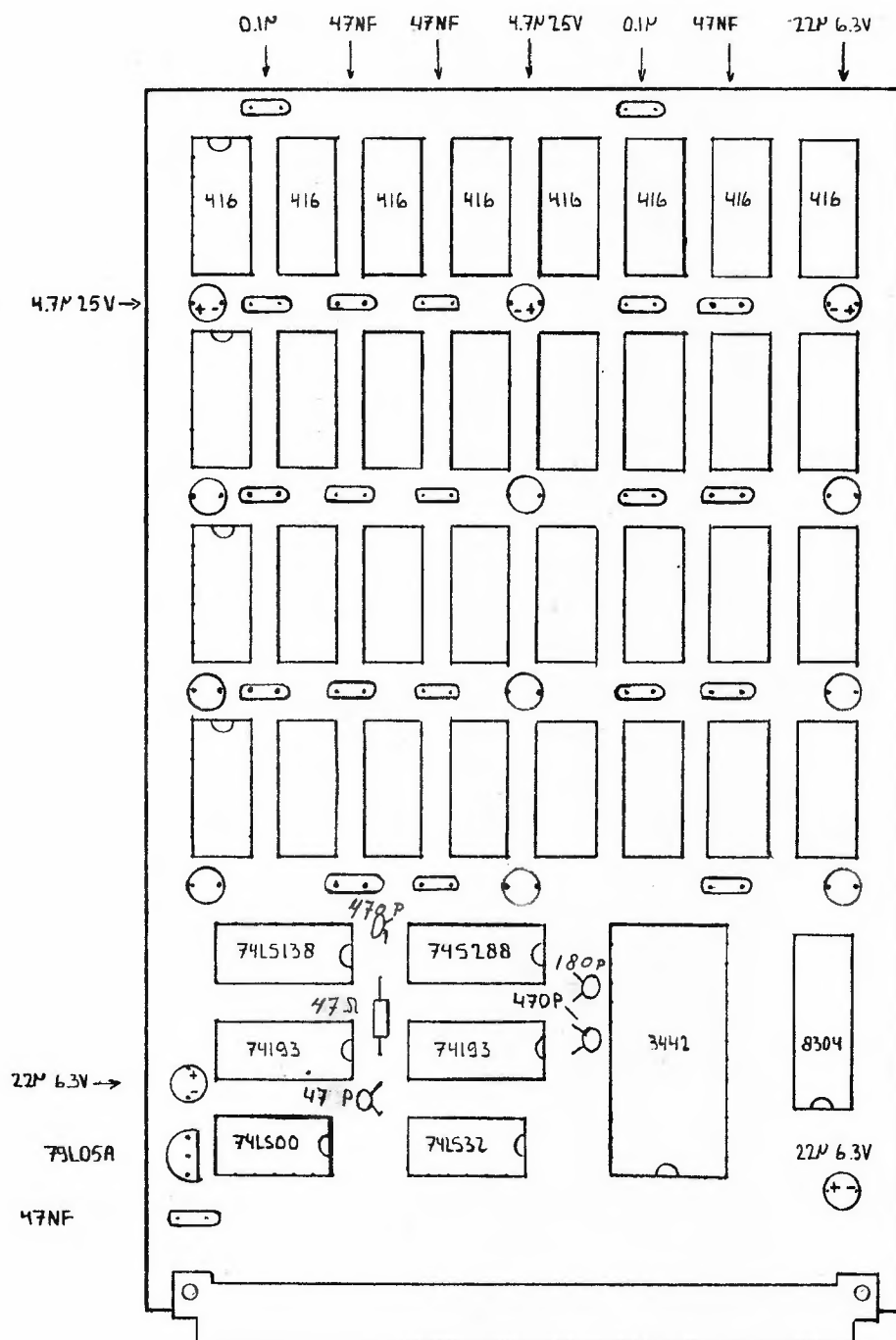
```

/*** Logic ***/
2Q = E $ Q;
Q2.d = !Q2;
BANK3 = !(A18 & A19) # !(Q # E) # VMA;
BANK2 = !(A18 & A19) # !(Q # E) # VMA;
BANK1 = !(A18 & A19) # !(Q # E) # VMA;
BANK0 = !(A18 & A19) # !(Q # E) # VMA;
FXXXX = (A16 & A17 & A18 & A19);
56K = A13 & A14 & A15;

```

Correction for RAM-815a card.

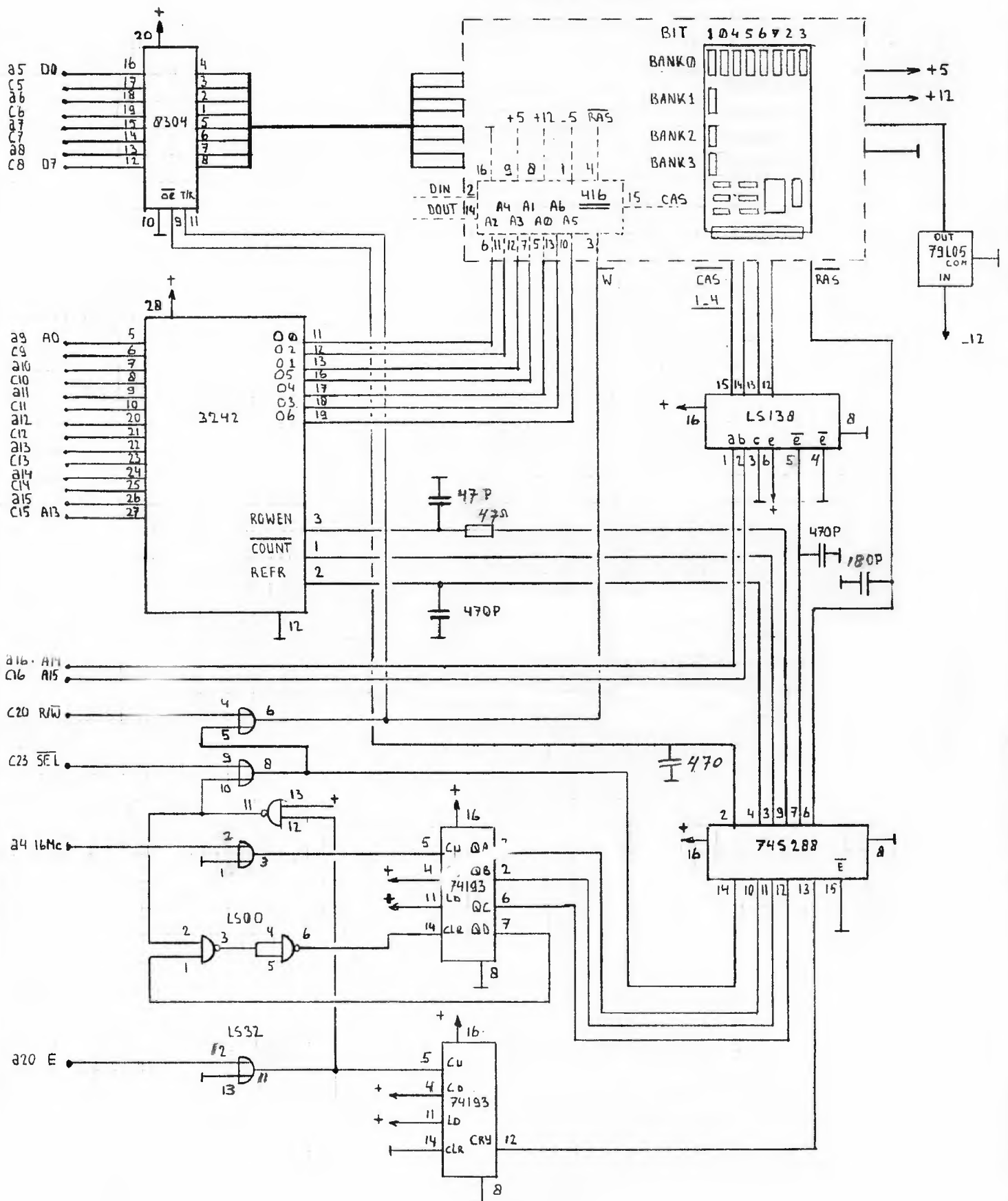
- a) E clock connected to port 13, 12 and 11
16Mhz connected to port 3, 2 and 1

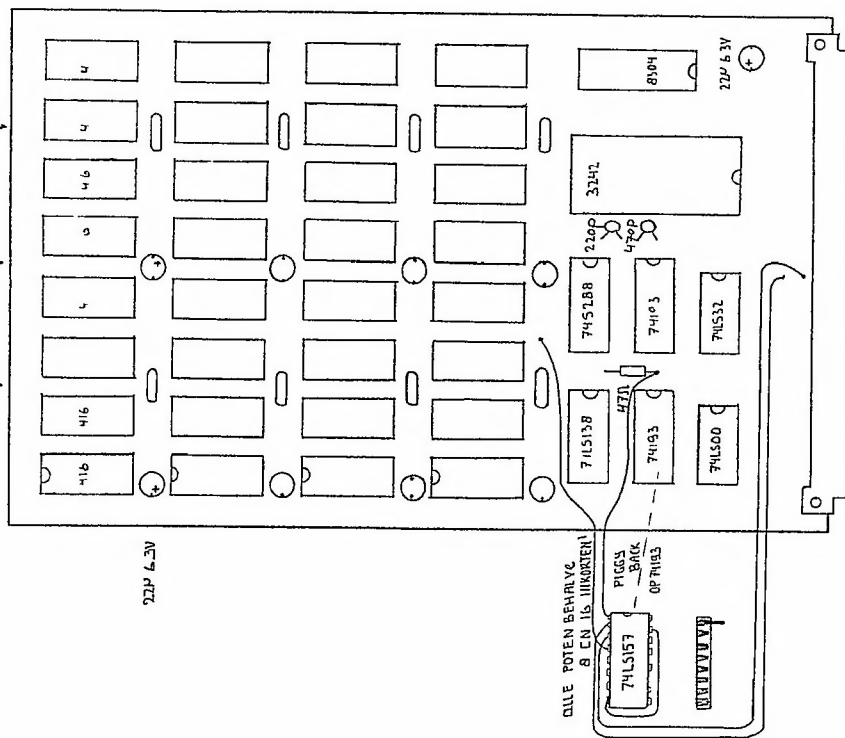


AAN SOLDEERZIJDE DE VOLGENDE CONDENSATOREN

470PF TUSSEN 4 EN 5 VAN 74LS138
 470PF TUSSEN 9 EN 10 VAN 8304
 GEBRUIK IC VOETEN ALLEEN VOOR
 4116 - 74LS288 - 3442

MEMORY ARRAY (4x8) x 8116

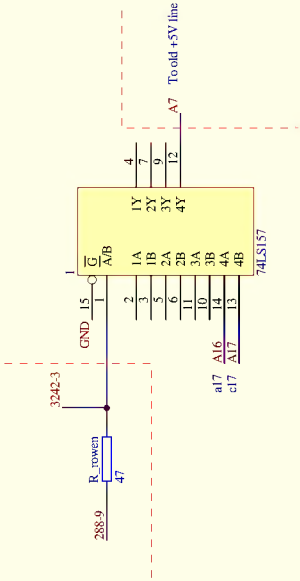


[illegible]

AAN SCILCEERZJDE DE VOLGENDE CONDENSATOREN

4-0DF TUSSEN 9 EN 10 VAN 8304
470 PF TUSSEN 4 EN 5 VAN 745130
22024 TUSSEN PINNEN VAN 745200 EN 0VOLT
GEENWIJK IC VOER EN ALLEEN VOLK
8764 - 745200 - 3342

D	C	B	A
1	2	3	4
1	2	3	4
1	2	3	4
1	2	3	4
1	2	3	4
1	2	3	4
1	2	3	4
6	5	6	6



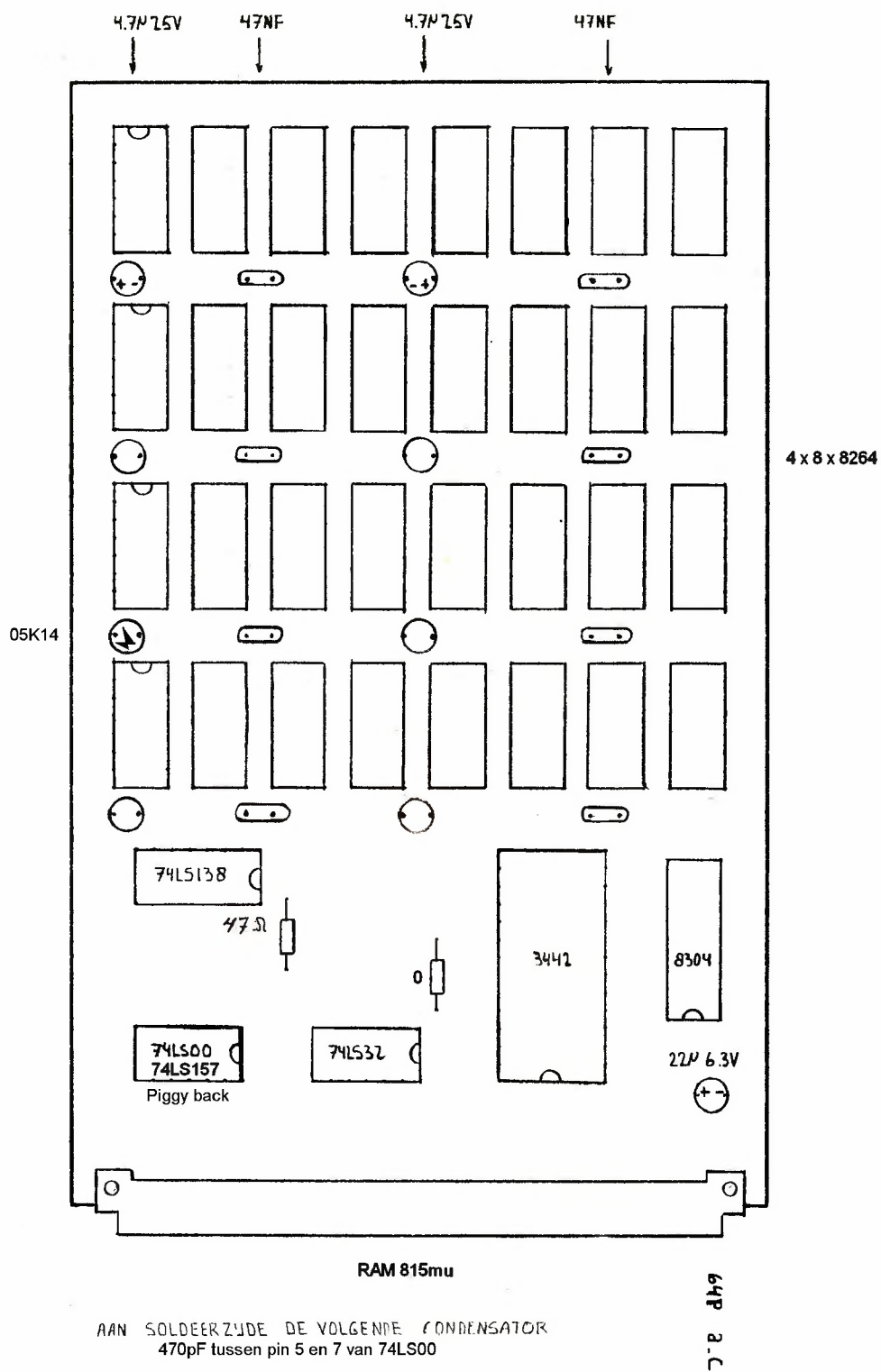
Modification 64K RAM card > 256K RAM card

- Remove 79L05 and all condensators on the -5V line
- Remove 47pF condensator
- Remove 416 chips
- Cut +5V by pin 16 from 74S288
- Cut +12V by AC64 connector
- Place wire from +12V trace to +5V by AC64 connector
- Piggy back 74LS157 on the 74LS00
- Place 8264 or NEC4164 chips.....

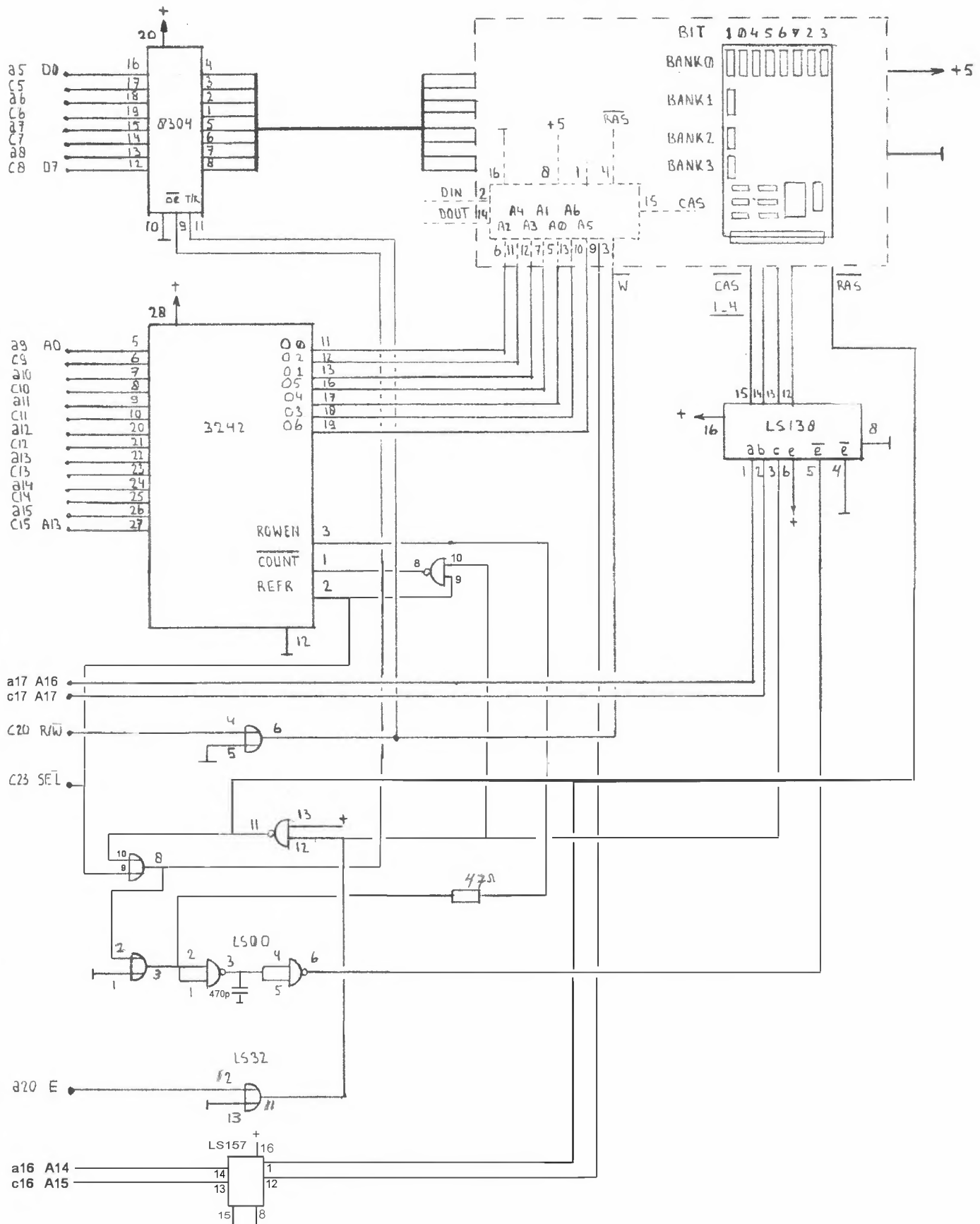
Linear addressing:

- Cut A14 and A15 traces by 74LS00 on component side.
- Connect A14 trace with 74LS157 - pin 14
- Connect A15 trace with 74LS157 - pin 15
- (between the 74LS00 and AC64 connector)
- Connect A16 with 74LS138 - pin 1
- Connect A17 with 74LS138 - pin 2

Title			
Size	Number	Revision	
B			
Date:	12-Oct-2020	Sheet	of
File:	Z:\CS System\CS Computer data\RAM 811\RAM4656K.dib		



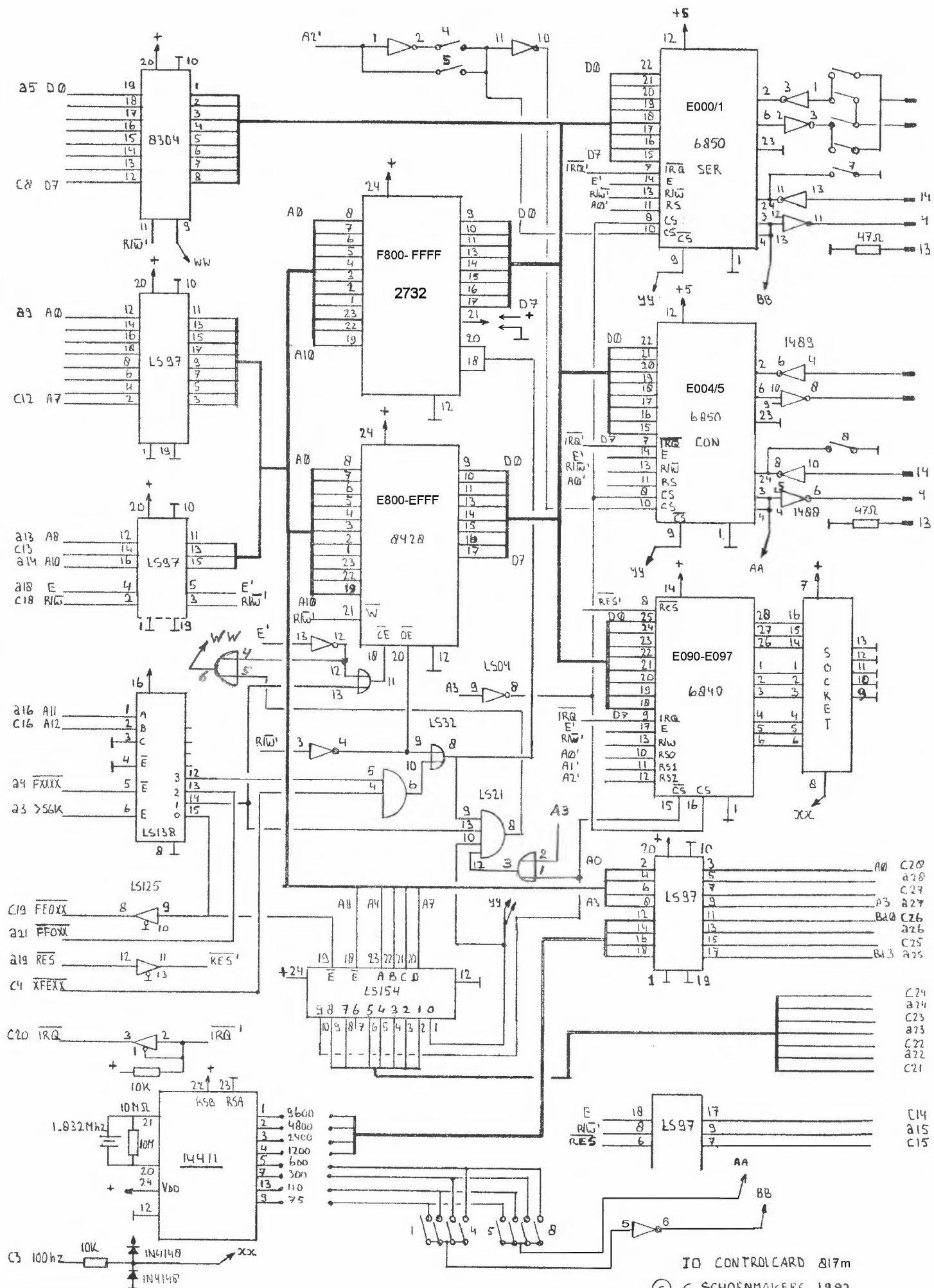
MEMORY ARRAY (4x8) x 8264



Modifications for MON-817 card.

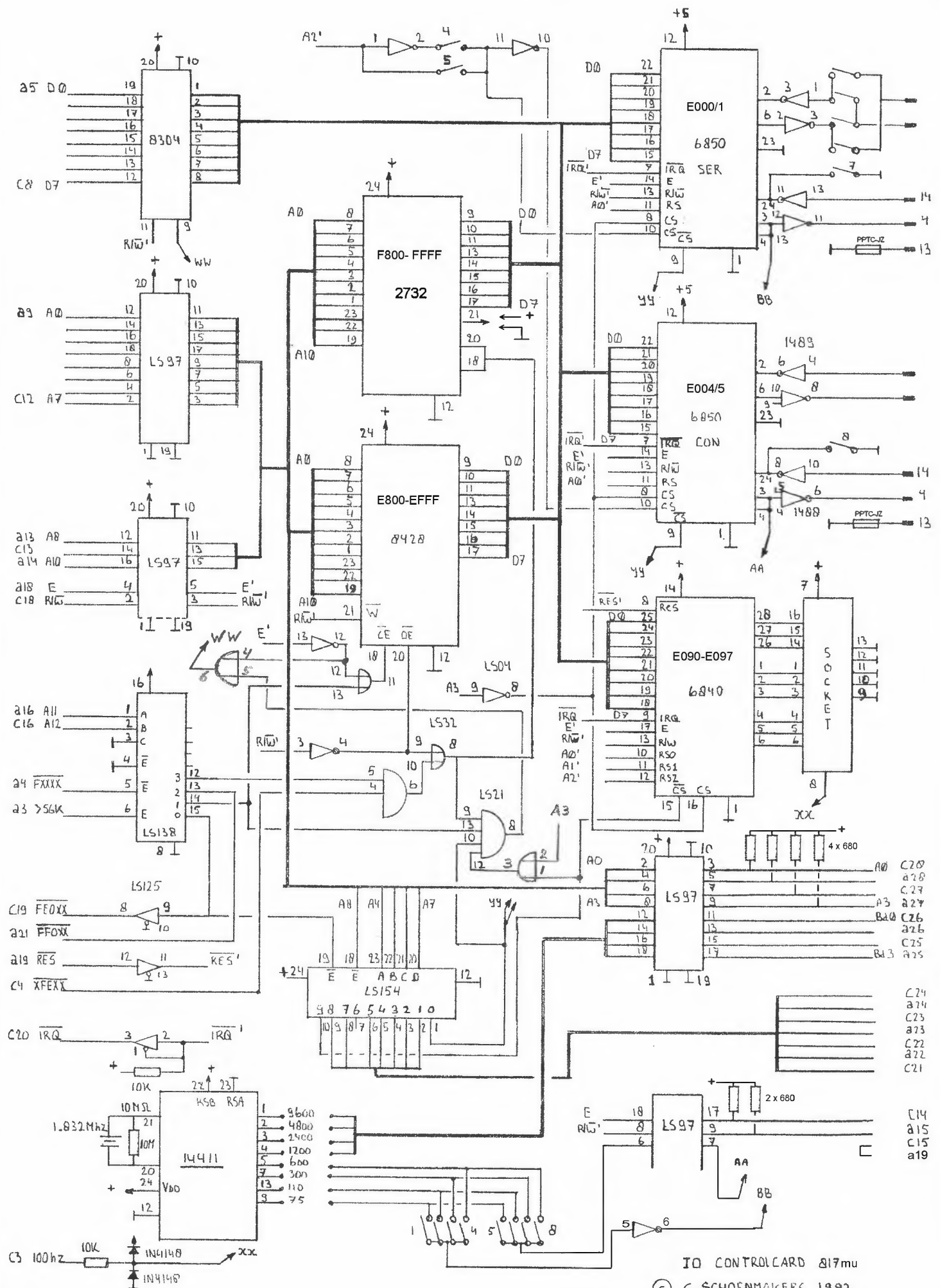
- a) (2MHz System)
EPROM must be 350 nsec.
- b) (Clean DATA bus)
Cut trace between 74LS21 pin-8 and DP8304 pin-9.
Place wire 74LS32 pin-4 to 74LS32 pin-12.
Place wire 74LS32 pin-5 to 74LS21 pin-8.
Place wire 74LS32 pin-6 to DP8304 pin-9.
- c) (Schematic error 1)
pin-18 of the lower 81LS97 is not connected to E' but to E.
- d) (Schematic error 2)
Between pin-10 of the 74LS154 and pin-12 of the 74LS21
is a 74LS32 port present:

pin-10 of the 74LS154 is connected to pin-1 of the 74LS32
pin-12 of the 74LS21 is connected to pin-3 of the 74LS32
pin-2 of the 74LS32 is connected to A3.
- e) (Chip load)
The load on the MC14411 chip AA and BB can get to high.
See MON - 817m and MON - 817mu for modification.
- f) (Ground spike problems)
Replace the two 47 ohm resistors by 50mA wirefuse.



IO CONTROL CARD 817m

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Modifications for Floppy-818 card.

a) (Design error)

Piggyback 74LS08 on 74LS32 next to AC64.

Cut trace between 74LS640 pin-19 and Gnd.

Place wire 74LS640 pin-19 and 74LS08 pin-3.

Place wire 74LS273 pin-11 and 74LS08 pin-2.

Place wire WD1791 pin-3 and 74LS08 pin-1.

Cut trace between 74LS02 pin-8 and Gnd.

Place wire 74LS02 pin-8 and 74LS273 pin-5.

Cut trace between 74LS32 pin-9 and 74LS240 pin-15 & pin-16.

Place wire 74LS32 pin-9 and Gnd.

b) (2MHz System)

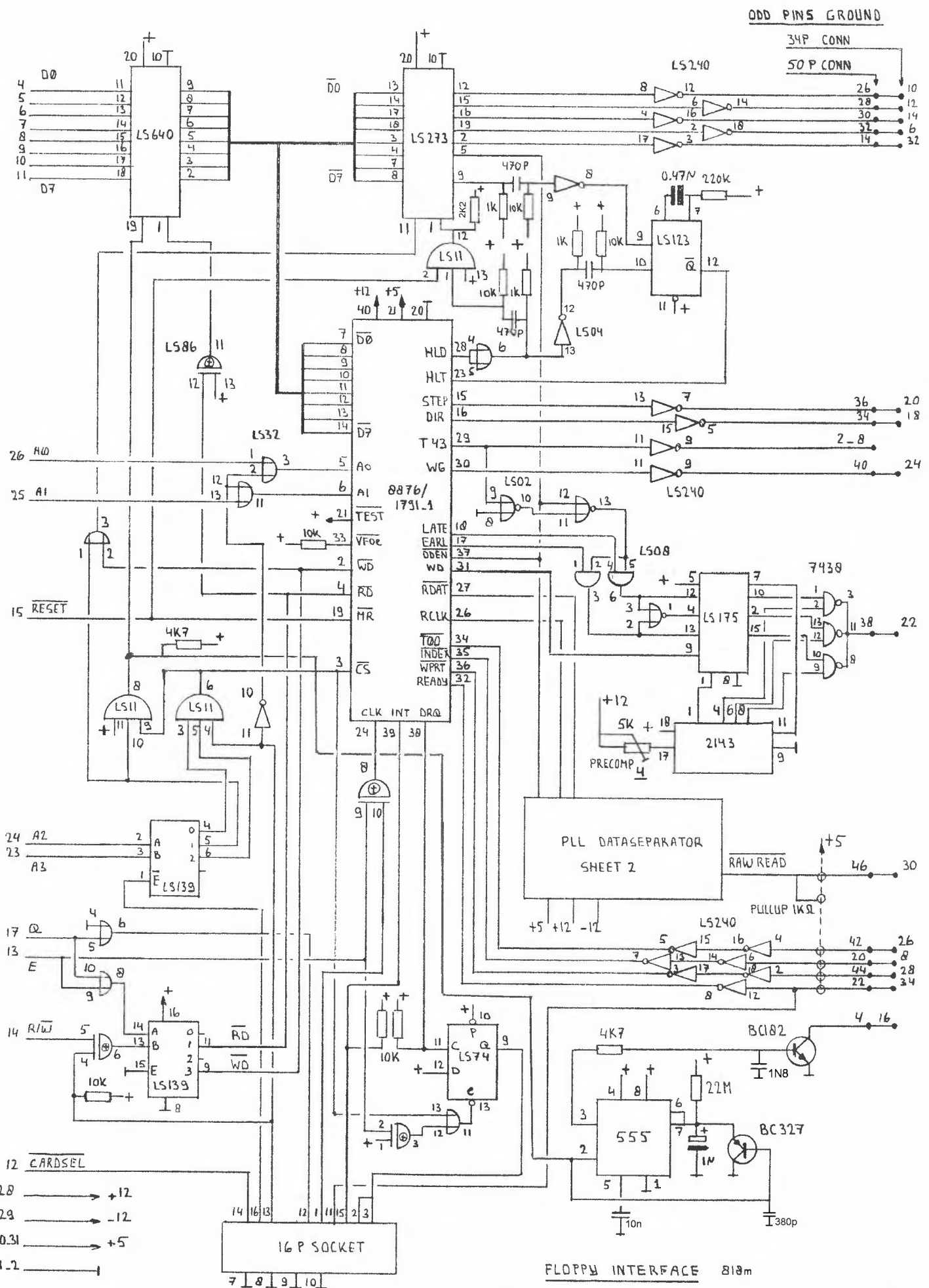
Q and E clock must be connected!

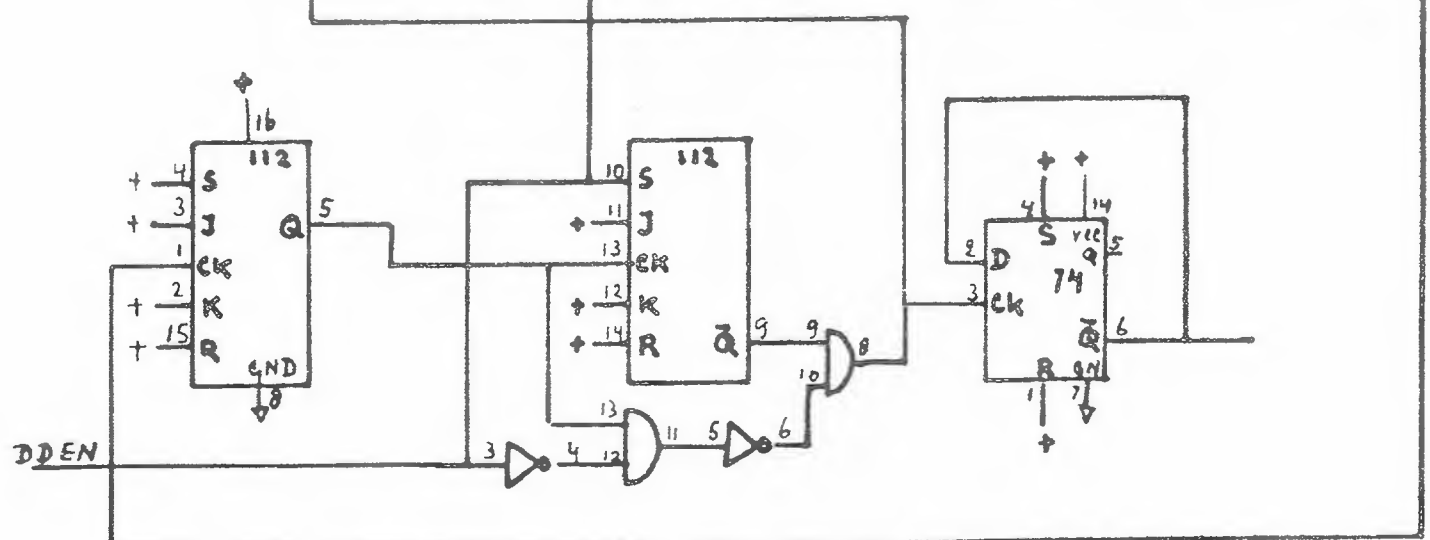
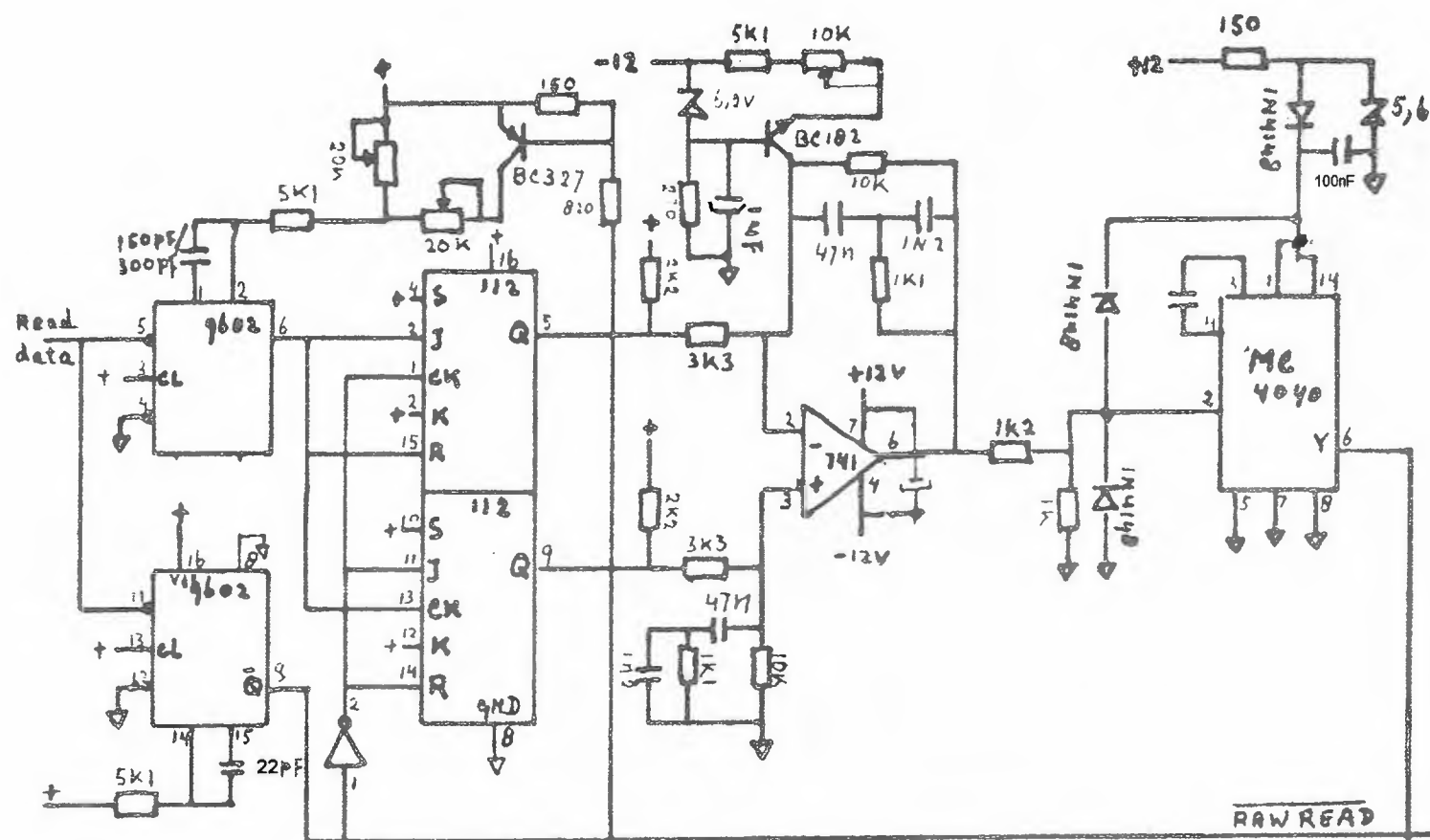
NOT AVAILABLE

Modifications for Floppy-818A card.

- a) (2MHz System)
Q and E clock must be connected!
- b) (Motor on)
Cut trace between WD1791 pin-3 and NE555 pin-2.
Place wire between NE555 pin-2 and 74LS640 pin-19.
- c) (Schematic error)
For pin-1 and pin-2 on the 74LS02 read pin-12 and pin-13!
- d) (WD specs)
Use 100ns read puls, change 82pF in VCO to 22pF.
- e) (Glitches)
Connect 380pF from NE555 pin-2 to Gnd.
Connect 1n8 from basis BC182 to Gnd.

Replace 47nF next the 74LS273 by 1uF tantaal.
Replace 47nF next the WD2143 by 150nF MKM.
- f) (Logic level)
Connect 2K2 from pin-1 of the 74LS273 to VCC.
- g) (???)
Place wire jumper socket pin-11 and 8" connector pin-4





PLL (CS)

Modifications for DMA-816a card.

- a) (2MHz system)
 - Cut trace between 6844 pin-40 and 74LS32 pin-2.
 - Place wire 6844 pin-40 to 74LS32 pin-3.

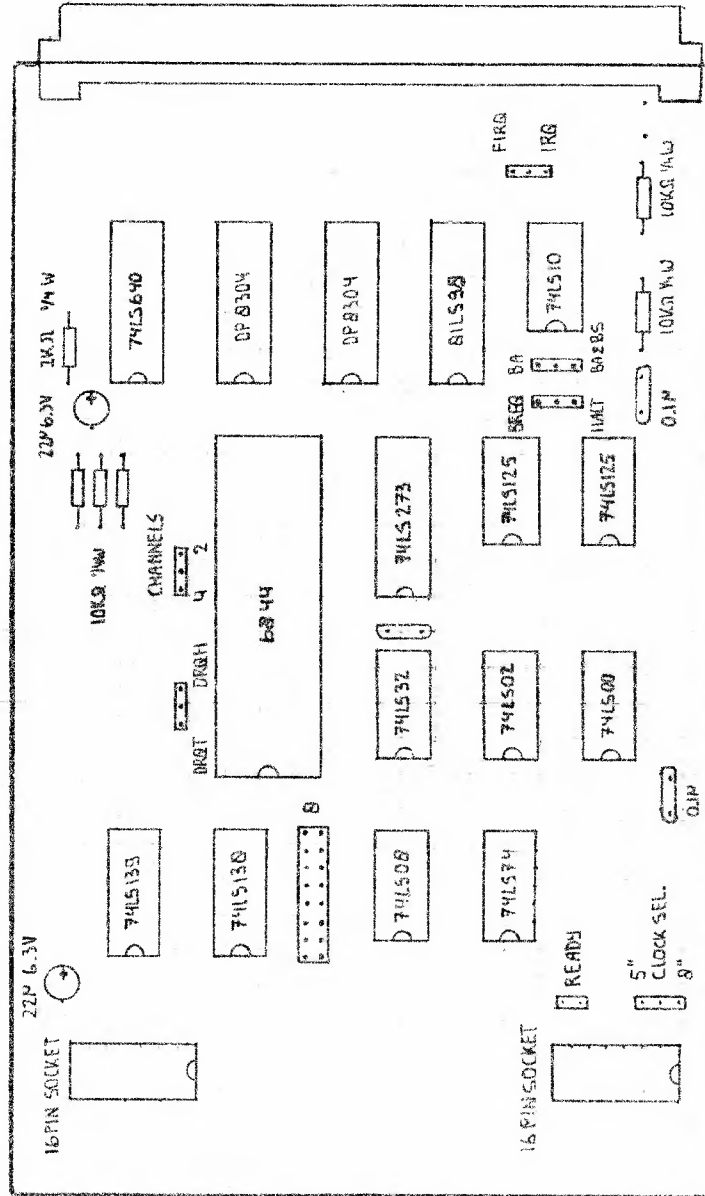
- b) (Schematic error 1)
 - pin-6 of 74LS138 is connected to pin-3 of the 74LS32,
 - and not to pin-2 of the 74LS32!

- c) (Schematic error 2)
 - pin-2 and pin-3 from the 74LS02 is not connected
 - to pin-3 of the 74LS32, but to pin-2 of the 74LS32!

649 9-C

SCIENCE CHANNELS

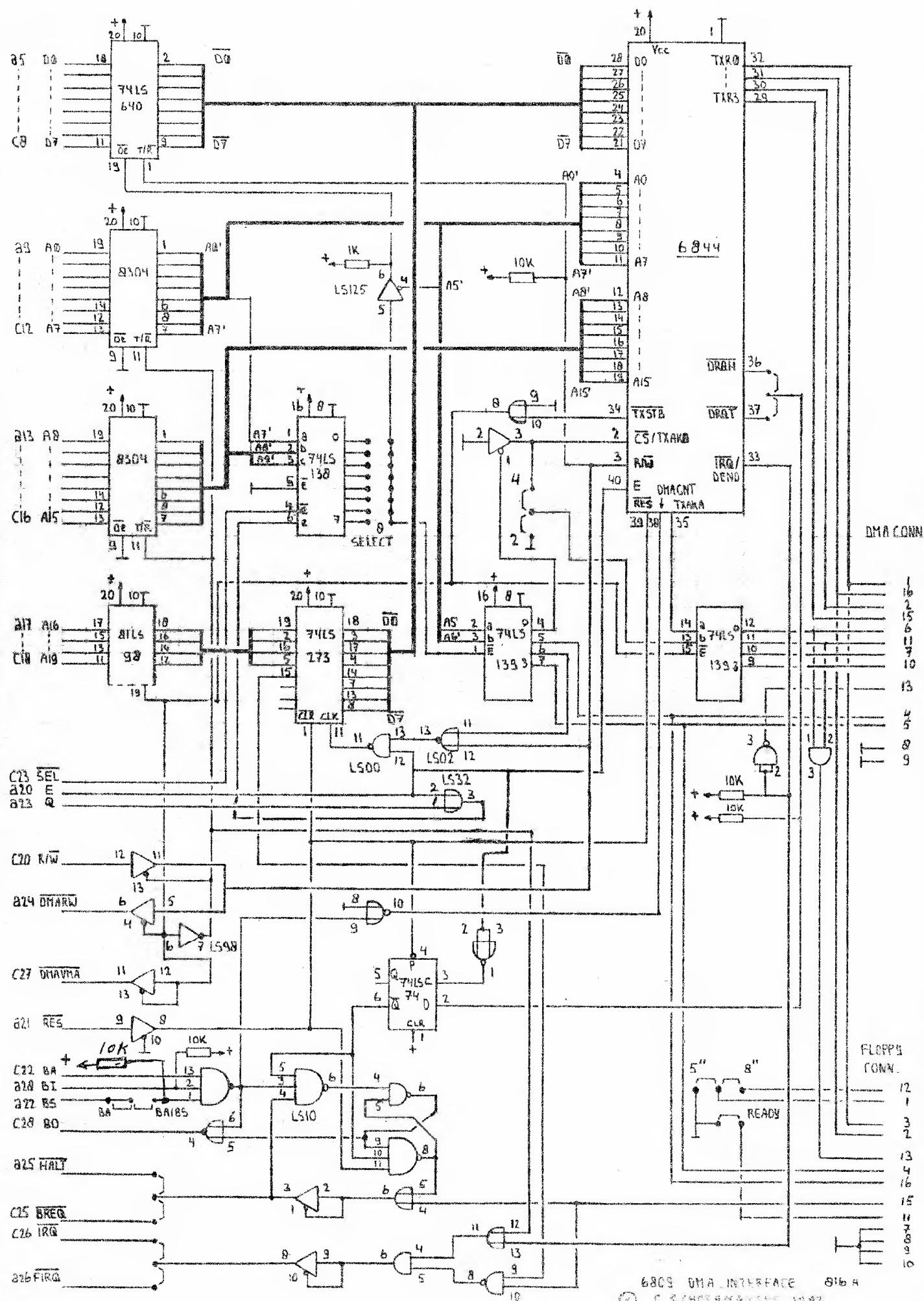
MS-9 277



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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1000

COCKNOG: 5' OF 3" EN EVENT DEEL READY



Modifications for SASI-824 card.

a) (Card error, 824 only) Chips marker

Place 74LS08 at Spare location.

Wire pin-14 to Vcc (hole-16)

.

Component side:

Cut trace between pin-9 74LS27 and pin-9 74LS74 next LS651.

Cut trace between 74LS74 pin-4 and Vcc.

Cut trace between 74LS74 pin-4 and pin-10.

Cut trace at pin-1 74LS139.

Solder side:

Cut trace at pin-10 from 74LS74 next 74LS651.

Cut trace at pin-11 from 74LS74 next 74LS651.

Cut trace between pin-15 74LS138 and pin-12 74LS00.

Cut trace between pin-11 74LS138 and pin-13 74LS00.

Cut trace at pin-6 74LS139.

Cut trace at pin-7 74LS139.

Wire pin-10 74LS74 to Vcc.

Wire pin-13 74LS139 to Gnd.

Wire pin-1 to pin-11 74LS139.

Wire pin-9 to pin-10 74LS27.

Wire pin-12 74LS00 to pin-6 74LS08.

Wire pin-13 74LS00 to pin-11 74LS32.

Wire pin-11 74LS138 to pin-5 74LS32.

Wire pin-15 74LS138 to pin-12 74LS32.

Wire pin-4 74LS32 to pin-3 74LS14.

Wire pin-6 74LS32 to pin-5 74LS08.

Wire pin-13 74LS32 to pin-4 74LS14.

Wire pin-4 74LS08 to pin-5 74LS74 the middle one.

Wire pin-8 74LS08 to pin-21 74LS651.

Wire pin-9 74LS08 to pin-7 74LS139.

Wire pin-10 74LS08 to pin-5 74LS139.

Wire pin-12 74LS08 to pin-6 74LS139.

Wire pin-13 74LS08 to pin-4 74LS139.

Wire pin-11 74LS08 to pin-11 74LS14.

Wire pin-3 74LS14 to pin-50 50pin connector.

Wire pin-14 74LS139 to pin-42 50pin connector.

Wire pin-15 74LS139 to pin-48 50pin connector.

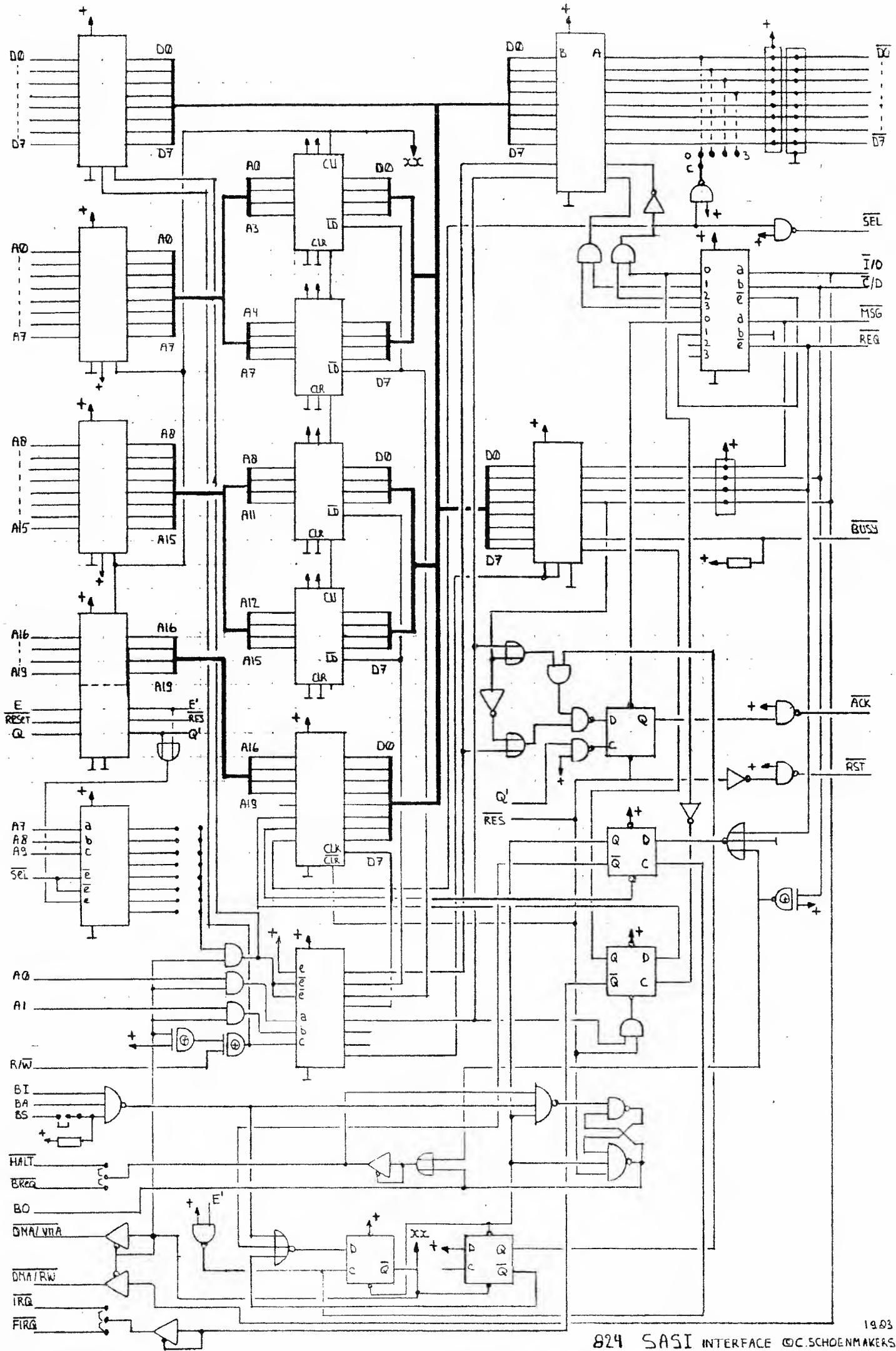
b) (2MHz system) 74LS138 marker 2MHz.

Component side:

Cut trace at pin-6 from 74LS138.

Solder side:

Connect pin-6 from 74LS138 to VCC.



Modifications for SASI-824a card.

a) (2MHz system) 74LS138 marker 2MHz.

Solder side:

Cut trace between pin-6 74LS138 and pin-3 81LS97.

Connect pin-6 from 74LS138 to VCC.

b) (IRQ problem) Chips marker *

Component side:

Cut trace between 74LS74 pin-4 and pin-11.

Solder side:

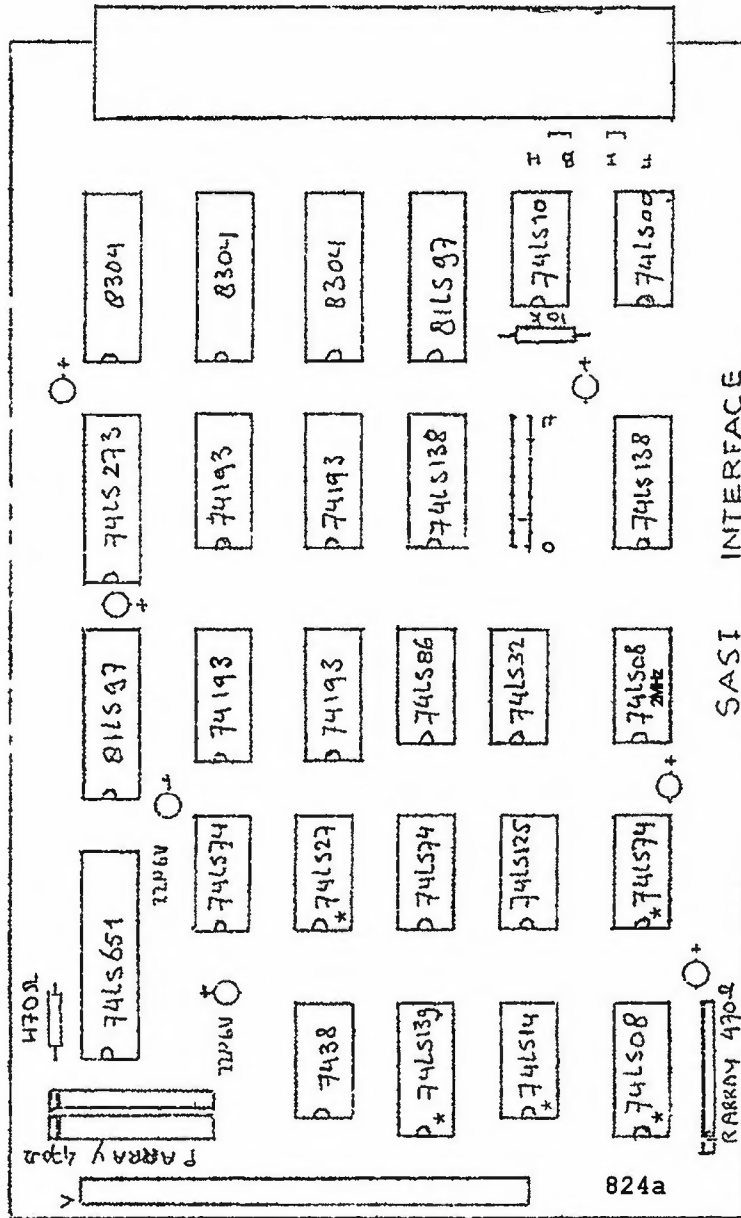
Cut trace between 74LS74 pin-11 and 74LS139 pin-11.

Wire 74LS139 pin-4 to 74LS74 pin-4.

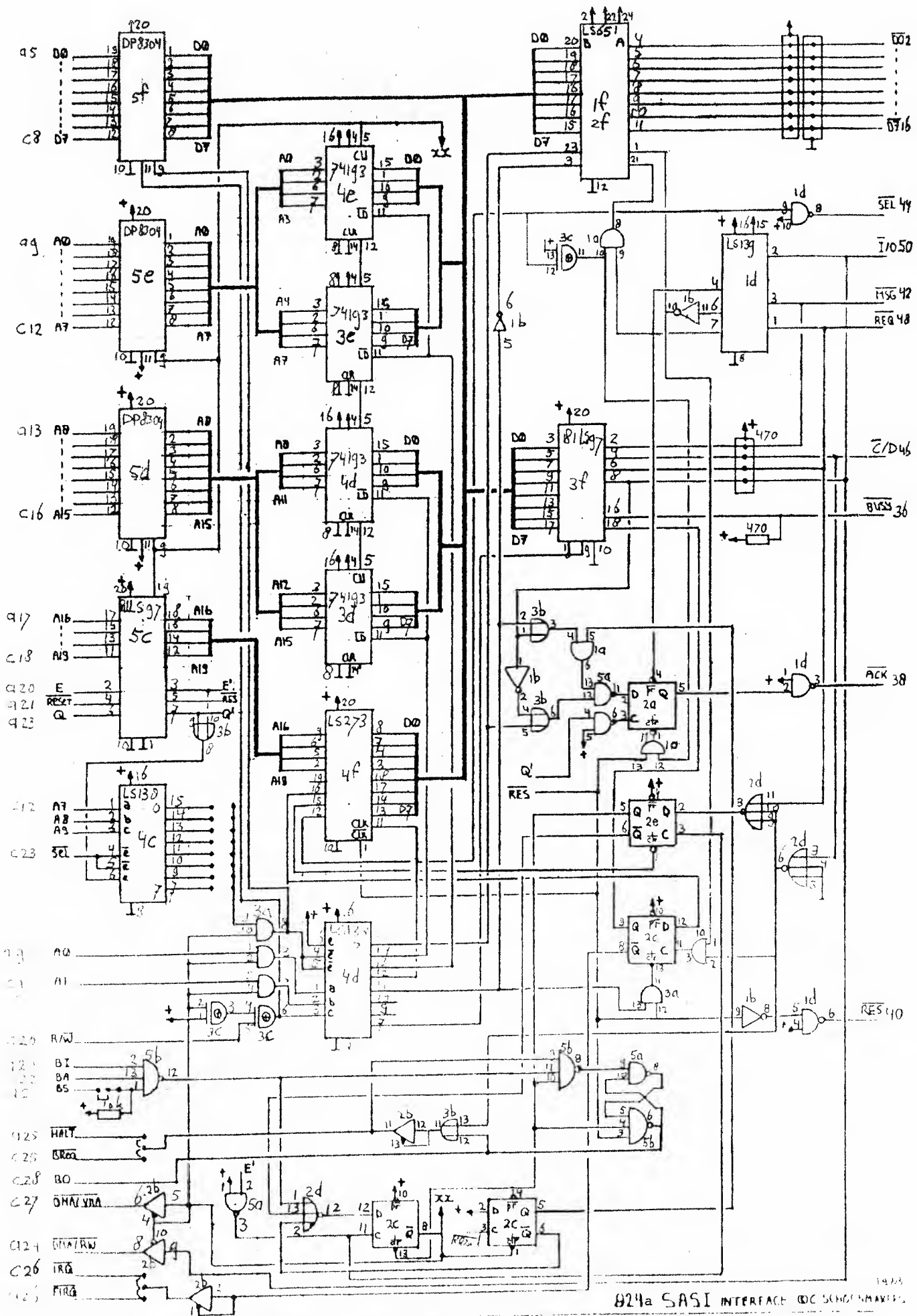
Wire 74LS27 pin-6 to 74LS08 pin-2.

Wire 74LS14 pin-10 to 74LS08 pin-1.

Wire 74LS08 pin-3 to 74LS74 pin-11.



TANTIAL 22 μ F 16V REV a 840723



DMA/BREQ PATCH SASI

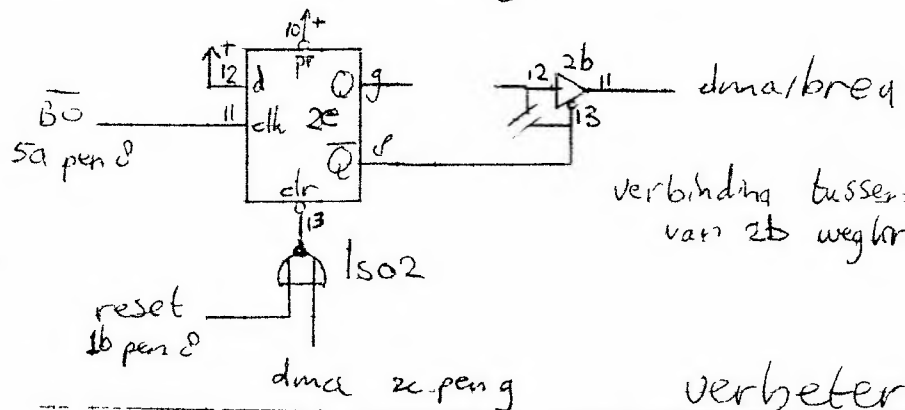
824

Het volgende circuit geeft een oplossing voor het te-lange dma/breq signaal:

De enable van de dma/breq buffer wordt geschakeld met de 1574 FlipFlop die over was

enable begint als de RS Flip 5a pen 8 Hoog wordt

de enable verdwijnt weer als dma 2c pen 9 Hoog wordt of reset 1b pen 8 Hoog wordt



voor transfer 1 sector
 $3 \times 512 = 1536$ clock cycles

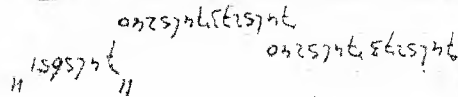
interleave $S = 5 \times 960 = 49$ ms
 $8 \times 960 = 768$ ms

		verbetering			
		oud	nieuw	volume	SWAPS
lezen hardisk	dead:	2048 = 58%	1536 = 41%	$\frac{512}{15680} = 3,2\%$	$\frac{512}{4544} = 11,2\%$
3200 cycles	cpu	1472 = 42%	1984 = 56%		
schrijven hardisk	dead:	3062 = 93,4%	1536 = 47%	$\frac{1526}{15680} = 9,7\%$	$\frac{1526}{9536} = 15,9\%$
3200 cycles	cpu	218 = 6,6%	1744 = 53%		

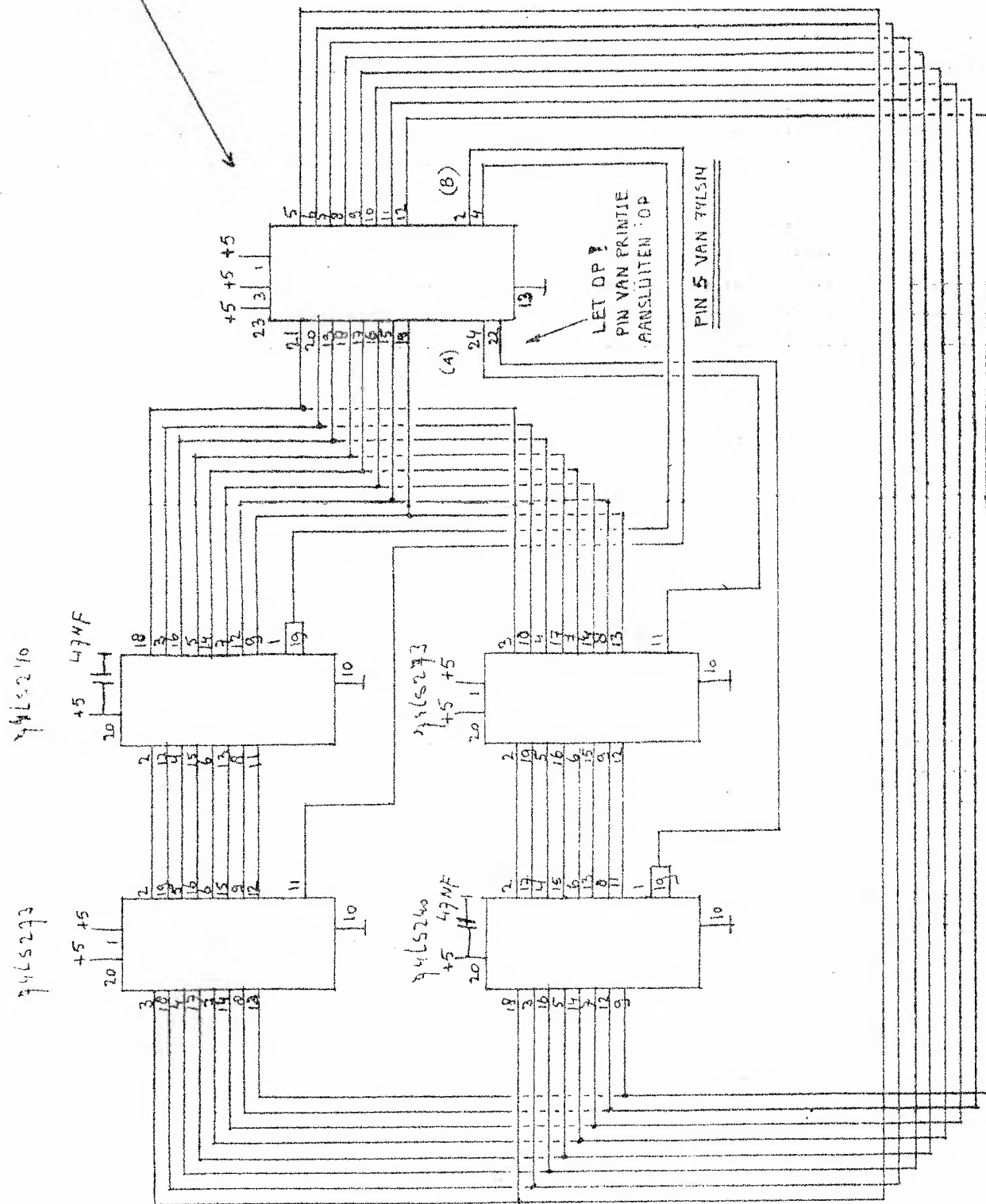
verbetering is evenredig met sectors / seconde

8 sectors 58.4%
 7680 cycles 49.1%
 15360 cycles 98.1%
 swap 204

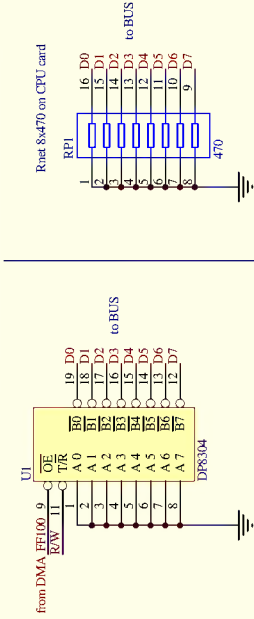
LETOPI
PINC
GESE



1-10-1984



UniFlex use empty databus to fill a 4K memory block with zero's.
SWTPC Sytem reads low
CS System reads high,, needs optional chip to read the zero's.
OR
Just load the databus with 470 ohm resistors.



Title		
Size	Number	Revision
B		
Date:	29-Oct-2020	Sheet of
File:	Z:\CS System\CS Computer data\RAM 811\RAM4058K.dib	6