COS1004 – Computer System

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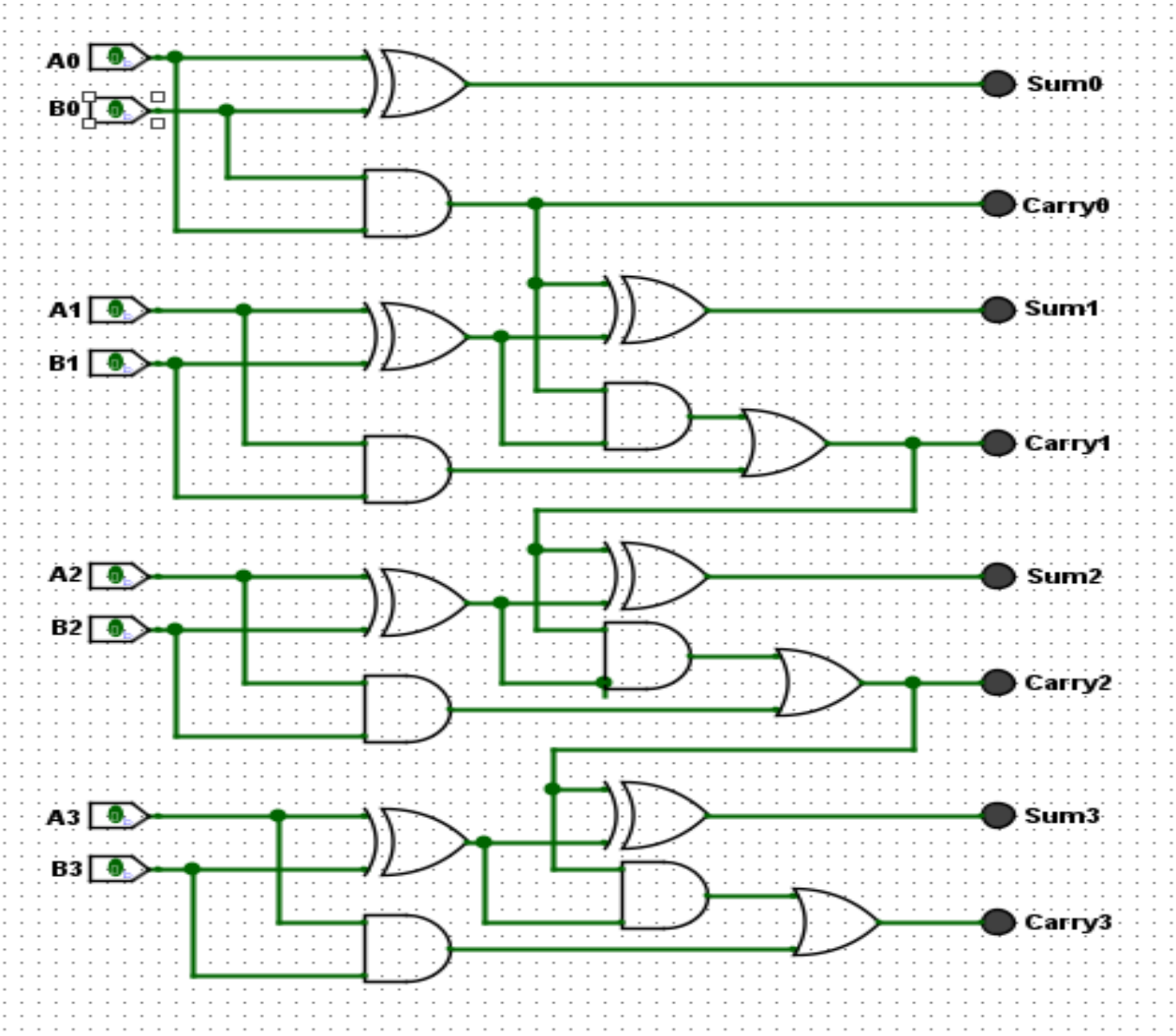
LAB 2

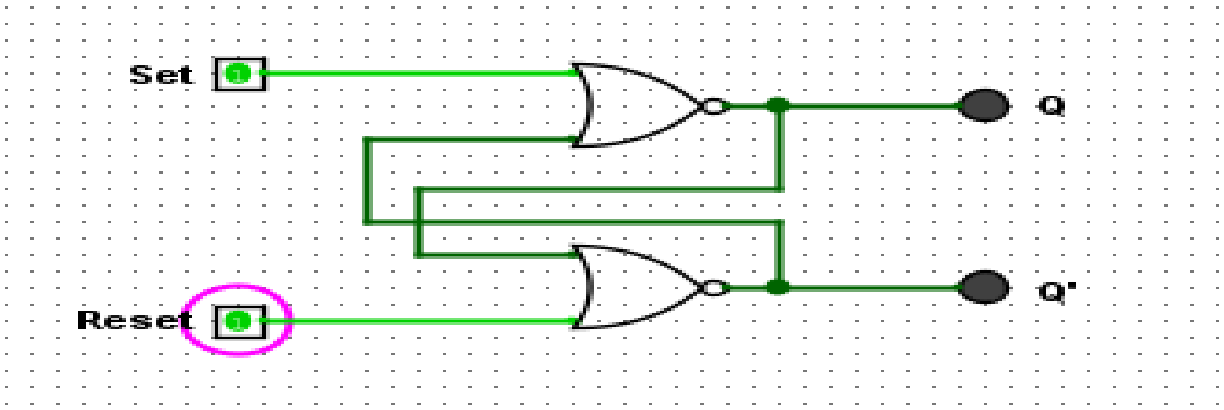
Part 1 – 4-bit adder



Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111

0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

Part 2 – Storing bits with Flip Flops



Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0

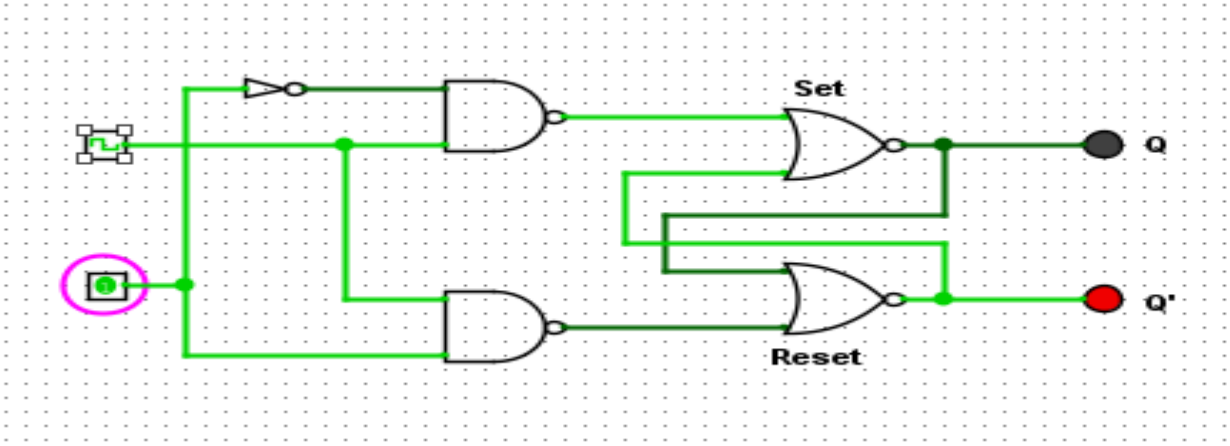
Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

When RS flip flop is made from cross coupled NOR gates. Then, taking Set momentarily 1 will set the Q and when taking Reset momentarily 1 will set the NotQ or Q’, which means it is resetting the Q.

What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design?

When both the SET and RESET inputs are 1, then the flip flop will be undefine state. This can be issue for digital circuit design as it violates the rule of flip flop that outputs should complement each other.

Part 3 – D Flip Flops



Clock	Pin	Q	Q’
0	0	0	0
0	1	0	0
1	1	0	1
1	0	1	0

Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

The D flip-flop has only one input, Q is updated to be the same as D when the clock goes active. The external D input (Data) internally generate both an R and as S input. D flip-flops are used in computer registers and memories and in counters and shift registers.

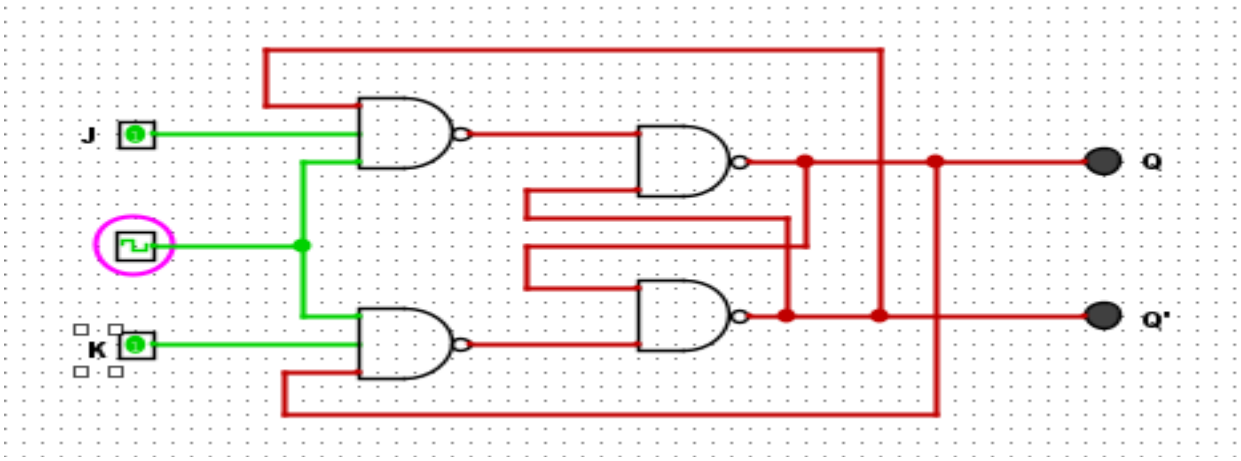
What is the role of the clock? How does it impact the changing of state of Q and Q’?

Clock is used to signal to control signal. When the clock signal is LOW, the input is not going to affect the output state. But, when clock signal is HIGH for the inputs to get active.

Why is it generally preferred over the R-S Flip Flop?

D Flip- Flop is preferred over the R-S flip flop because it help to synchronized data where everything needs to be clocked, and the D flip-flop has that advantage to do so. D flip-flop for serial-to-parallel conversion, making non-standard counters, frequency division, and without all the extra pins that needed to be conditioned in SR flip-flops.

Part 4 – J-K Flip Flops



J	K	Q (when clocked)	Q' (when clocked)
0	0	No change	
1	0	1	0
0	1	0	1
1	1	Toggle	

How can a J-K Flip Flop be made to behave like a D Flip Flop?

JK flip-flop can be converted into a D flip-flop by driving its J and K inputs pins with the D input and required additional hardware component would be a NOT gate.

How can a J-K Flip Flop be made to behave like a toggle (T Flip Flop)?

J-K Flip Flop be made to behave like a toggle when both J and K inputs is 1.