Samuel Coward

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Research Interests

Computer Arithmetic Electronic Design Automation Programming Languages Formal Verification

Education

04/21 – 02/25 **Ph.D. Imperial College London,** in Electrical and Electronic Engineering
Thesis Title: *Equality Saturation for Circuit Synthesis and Verification.*
Supervisors: *Prof. George A. Constantinides* and *Dr Theo Drane*.
Departmental Award for most promising doctoral work with 9 publications.
Industrial Impact with 7 patents filed based on PhD research.

10/18 – 08/19 **M.Phil. University of Cambridge, Distinction** in Scientific Computing.
Thesis Title: *GPU-Accelerated Interpolation for Initialising Transition State Searches*.

10/15 – 06/18 **BA. University of Cambridge, 1st-class** in Mathematics.
College Award for academic excellence and contributions to College.

Employment

12/25 – pres. **1851 Royal Commission Research Fellow** University College London
3-year fellowship hosted by UCL's Computer Science Department
Proposal Title: *Empowering Computer Chip Design through Formal Methods*

06/25 – 12/25 **Senior Research Fellow** with Prof. Alexandra Silva, University College London
Incorporated a 3 week Visiting Researcher post at Cornell University

04/25 – 06/25 **Post-Doc** with Prof. Tobias Grosser, University of Cambridge
Established myself in the open-source community and initiated new collaboration

04/21 – 04/25 **GPU Design Engineer** Numerical Hardware Group, Intel Corporation
Applied research and arithmetic circuit design for Intel GPUs, with 9 patents filed.
Supervised three interns - each leading to a conference publication (4, 10 and 11 below).

11/19 – 04/21 **Firmware Engineer** Alcatel IP Networks, Nokia
Developed C++ firmware and worked on bring-up of next generation silicon.

06/17 – 09/19 **Summer Internships** Cadence (2017), Riverlane Quantum (2018) and Intel (2019)

Awards and Achievements

2025 **1851 Royal Commission Research Fellowship**, 3-year fellowship (approx. £270k).

2024 **Stylianos Kalaitzis Award**, Imperial College EEE, for most promising doctoral work.

2022–2024 **Best Paper Candidates**, 1 × ASPLOS (4 below) and 2 × ARITH (6 & 13 below).

2022 **Division Recognition Award**, Intel Graphics, for innovation and network building.

2018 **Tallow Chandlers Award**, Selwyn College Cambridge, academic excellence.

Academic and Departmental Service

2024–pres. **Co-Founder & Steering Committee Member**. EGRAPHS Community.
Organise monthly seminar series and annual workshop.

2025–pres. **Athena Swan Committee Member**. UCL Computer Science.
Assist in action plan development and outreach activities.

Academic and Departmental Service (continued)

2023–2024 **Postgraduate Representative**. Imperial EEE CAS Group.
Reformed group meetings to foster collaboration and inclusive environment.
Collaborated with department management on office and social space renovation.

2024–pres. **Journal Reviewer**. IEEE TC, IEEE TCAD, ACM TACO.

2023–pres. **Program Committee Member**. ARITH Conference, LATTE & EGRAPHS Workshops.

Outreach

2021–pres. **Secondary School Project Supervision**. Five cohorts of students across Imperial College London Maths School and Folsom Preceptorship Program (California).

2023–pres. **STEM Ambassadors**. Supported school science week and school careers fairs.

2025–pres. **A-COMPS Program**. Mentoring A-level students from under-represented backgrounds.

Technical Skills

Coding	Verilog, Rust, C++, Linux, Git.
Tools	Logic synthesis (Design Compiler), formal verification (Jasper & VC Formal).
Technologies	Equality Saturation, SMT, Integer Linear Programming.

Research Publications and Patents

Journal Articles

1. **S. Coward**, T. Drane, and G. A. Constantinides, "Constraint-Aware E-Graph Rewriting for Hardware Performance Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, 2024. DOI: 10.1109/TCAD.2024.3483096.

2. **S. Coward**, T. Drane, and G. A. Constantinides, "ROVER: RTL Optimization via Verified E-Graph Rewriting," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, 2024. DOI: 10.1109/TCAD.2024.3410154.

3. **S. Coward**, L. Paulson, T. Drane, and E. Morini, "Formal verification of transcendental fixed- and floating-point algorithms using an automatic theorem prover," *ACM Formal Aspects of Computing (**FAC**)*, 2022. DOI: 10.1145/3543670.

Conference Proceedings

1. **[In Submission]** J. Merckx, S. Lokuphine, **S. Coward**, J. Cheng, B. Sutter, and T. Grosser, "E-graphs as a persistent compiler abstraction," in *47th ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**)*, 2026.

2. **[In Submission] S. Coward**, H. Ueno, B. Healey, and T. Grosser, "An IR for composing and verifying datapath optimizations," in *63rd ACM/IEEE Design Automation Conference (**DAC**)*, 2026.

3. O. Cassidy, M. Andronic, **S. Coward**, and G. A. Constantinides, "ReducedLUT: Table decomposition with "don't care" conditions," in *33rd ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Feb. 2025. DOI: 10.1145/3706628.3708823.

4. J. Cheng, **S. Coward**, L. Chelini, R. Barbalho, and T. Drane, "SEER: Super-Optimization Explorer for HLS using E-graph Rewriting with MLIR," in *29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, : **Best Paper Candidate**, Apr. 2024. DOI: 10.1145/3620665.3640392.

5. T. Drane, **S. Coward**, M. Temel, and J. Leslie-Hurd, "On the systematic creation of faithfully rounded commutative truncated booth multipliers," in *31st IEEE Symposium on Computer Arithmetic (**ARITH**)*, Jun. 2024. DOI: 10.1109/ARITH61463.2024.00027.

6. **S. Coward**, T. Drane, E. Morini, and G. Constantinides, "Combining power and arithmetic optimization via datapath rewriting," in *31st IEEE Symposium on Computer Arithmetic (**ARITH**)*, 🏆: **Best Paper Candidate**, Jun. 2024. DOI: 10.1109/ARITH61463.2024.00014.

7. B. Orloski, **S. Coward**, and T. Drane, "Automatic generation of complete polynomial interpolation design space for hardware architectures," in *28th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, Jan. 2023. DOI: 10.1145/3566097.3567840.

8. **S. Coward**, G. A. Constantinides, and T. Drane, "Automating constraint-aware datapath optimization using e-graphs," in *60th ACM/IEEE Design Automation Conference (**DAC**)*, Jun. 2023. DOI: 10.1109/DAC56929.2023.10247797.

9. **S. Coward**, G. A. Constantinides, and T. Drane, "Combining e-graphs with abstract interpretation," in *12th ACM SIGPLAN International Workshop on the State Of the Art in Program Analysis (**SOAP**)*, Jun. 2023. DOI: 10.1145/3589250.3596144.

10. **S. Coward**, E. Morini, B. Tan, T. Drane, and G. Constantinides, "Datapath verification via word-level e-graph rewriting," in *Formal Methods in Computer-Aided Design (**FMCAD**)*, Oct. 2023. DOI: 10.34727/2023/isbn.978-3-85448-060-0_17.

11. A. Wanna, **S. Coward**, T. Drane, G. A. Constantinides, and M. D. Ercegovac, "Multiplier optimization via e-graph rewriting," in *57th IEEE Asilomar Conference on Signals, Systems, and Computers*, Dec. 2023. DOI: 10.1109/IEEECONF59524.2023.10476812.

12. O. Flatt, **S. Coward**, M. Willsey, Z. Tatlock, and P. Panchekha, "Small Proofs from Congruence Closure," in *Formal Methods in Computer-Aided Design (**FMCAD**)*, Oct. 2022. DOI: 10.34727/2022/isbn.978-3-85448-053-2-13.

13. **S. Coward**, G. A. Constantinides, and T. Drane, "Automatic datapath optimization using e-graphs," in *29th IEEE Symposium on Computer Arithmetic (**ARITH**)*, 🏆: **Best Paper Candidate**, Sep. 2022. DOI: 10.1109/ARITH54963.2022.00016.

14. **S. Coward**, T. Drane, and Y. Harel, "Automatic design space exploration for an error tolerant application," in *27th IEEE Symposium on Computer Arithmetic (**ARITH**)*, Jun. 2020. DOI: 10.1109/ARITH48897.2020.00025.

Patents

1. E. Morini, **S. Coward**, T. Drane, G. A. Constantinides, and J. Schmerge, *Automatic bug fixing of rtl via word level rewriting and formal verification*, US Patent App. 18/505,397, Jan. 2025.

2. **S. Coward**, T. Drane, E. Morini, W. Zorn, and A. Bhinge, *Summarizing stimulus space via clustering and stochastic processes*, US Patent App. 18/606,542, Sep. 2025.

3. J. Cheng, **S. Coward**, L. Chelini, R. Barbalho, and T. Drane, *Program analysis, design space exploration and verification for high-level synthesis via e-graph rewriting*, US Patent App. 18/396,321, Apr. 2024.

4. J. Cheng, **S. Coward**, L. Chelini, R. Barbalho, and T. Drane, *Super-optimization explorer using e-graph rewriting for high-level synthesis*, US Patent App. 18/396,335, Apr. 2024.

5. T. Drane, E. Morini, J. Schmerge, and **S. Coward**, *Automatic code generation of optimized RTL via redundant code removal*, US Patent App. 18/512,518, Mar. 2024.

6. **S. Coward**, T. Drane, and G. Constantinides, *Apparatus, device, method and computer program for generating an RTL representation of a circuit*, US Patent App. 18/391,716, May 2024.

7 **S. Coward**, T. Drane, and G. A. Constantinides, *Automated detection of case-splitting opportunities in RTL*, US Patent App. 18/395,066, Apr. 2024.

8 **S. Coward**, T. Drane, and G. A. Constantinides, *Hardware power optimization via e-graph based automatic RTL exploration*, US Patent App. 18/538,104, Apr. 2024.

9 **S. Coward**, T. Drane, G. A. Constantinides, and E. Morini, *Constructing hierarchical clock gating architectures via rewriting*, US Patent App. 18/538,116, Apr. 2024.

10 **S. Coward**, T. Drane, and G. Constantinides, *Apparatus, device, method, and computer program for generating a register transfer level representation of a circuit*, US Patent App. 17/649,937, Nov. 2022.

11 **S. Coward**, M. Langenbuch, and J. H. Lee, *Apparatus, device, method and computer program for an integrated development environment*, US Patent App. 17/644,112, Nov. 2022.