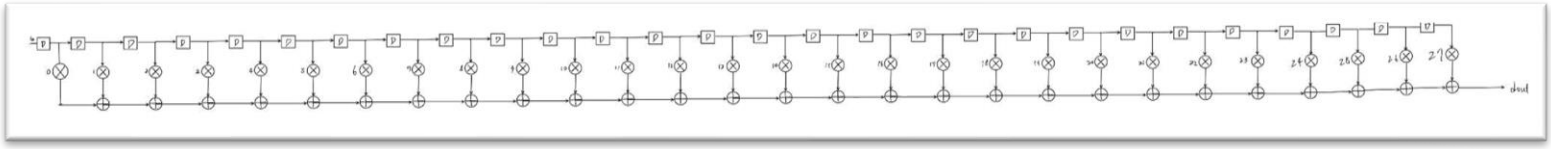
HW4 的基本設計

(速度 clock speed、資料運算吞吐量 throughput，面積/邏輯閘數/FPGA 成本，耗能)

下圖為 Direct Form FIR 架構



```
`timescale 1ns/10ps
`define CYCLE 6.0
```

1. 速度 clock speed:6.0
2. 資料運算吞吐量 throughput:2.6 G bits/sec
3. 面積

area.log

```
****************************************
Report : area
Design : FIR
Version: R-2020.09-SP5
Date   : Wed Jan  4 03:49:23 2023
****************************************

Library(s) Used:

    slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                         4201
Number of nets:                         20627
Number of cells:                        15931
Number of combinational cells:          14429
Number of sequential cells:              1350
Number of macros/black boxes:               0
Number of buf/inv:                       3544
Number of references:                      75

Combinational area:             172353.995716
Buf/Inv area:                    19128.000422
Noncombinational area:           53788.907932
Macro/Black Box area:                0.000000
Net Interconnect area:         1556294.586029

Total cell area:                226142.903648
Total area:                    1782437.489677
```

area.log

```
--------------------------------

                                 Global cell area              Local cell area
                                 ------------------  ------------------------------------
Hierarchical cell                Absolute     Percent  Combi-      Noncombi-   Black-
                                 Total        Total    national    national    boxes   Design
-------------------------------- -----------  -------  ----------  ----------  ------  ----------------
FIR                              226142.9836    100.0    1420.7230  53788.9079  0.0000  FIR
add_0_root_add_0_root_add_150_27   3471.1830      1.5    3471.1830     0.0000  0.0000  FIR_DW01_add_27
add_10_root_add_0_root_add_150_27  4435.3062      2.0    4435.3062     0.0000  0.0000  FIR_DW01_add_39
add_11_root_add_0_root_add_150_27  4431.9114      2.0    4431.9114     0.0000  0.0000  FIR_DW01_add_29
add_12_root_add_0_root_add_150_27  4654.2708      2.1    4654.2708     0.0000  0.0000  FIR_DW01_add_33
add_13_root_add_0_root_add_150_27  3771.6228      1.7    3771.6228     0.0000  0.0000  FIR_DW01_add_45
add_14_root_add_0_root_add_150_27  2763.3672      1.2    2763.3672     0.0000  0.0000  FIR_DW01_add_55
add_15_root_add_0_root_add_150_27  2780.3412      1.2    2780.3412     0.0000  0.0000  FIR_DW01_add_54
add_16_root_add_0_root_add_150_27  3707.1216      1.6    3707.1216     0.0000  0.0000  FIR_DW01_add_37
add_17_root_add_0_root_add_150_27  3819.1500      1.7    3819.1500     0.0000  0.0000  FIR_DW01_add_50
add_18_root_add_0_root_add_150_27  3739.3722      1.7    3739.3722     0.0000  0.0000  FIR_DW01_add_42
add_19_root_add_0_root_add_150_27  3951.5472      1.7    3951.5472     0.0000  0.0000  FIR_DW01_add_38
add_1_root_add_0_root_add_150_27   5053.1598      2.2    5053.1598     0.0000  0.0000  FIR_DW01_add_31
add_20_root_add_0_root_add_150_27  4148.4456      1.8    4148.4456     0.0000  0.0000  FIR_DW01_add_35
add_21_root_add_0_root_add_150_27  3848.0058      1.7    3848.0058     0.0000  0.0000  FIR_DW01_add_48
add_22_root_add_0_root_add_150_27  3725.7930      1.6    3725.7930     0.0000  0.0000  FIR_DW01_add_44
add_23_root_add_0_root_add_150_27  3793.6890      1.7    3793.6890     0.0000  0.0000  FIR_DW01_add_49
add_24_root_add_0_root_add_150_27  4175.6040      1.8    4175.6040     0.0000  0.0000  FIR_DW01_add_28
add_25_root_add_0_root_add_150_27  3659.5944      1.6    3659.5944     0.0000  0.0000  FIR_DW01_add_32
add_26_root_add_0_root_add_150_27  3730.2942      1.7    3730.2942     0.0000  0.0000  FIR_DW01_add_46
add_2_root_add_0_root_add_150_27   4603.3488      2.0    4603.3488     0.0000  0.0000  FIR_DW01_add_41
add_3_root_add_0_root_add_150_27   4671.2448      2.1    4671.2448     0.0000  0.0000  FIR_DW01_add_40
add_4_root_add_0_root_add_150_27   4691.6136      2.1    4691.6136     0.0000  0.0000  FIR_DW01_add_30
add_5_root_add_0_root_add_150_27   4810.4316      2.1    4810.4316     0.0000  0.0000  FIR_DW01_add_34
add_6_root_add_0_root_add_150_27   4372.5024      1.9    4372.5024     0.0000  0.0000  FIR_DW01_add_43
add_7_root_add_0_root_add_150_27   3240.3366      1.4    3240.3366     0.0000  0.0000  FIR_DW01_add_56
add_8_root_add_0_root_add_150_27   4457.3724      2.0    4457.3724     0.0000  0.0000  FIR_DW01_add_36
add_9_root_add_0_root_add_150_27   4251.9870      1.9    4251.9870     0.0000  0.0000  FIR_DW01_add_47
mult_113                           1497.1068      0.7    1497.1068     0.0000  0.0000  FIR_DW_mult_tc_48
mult_114                           1183.8774      0.5    1183.8774     0.0000  0.0000  FIR_DW_mult_tc_57
mult_115                           2210.8148      1.0    2210.8148     0.0000  0.0000  FIR_DW_mult_tc_59
mult_116                           1946.9178      0.9    1946.9178     0.0000  0.0000  FIR_DW_mult_tc_50
mult_117                           1308.6954      0.6    1308.6954     0.0000  0.0000  FIR_DW_mult_tc_52
mult_118                           3292.9561      1.5    3292.9561     0.0000  0.0000  FIR_DW_mult_tc_32
mult_119                           2065.7358      0.9    2065.7358     0.0000  0.0000  FIR_DW_mult_tc_42
mult_120                           2062.3410      0.9    2062.3410     0.0000  0.0000  FIR_DW_mult_tc_36
mult_121                           2496.8754      1.1    2496.8754     0.0000  0.0000  FIR_DW_mult_tc_40
mult_122                           2495.1780      1.1    2495.1780     0.0000  0.0000  FIR_DW_mult_tc_44
mult_123                           3862.1096      1.4    3862.1096     0.0000  0.0000  FIR_DW_mult_tc_28
mult_124                           2564.7714      1.1    2564.7714     0.0000  0.0000  FIR_DW_mult_tc_34
mult_125                           2498.5728      1.1    2498.5728     0.0000  0.0000  FIR_DW_mult_tc_30
mult_126                           2298.2796      1.0    2298.2796     0.0000  0.0000  FIR_DW_mult_tc_61
mult_127                           2274.5160      1.0    2274.5160     0.0000  0.0000  FIR_DW_mult_tc_60
mult_128                           2474.8092      1.1    2474.8092     0.0000  0.0000  FIR_DW_mult_tc_31
mult_129                           2554.5870      1.1    2554.5870     0.0000  0.0000  FIR_DW_mult_tc_35
mult_130                           3060.4122      1.4    3060.4122     0.0000  0.0000  FIR_DW_mult_tc_29
mult_131                           2490.0858      1.1    2490.0858     0.0000  0.0000  FIR_DW_mult_tc_45
mult_132                           2503.6650      1.1    2503.6650     0.0000  0.0000  FIR_DW_mult_tc_41
mult_133                           2083.4994      0.9    2083.4994     0.0000  0.0000  FIR_DW_mult_tc_37
mult_134                           2084.4072      0.9    2084.4072     0.0000  0.0000  FIR_DW_mult_tc_43
mult_135                           3466.0909      1.5    3466.0909     0.0000  0.0000  FIR_DW_mult_tc_33
mult_136                           1295.1162      0.6    1295.1162     0.0000  0.0000  FIR_DW_mult_tc_53
mult_137                           1943.5230      0.9    1943.5230     0.0000  0.0000  FIR_DW_mult_tc_51
mult_138                           2220.1992      1.0    2220.1992     0.0000  0.0000  FIR_DW_mult_tc_58
mult_139                           1183.0878      0.5    1183.0878     0.0000  0.0000  FIR_DW_mult_tc_56
mult_140                           1485.2250      0.7    1485.2250     0.0000  0.0000  FIR_DW_mult_tc_49
-------------------------------- -----------  -------  ----------  ----------  ------  ----------------
Total                                                  172353.9957  53788.9079  0.0000
```

4. 耗能

power.log

```
Loading db file '/home/m111/m111064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db'
Information: Propagating switching activity (high effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort high
        -verbose
Design : FIR
Version: R-2020.09-SP5
Date   : Wed Jan  4 03:49:28 2023
****************************************


Library(s) Used:

    slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
FIR                   tsmc13_wl10       slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.4328 mW   (71%)
  Net Switching Power  =   3.8478 mW   (29%)
                         ---------
Total Dynamic Power    =  13.2806 mW  (100%)

Cell Leakage Power     = 195.8756 uW

                 Internal         Switching           Leakage            Total                          Cell
Power Group      Power            Power               Power              Power   (   %    ) Attrs   Count
-----------------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)             0
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)             0
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)             0
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)             0
register           7.7387           0.3109          4.9670e+07            8.0993  (  60.10%)          1350
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)             0
combinational      1.6941           3.5369          1.4621e+08            5.3772  (  39.90%)         14429
-----------------------------------------------------------------------------------------------------------
Total              9.4328 mW        3.8478 mW       1.9588e+08 pW        13.4765 mW
1
```

5. timing report:

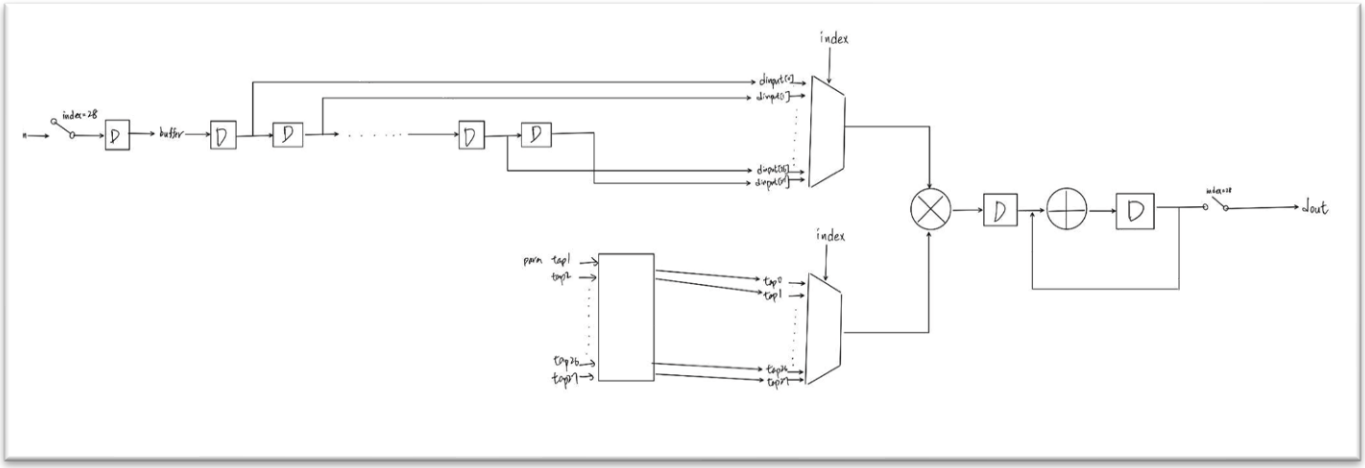
power.log timing.log

```
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : FIR
Version: R-2020.09-SP5
Date   : Wed Jan  4 03:49:23 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: account_reg[5][8]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: d_output_reg[31]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR                tsmc13_wl10           slow

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.50       0.50
  account_reg[5][8]/CK (DFFRX4)                            0.00 #     0.50 r
  account_reg[5][8]/Q (DFFRX4)                             0.42       0.92 r
  add_17_root_add_0_root_add_150_27/A[8] (FIR_DW01_add_50)
                                                           0.00       0.92 r
  add_17_root_add_0_root_add_150_27/U487/Y (NAND2X8)       0.13       1.05 f
  add_17_root_add_0_root_add_150_27/U486/Y (OAI21X4)       0.21       1.25 r
  add_17_root_add_0_root_add_150_27/U249/Y (AOI21X4)       0.13       1.38 f
  add_17_root_add_0_root_add_150_27/U197/Y (OAI21X4)       0.14       1.53 r
  add_17_root_add_0_root_add_150_27/U195/Y (AOI21X4)       0.11       1.64 f
  add_17_root_add_0_root_add_150_27/U375/Y (CLKBUFX4)      0.38       2.02 f
  add_17_root_add_0_root_add_150_27/U519/Y (OAI21X2)       0.28       2.30 r
  add_17_root_add_0_root_add_150_27/U461/Y (XOR2X4)        0.24       2.54 r
  add_17_root_add_0_root_add_150_27/SUM[24] (FIR_DW01_add_50)
                                                           0.00       2.54 r
  add_9_root_add_0_root_add_150_27/B[24] (FIR_DW01_add_47)
                                                           0.00       2.54 r
  add_9_root_add_0_root_add_150_27/U403/Y (NOR2X8)         0.15       2.68 f
  add_9_root_add_0_root_add_150_27/U477/Y (NOR2X6)         0.13       2.82 r
  add_9_root_add_0_root_add_150_27/U434/Y (INVX3)          0.12       2.93 f
  add_9_root_add_0_root_add_150_27/U405/Y (INVX3)          0.13       3.07 r
  add_9_root_add_0_root_add_150_27/U484/Y (NAND2X2)        0.12       3.19 f
  add_9_root_add_0_root_add_150_27/U77/Y (OAI21X4)         0.16       3.34 r
  add_9_root_add_0_root_add_150_27/U64/Y (XNOR2X4)         0.20       3.54 r
  add_9_root_add_0_root_add_150_27/SUM[26] (FIR_DW01_add_47)
                                                           0.00       3.54 r
  add_3_root_add_0_root_add_150_27/B[26] (FIR_DW01_add_40)
                                                           0.00       3.54 r
  add_3_root_add_0_root_add_150_27/U511/Y (NAND2X4)        0.19       3.73 f
  add_3_root_add_0_root_add_150_27/U531/Y (OAI21X4)        0.17       3.90 r
  add_3_root_add_0_root_add_150_27/U57/Y (AOI21X4)         0.11       4.01 f
  add_3_root_add_0_root_add_150_27/U483/Y (OAI21X2)        0.22       4.23 r
  add_3_root_add_0_root_add_150_27/U536/Y (AOI21X4)        0.11       4.34 f
  add_3_root_add_0_root_add_150_27/U545/Y (OAI21X4)        0.09       4.43 r
  add_3_root_add_0_root_add_150_27/U442/Y (XNOR2X4)        0.19       4.62 r
  add_3_root_add_0_root_add_150_27/SUM[29] (FIR_DW01_add_40)
                                                           0.00       4.62 r
```

```
  add_2_root_add_0_root_add_150_27/B[29] (FIR_DW01_add_41)
                                                           0.00       4.62 r
  add_2_root_add_0_root_add_150_27/U482/Y (NOR2X8)         0.14       4.76 f
  add_2_root_add_0_root_add_150_27/U536/Y (NOR2X8)         0.12       4.88 r
  add_2_root_add_0_root_add_150_27/U535/Y (INVX8)          0.08       4.96 f
  add_2_root_add_0_root_add_150_27/U547/Y (NOR2X8)         0.11       5.08 r
  add_2_root_add_0_root_add_150_27/U374/Y (NAND2X4)        0.09       5.16 f
  add_2_root_add_0_root_add_150_27/U490/Y (OAI21X4)        0.14       5.31 r
  add_2_root_add_0_root_add_150_27/U456/Y (XOR2X4)         0.16       5.47 f
  add_2_root_add_0_root_add_150_27/SUM[30] (FIR_DW01_add_41)
                                                           0.00       5.47 f
  add_0_root_add_0_root_add_150_27/A[30] (FIR_DW01_add_27)
                                                           0.00       5.47 f
  add_0_root_add_0_root_add_150_27/U561/Y (OR2X8)          0.19       5.66 f
  add_0_root_add_0_root_add_150_27/U446/Y (AOI21X4)        0.15       5.81 r
  add_0_root_add_0_root_add_150_27/U445/Y (OAI21X4)        0.10       5.91 f
  add_0_root_add_0_root_add_150_27/U444/Y (AOI21X4)        0.12       6.04 r
  add_0_root_add_0_root_add_150_27/U443/Y (OAI2BB1X4)      0.09       6.13 f
  add_0_root_add_0_root_add_150_27/U439/Y (XNOR2X4)        0.11       6.24 r
  add_0_root_add_0_root_add_150_27/SUM[31] (FIR_DW01_add_27)
                                                           0.00       6.24 r
  d_output_reg[31]/D (DFFRHQX8)                            0.00       6.24 r
  data arrival time                                                   6.24

  clock clk (rise edge)                                    6.00       6.00
  clock network delay (ideal)                              0.50       6.50
  clock uncertainty                                       -0.10       6.40
  d_output_reg[31]/CK (DFFRHQX8)                           0.00       6.40 r
  library setup time                                      -0.16       6.24
  data required time                                                  6.24
  -----------------------------------------------------------------------------
  data required time                                                  6.24
  data arrival time                                                  -6.24
  -----------------------------------------------------------------------------
  slack (MET)                                                         0.00
```

Final-Project-Report

下圖為 Folding FIR 架構圖:



*製成採用的是 tsmc13_neg.v

(1)預期規格:

>面積:由前面所列作業四的合成 report 可以看到 cell area 面積很大，一共 22 萬，造成面積這麼大的原因是因為一共有 28 個乘法器和加法器，所以我主要是用 Folding 來減少面積，將原本 28 個乘法器和加法器，進行 Folding 後，只需要 1 個乘法器和加法器，我預期可以減少 2 倍以上的面積。

>速度:Clock speed 是 6ns，critical path 是由一個乘法器和一個加法器所組成的，我採用 pipeline 來切開一個乘法器和一個加法器，將 critical path 切成只剩下乘法器，所以我預期可以減少 1ns 的 clock speed

2. Fixed Point 模擬

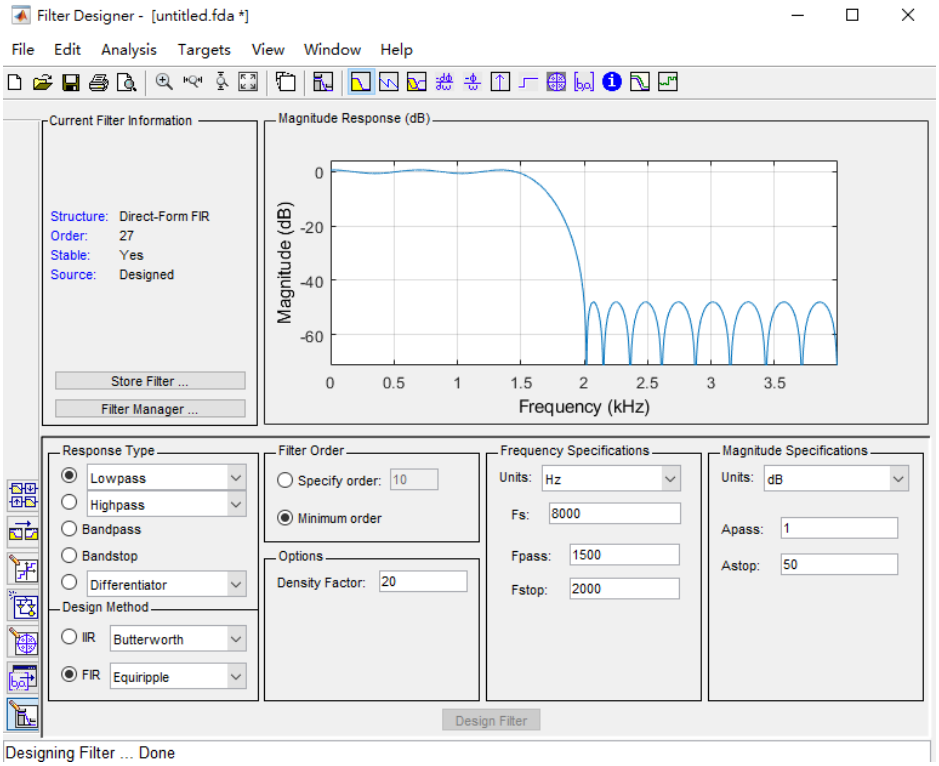
(a)

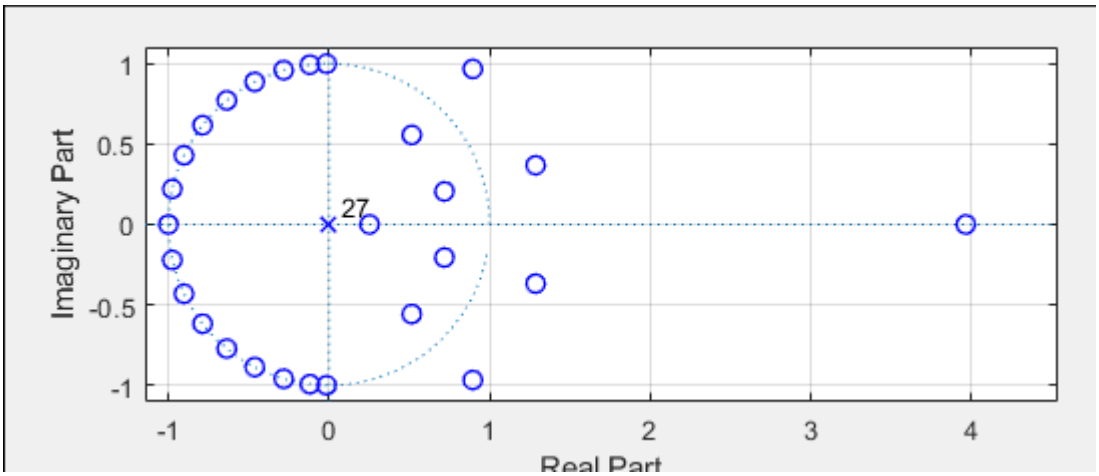
(i)floating coef:

-0.00296489474904223539175607271545231924 4
0.00501586115236337184986048498558375285 9
0.02066789310173582777663270348966761957 9
0.02514888811261038747968399320598109625 3
0.00231686527577968683078157852150980033 9
-0.02577962493350009764991881411333451978 9
-0.01594651813121744296508630611697299173 1

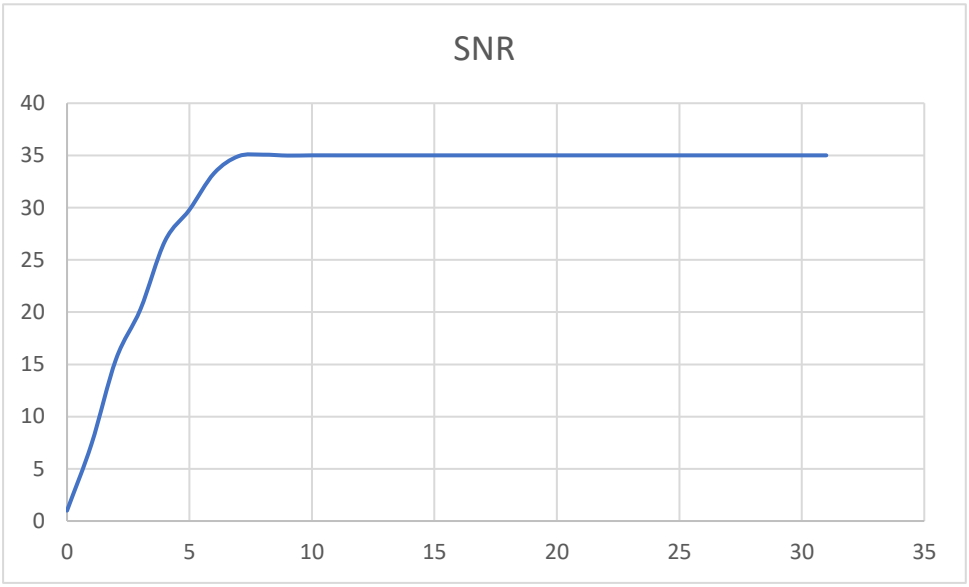
0.029216940020626670782011302662795060314
0.042349361155728501571182675888849189505
-0.020197194227754448891953842348812031 56
-0.085611751306674921391248744839685969055
-0.021255965443284792482092626642042887397
0.191877715214637978302647525197244249284
0.391355121984242604327164372080005705357
0.391355121984242604327164372080005705357
0.191877715214637978302647525197244249284
-0.021255965443284792482092626642042887397
-0.085611751306674921391248744839685969055
-0.020197194227754448891953842348812031 56
0.042349361155728501571182675888849189505
0.029216940020626670782011302662795060314
-0.015946518131217442965086306116972991731
-0.025779624933500097649918814113334519789
0.002316865275779686830781578521509800339
0.025148888112610387479683993205981096253
0.020667893101735827776632703489667619579
0.005015861152363371849860484985583752859
-0.002964894749042235391756072715452319244

(ii)





(b)

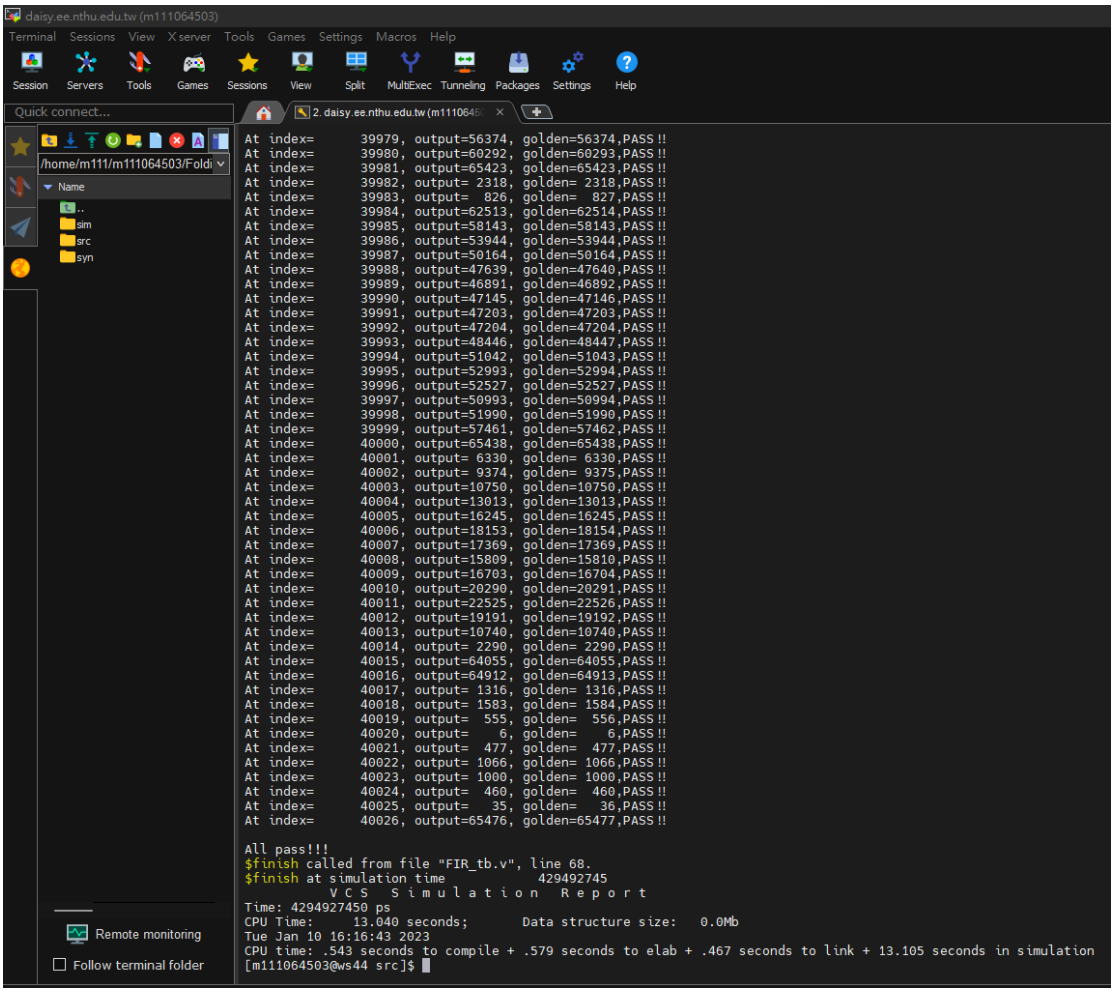


可以看到在精度為 8 左右就開始收斂了

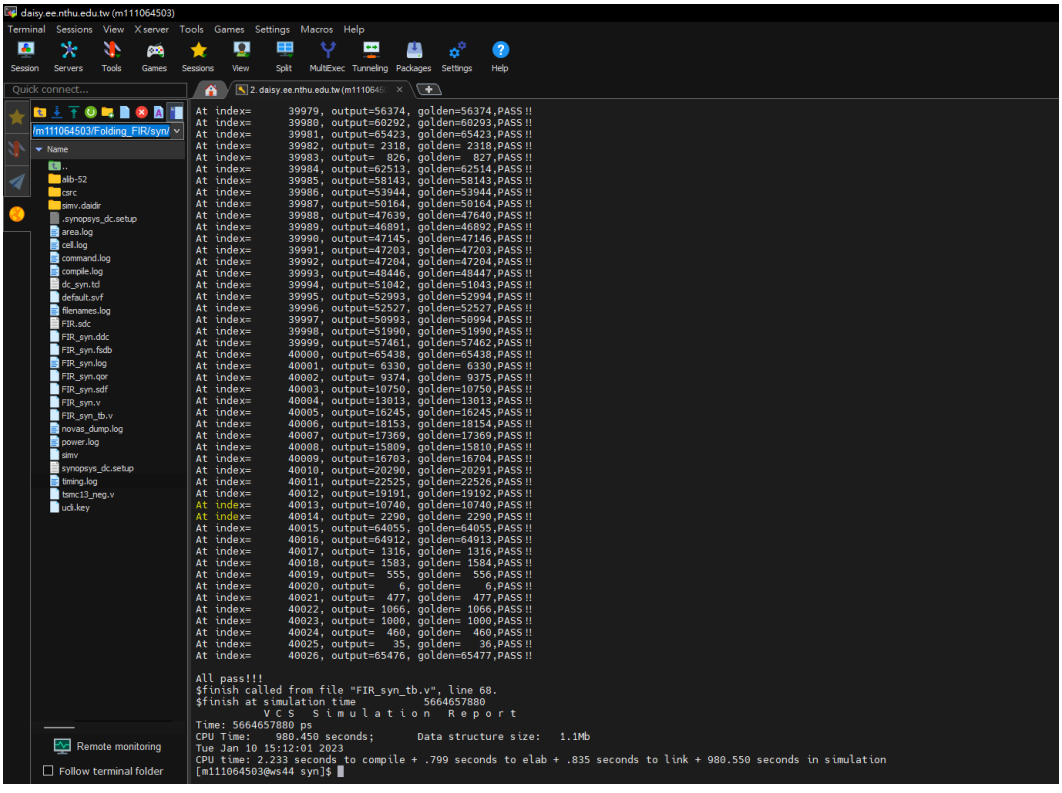
我採用精度為 15

➔ SNR loss=0 dB

(3)presim:



(4)gate level simulation:



(5) synthesis Report

1. area report:

從原本 cell area22 萬降到 7 萬，少了 3 倍，達到預期規格面積少 2 倍以上。

area.log

```
****************************************
Report : area
Design : FIR
Version: R-2020.09-SP5
Date   : Tue Jan 10 15:02:48 2023
****************************************

Library(s) Used:

    slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           35
Number of nets:                          4747
Number of cells:                         4287
Number of combinational cells:           3717
Number of sequential cells:               570
Number of macros/black boxes:               0
Number of buf/inv:                        747
Number of references:                     137

Combinational area:              51449.891363
Buf/Inv area:                     7762.210212
Noncombinational area:           18608.595634
Macro/Black Box area:                0.000000
Net Interconnect area:          448188.984436

Total cell area:                 70058.486998
Total area:                     518247.471434

Hierarchical area distribution
------------------------------

                                  Global cell area           Local cell area
                                  -----------------  -------------------------------
Hierarchical cell                 Absolute    Percent  Combi-      Noncombi-   Black-
                                  Total       Total    national    national    boxes    Design
-------------------------------- ----------  -------  ----------  ----------  ------  ---------
FIR                               70058.4870    100.0  51449.8914  18608.5956  0.0000  FIR
-------------------------------- ----------  -------  ----------  ----------  ------  ---------
Total                                                  51449.8914  18608.5956  0.0000

1
```

2. timing report:

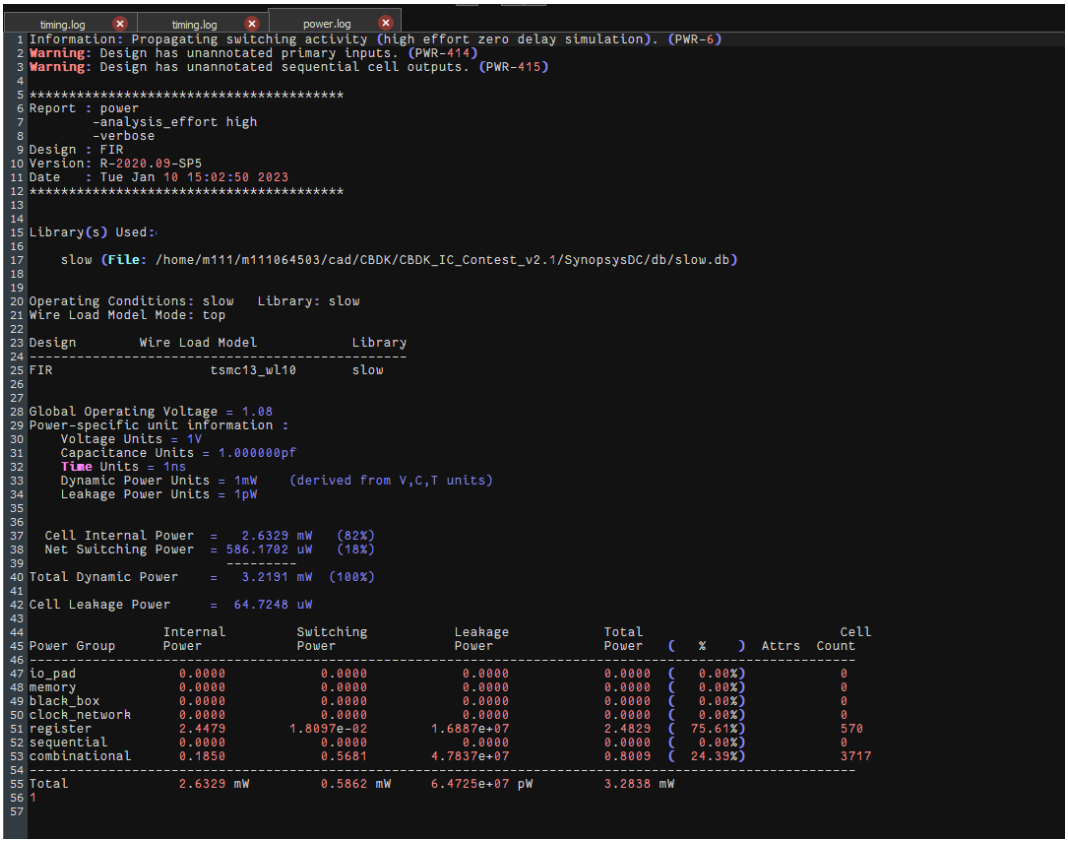
```
`timescale 1ns/10ps
`define CYCLE 4.88
```

從 timing report 看出 critical path 只剩下乘法器，所以有成功在乘法和加法器之間切 pipeline，6-4.88=1.12ns，也有達成預期規格少 1ns 的要求。

timing.log

```
Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: index_reg[4]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: D_in_reg[11]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR                tsmc13_wl10           slow

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.50       0.50
  index_reg[4]/CK (DFFRX4)                 0.00       0.50 r
  index_reg[4]/Q (DFFRX4)                  0.54       1.04 f
  U4686/Y (NOR2X8)                         0.16       1.20 r
  U5302/Y (NAND2X8)                        0.14       1.35 f
  U3975/Y (INVX12)                         0.09       1.43 r
  U4123/Y (NAND2X8)                        0.09       1.53 f
  U4122/Y (INVX20)                         0.15       1.68 r
  U4096/Y (NAND2X6)                        0.09       1.77 f
  U4842/Y (NAND4X6)                        0.14       1.90 r
  U4231/Y (NOR3X8)                         0.10       2.00 f
  U4055/Y (NAND3X8)                        0.11       2.11 r
  U4177/Y (XOR2X4)                         0.24       2.35 r
  U4167/Y (AND2X8)                         0.23       2.58 r
  U4165/Y (INVX12)                         0.08       2.66 f
  U4201/Y (BUFX20)                         0.12       2.78 f
  U3251/Y (INVX12)                         0.06       2.84 r
  U5433/Y (NAND2X4)                        0.07       2.91 f
  U3165/Y (NAND3X4)                        0.13       3.04 r
  U5098/Y (NOR2X8)                         0.09       3.13 f
  U4205/Y (INVX4)                          0.08       3.21 r
  U5182/Y (NAND2X6)                        0.07       3.28 f
  U3056/Y (NAND2X6)                        0.08       3.36 r
  U5179/Y (XOR2X4)                         0.13       3.49 r
  U5138/Y (XNOR2X4)                        0.24       3.73 r
  U5137/Y (INVX12)                         0.10       3.83 f
  U2913/Y (BUFX6)                          0.14       3.97 f
  U5873/CO (ACHCINX4)                      0.35       4.32 f
  U5874/Y (NAND2X2)                        0.26       4.58 r
  U5875/Y (NAND2X2)                        0.13       4.71 f
  U5877/Y (NAND3X2)                        0.14       4.86 r
  U5878/Y (XNOR2X4)                        0.16       5.02 f
  U2833/Y (NOR2X4)                         0.10       5.12 r
  D_in_reg[11]/D (DFFRX2)                  0.00       5.12 r
  data arrival time                                   5.12

  clock clk (rise edge)                    4.88       4.88
  clock network delay (ideal)              0.50       5.38
  clock uncertainty                       -0.10       5.28
  D_in_reg[11]/CK (DFFRX2)                 0.00       5.28 r
  library setup time                      -0.16       5.12
  data required time                                  5.12
  -----------------------------------------------------------
  data required time                                  5.12
  data arrival time                                  -5.12
  -----------------------------------------------------------
  slack (MET)                                        0.00

```

3. power report:



```
timing.log   timing.log   power.log
Information: Propagating switching activity (high effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort high
        -verbose
Design : FIR
Version: R-2020.09-SP5
Date   : Tue Jan 10 15:02:50 2023
****************************************


Library(s) Used:

    slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
FIR                   tsmc13_wl10       slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.6329 mW   (82%)
  Net Switching Power  = 586.1702 uW   (18%)
                         ---------
Total Dynamic Power    =   3.2191 mW  (100%)

Cell Leakage Power     =  64.7248 uW

                 Internal         Switching           Leakage            Total                          Cell
Power Group      Power            Power               Power              Power   (   %    )  Attrs     Count
--------------------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000              0.0000             0.0000  (   0.00%)                0
memory           0.0000           0.0000              0.0000             0.0000  (   0.00%)                0
black_box        0.0000           0.0000              0.0000             0.0000  (   0.00%)                0
clock_network    0.0000           0.0000              0.0000             0.0000  (   0.00%)                0
register         2.4479           1.8097e-02          1.6887e+07         2.4829  (  75.61%)              570
sequential       0.0000           0.0000              0.0000             0.0000  (   0.00%)                0
combinational    0.1850           0.5681              4.7837e+07         0.8009  (  24.39%)             3717
--------------------------------------------------------------------------------------------------------------
Total            2.6329 mW        0.5862 mW           6.4725e+07 pW      3.2838 mW
1
```

4. Throughput=117M bits/sec

(6) 設計前與設計後比較

設計	Direct Form FIR(前)	Folding FIR(後)
Clock speed	6.0	4.88
Hardware cost (cell area)	226242	70058
Throughput	2.6 G bits/sec	117M bits/sec
power	13.4765mW	3.2837mW

(7)設計想法

原本的設計是 Direct Form FIR 但會需要用到 28 個乘法器和加法器，這樣會造成面積過大，所以我採用 Folding 來讓只需要一個乘法器和加法器，但這就表示採樣頻率會變成原本的 1/28，造成 Latency 變長。這裡我設一個 reg index 來控制，當 index=28 時候 buffer 接 input 進來，index=0 時，multiplexer 根據 index 選出 d_input[0]和 tap[0]，然後進行乘法 D_in=d_input[0]*tap[0]，乘完之後會有一個 delay 進行累加 temp_output=temp_output+D_in，index=1，multiplexer 根據 index 選出 d_input[0]和 tap[0]，然後進行乘法 D_in=d_input[1]*tap[1] ，乘完之後會有一個 delay 加進行累加 temp_output=temp_output+D_in，以此類推，最後到 index=28 輸出 dout。