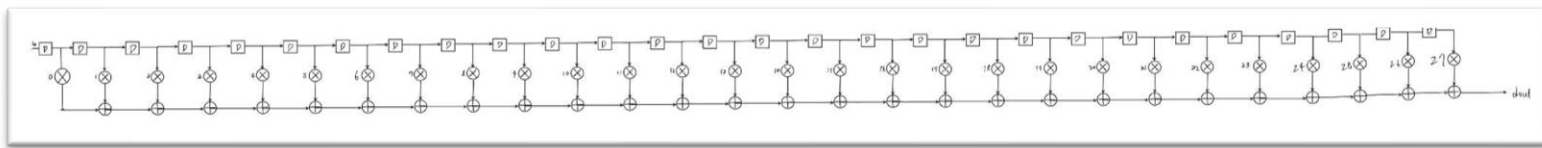


HW4 的基本設計

(速度 clock speed、資料運算吞吐量 throughput，面積/邏輯閘數/FPGA 成本，耗能)

下圖為 Direct Form FIR 架構



```
\timescale 1ns/10ps  
\define CYCLE 6.0
```

1. 速度 clock speed:6.0
2. 資料運算吞吐量 throughput:2.6 G bits/sec
3. 面積

```
area.log  
1  
2 *****  
3 Report : area  
4 Design : FIR  
5 Version: R-2020.09-SP5  
6 Date : Wed Jan 4 03:49:23 2023  
7 *****  
8  
9 Library(s) Used:  
10  
11 slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)  
12  
13 Number of ports: 4201  
14 Number of nets: 20627  
15 Number of cells: 15931  
16 Number of combinational cells: 14429  
17 Number of sequential cells: 1350  
18 Number of macros/black boxes: 0  
19 Number of buf/inv: 3544  
20 Number of references: 75  
21  
22 Combinational area: 172353.995716  
23 Buf/Inv area: 19128.000422  
24 Noncombinational area: 53788.907932  
25 Macro/Black Box area: 0.000000  
26 Net Interconnect area: 1556294.586029  
27  
28 Total cell area: 226142.903648  
29 Total area: 1782437.489677  
30
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33 Global cell area  
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35 Local cell area  
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37 Hierarchical cell  
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```

4. 耗能

```
power.log x
1 Loading db file '/home/m111/m111064503/cad/CBDK/CBDK_IC_Constest_v2.1/SynopsysDC/db/slow.db'
2 Information: Propagating switching activity (high effort zero delay simulation). (PWR-6)
3 Warning: Design has unannotated primary inputs. (PWR-414)
4 Warning: Design has unannotated sequential cell outputs. (PWR-415)
5
6 *****
7 Report : power
8         -analysis_effort high
9         -verbose
10 Design : FIR
11 Version: R-2020.09-SP5
12 Date   : Wed Jan  4 03:49:28 2023
13 *****
14
15
16 Library(s) Used:
17
18     slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Constest_v2.1/SynopsysDC/db/slow.db)
19
20
21 Operating Conditions: slow   Library: slow
22 Wire Load Model Mode: top
23
24 Design      Wire Load Model      Library
25 -----
26 FIR         tsmc13_wl10         slow
27
28
29 Global Operating Voltage = 1.08
30 Power-specific unit information :
31   Voltage Units = 1V
32   Capacitance Units = 1.000000pf
33   Time Units = 1ns
34   Dynamic Power Units = 1mW (derived from V,C,T units)
35   Leakage Power Units = 1pW
36
37
38 Cell Internal Power = 9.4328 mW (71%)
39 Net Switching Power = 3.8478 mW (28%)
40
41 Total Dynamic Power = 13.2806 mW (100%)
42
43 Cell Leakage Power = 195.8756 uW
44
45
46 Power Group      Internal      Switching      Leakage      Total      ( % )      Attrs      Cell
47 -----
48 io_pad           0.0000         0.0000         0.0000         0.0000         ( 0.00%)         0
49 memory           0.0000         0.0000         0.0000         0.0000         ( 0.00%)         0
50 black_box        0.0000         0.0000         0.0000         0.0000         ( 0.00%)         0
51 clock_network    0.0000         0.0000         0.0000         0.0000         ( 0.00%)         0
52 register         7.7387         0.3109         4.9670e+07      8.0993         ( 60.10%)        1350
53 sequential       0.0000         0.0000         0.0000         0.0000         ( 0.00%)         0
54 combinational    1.6941         3.5369         1.4621e+08      5.3772         ( 39.90%)       14429
55 -----
56 Total            9.4328 mW      3.8478 mW      1.9588e+08 pW   13.4765 mW
57
58
```

5. timing report:

```

power.log x timing.log x
3 Report : timing
4         -path full
5         -delay max
6         -max_paths 1
7 Design : FIR
8 Version: R-2020.09-SP5
9 Date   : Wed Jan 4 03:49:23 2023
10 *****
11
12 # A fanout number of 1000 was used for high fanout net computations.
13
14 Operating Conditions: slow Library: slow
15 Wire Load Model Mode: top
16
17 Startpoint: account_reg[5][0]
18             (rising edge-triggered flip-flop clocked by clk)
19 Endpoint: d_output_reg[31]
20           (rising edge-triggered flip-flop clocked by clk)
21 Path Group: clk
22 Path Type: max
23
24 Des/Clust/Port Wire Load Model Library
25 -----
26 FIR tsmc13_wl10 slow
27
28 Point ----- Incr Path
29
30 clock clk (rise edge) 0.00 0.00
31 clock network delay (ideal) 0.50 0.50
32 account_reg[5][0]/CK (DFFRX4) 0.00 # 0.50 r
33 account_reg[5][0]/Q (DFFRX4) 0.42 0.92 r
34 add_17_root_add_0_root_add_150_27/A[0] (FIR_DW01_add_50)
35 0.00 0.92 r
36 add_17_root_add_0_root_add_150_27/U487/Y (NAND2X8) 0.13 1.05 f
37 add_17_root_add_0_root_add_150_27/U486/Y (OAI21X4) 0.21 1.25 r
38 add_17_root_add_0_root_add_150_27/U249/Y (AOI21X4) 0.13 1.38 f
39 add_17_root_add_0_root_add_150_27/U197/Y (OAI21X4) 0.14 1.53 r
40 add_17_root_add_0_root_add_150_27/U195/Y (AOI21X4) 0.11 1.64 f
41 add_17_root_add_0_root_add_150_27/U375/Y (CLKBUF4) 0.38 2.02 f
42 add_17_root_add_0_root_add_150_27/U519/Y (OAI21X2) 0.28 2.30 r
43 add_17_root_add_0_root_add_150_27/U461/Y (XOR2X4) 0.24 2.54 r
44 add_17_root_add_0_root_add_150_27/SUM[24] (FIR_DW01_add_50)
45 0.00 2.54 r
46 add_9_root_add_0_root_add_150_27/B[24] (FIR_DW01_add_47)
47 0.00 2.54 r
48 add_9_root_add_0_root_add_150_27/U403/Y (NOR2X8) 0.15 2.68 f
49 add_9_root_add_0_root_add_150_27/U477/Y (NOR2X6) 0.13 2.82 r
50 add_9_root_add_0_root_add_150_27/U434/Y (INVX3) 0.12 2.93 f
51 add_9_root_add_0_root_add_150_27/U405/Y (INVX3) 0.13 3.07 r
52 add_9_root_add_0_root_add_150_27/U484/Y (NAND2X2) 0.12 3.19 f
53 add_9_root_add_0_root_add_150_27/U77/Y (OAI21X4) 0.16 3.34 r
54 add_9_root_add_0_root_add_150_27/U64/Y (XNOR2X4) 0.20 3.54 r
55 add_9_root_add_0_root_add_150_27/SUM[26] (FIR_DW01_add_47)
56 0.00 3.54 r
57 add_3_root_add_0_root_add_150_27/B[26] (FIR_DW01_add_40)
58 0.00 3.54 r
59 add_3_root_add_0_root_add_150_27/U511/Y (NAND2X4) 0.19 3.73 f
60 add_3_root_add_0_root_add_150_27/U531/Y (OAI21X4) 0.17 3.90 r
61 add_3_root_add_0_root_add_150_27/U57/Y (AOI21X4) 0.11 4.01 f
62 add_3_root_add_0_root_add_150_27/U483/Y (AOI21X2) 0.22 4.23 r
63 add_3_root_add_0_root_add_150_27/U536/Y (AOI21X4) 0.11 4.34 f
64 add_3_root_add_0_root_add_150_27/U545/Y (OAI21X4) 0.09 4.43 r
65 add_3_root_add_0_root_add_150_27/U442/Y (XNOR2X4) 0.19 4.62 r
66 add_3_root_add_0_root_add_150_27/SUM[29] (FIR_DW01_add_40)
67 0.00 4.62 r

```

```

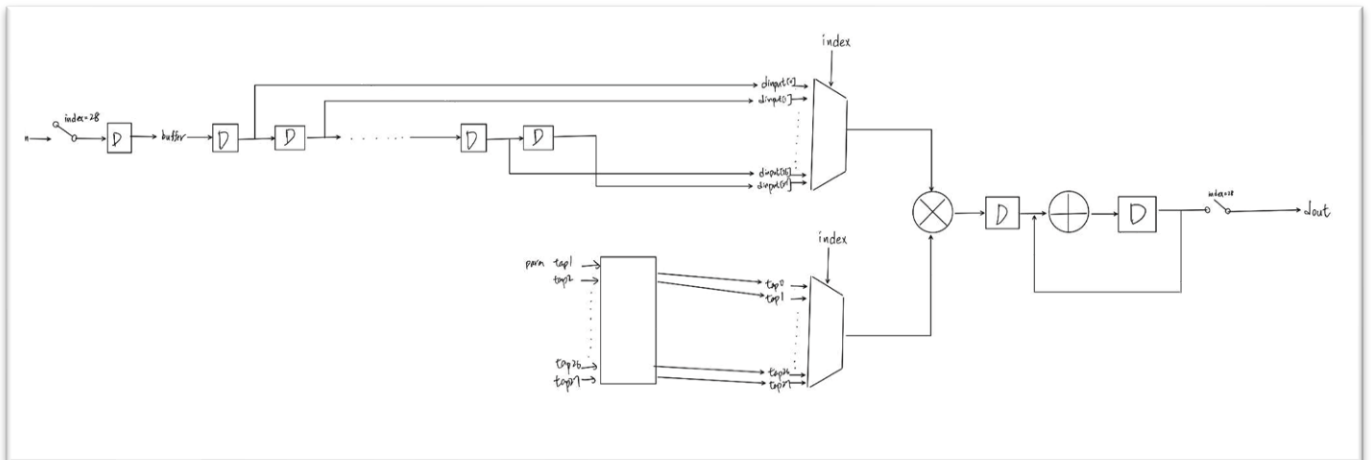
add_2_root_add_0_root_add_150_27/B[29] (FIR_DW01_add_41)
0.00 4.62 r
add_2_root_add_0_root_add_150_27/U482/Y (NOR2X8) 0.14 4.76 f
add_2_root_add_0_root_add_150_27/U536/Y (NOR2X8) 0.12 4.88 r
add_2_root_add_0_root_add_150_27/U535/Y (INVX8) 0.08 4.96 f
add_2_root_add_0_root_add_150_27/U547/Y (NOR2X8) 0.11 5.08 r
add_2_root_add_0_root_add_150_27/U374/Y (NAND2X4) 0.09 5.16 f
add_2_root_add_0_root_add_150_27/U490/Y (OAI21X4) 0.14 5.31 r
add_2_root_add_0_root_add_150_27/U456/Y (XOR2X4) 0.16 5.47 f
add_2_root_add_0_root_add_150_27/SUM[30] (FIR_DW01_add_41)
0.00 5.47 f
add_0_root_add_0_root_add_150_27/A[30] (FIR_DW01_add_27)
0.00 5.47 f
add_0_root_add_0_root_add_150_27/U561/Y (OR2X8) 0.19 5.66 f
add_0_root_add_0_root_add_150_27/U446/Y (AOI21X4) 0.15 5.81 r
add_0_root_add_0_root_add_150_27/U445/Y (OAI21X4) 0.10 5.91 f
add_0_root_add_0_root_add_150_27/U444/Y (AOI21X4) 0.12 6.04 r
add_0_root_add_0_root_add_150_27/U443/Y (OAI2BB1X4) 0.09 6.13 f
add_0_root_add_0_root_add_150_27/U439/Y (XNOR2X4) 0.11 6.24 r
add_0_root_add_0_root_add_150_27/SUM[31] (FIR_DW01_add_27)
0.00 6.24 r
d_output_reg[31]/D (DFFRHQX8) 0.00 6.24 r
data arrival time 6.24

clock clk (rise edge) 6.00 6.00
clock network delay (ideal) 0.50 6.50
clock uncertainty -0.10 6.40
d_output_reg[31]/CK (DFFRHQX8) 0.00 6.40 r
library setup time -0.16 6.24
data required time 6.24
-----
data required time 6.24
data arrival time -6.24
-----
slack (MET) 0.00

```

Final-Project-Report

下圖為 Folding FIR 架構圖：



*製成採用的是 tsmc13_neg.v

(1)預期規格：

➢面積：由前面所列作業四的合成 report 可以看到 cell area 面積很大，一共 22 萬，造成面積這麼大的原因是因為一共有 28 個乘法器和加法器，所以我主要是用 Folding 來減少面積，將原本 28 個乘法器和加法器，進行 Folding 後，只需要 1 個乘法器和加法器，我預期可以減少 2 倍以上的面積。

➢速度：Clock speed 是 6ns，critical path 是由一個乘法器和一個加法器所組成的，我採用 pipeline 來切開一個乘法器和一個加法器，將 critical path 切成只剩下乘法器，所以我預期可以減少 1ns 的 clock speed

2. Fixed Point 模擬

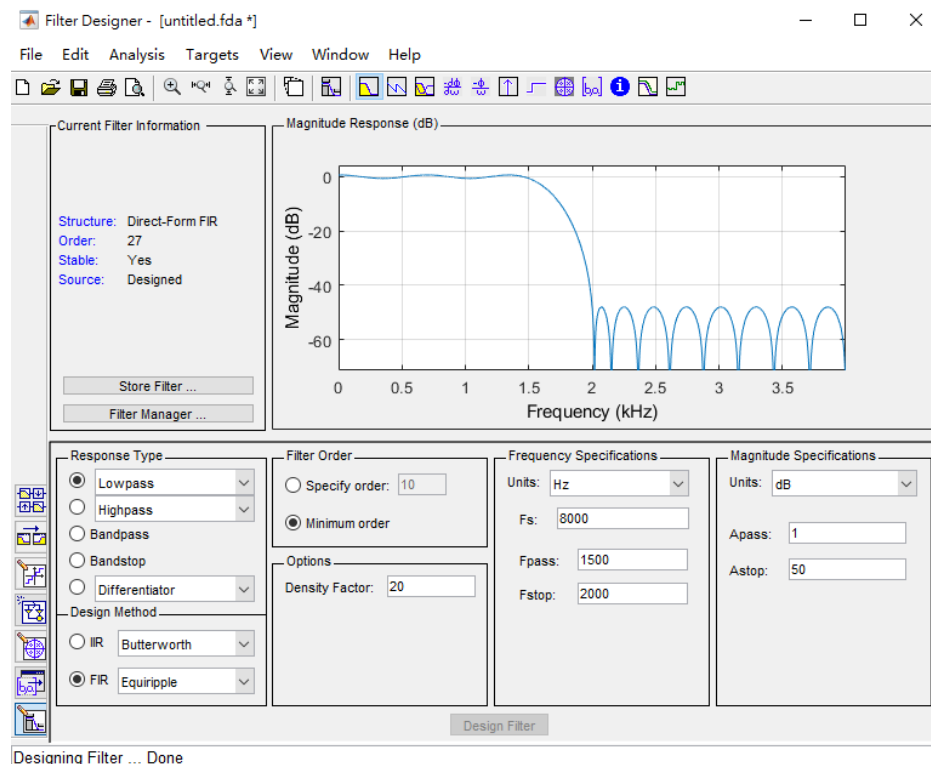
(a)

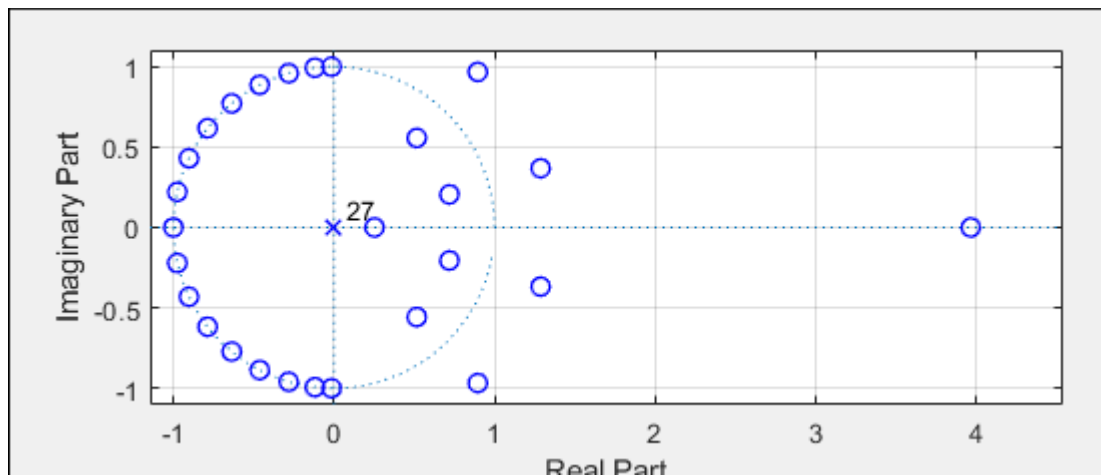
(i)floating coef:

-0.002964894749042235391756072715452319244
0.005015861152363371849860484985583752859
0.020667893101735827776632703489667619579
0.025148888112610387479683993205981096253
0.002316865275779686830781578521509800339
-0.025779624933500097649918814113334519789
-0.015946518131217442965086306116972991731

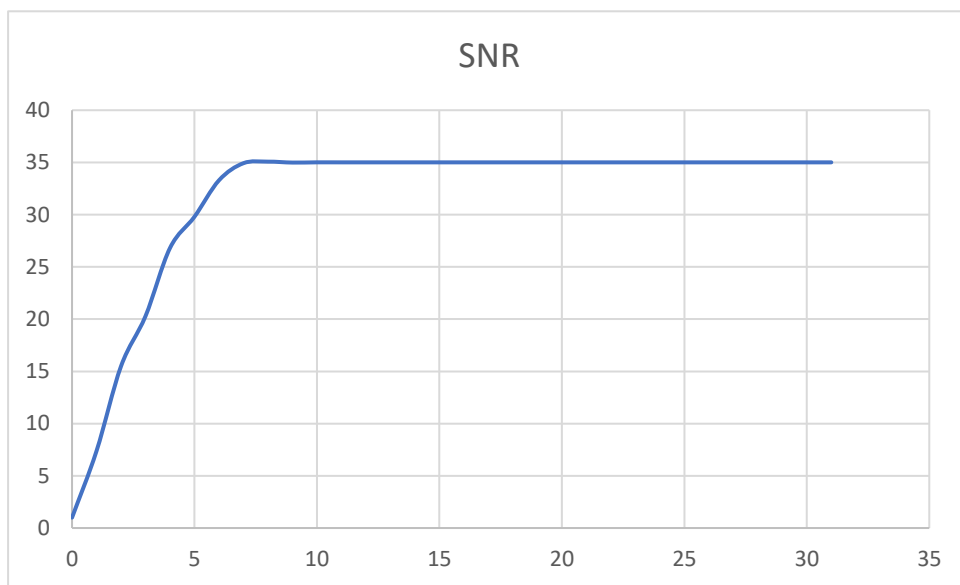
0. 029216940020626670782011302662795060314
 0. 042349361155728501571182675888849189505
 -0. 02019719422775444889195384234881203156
 -0. 085611751306674921391248744839685969055
 -0. 021255965443284792482092626642042887397
 0. 191877715214637978302647525197244249284
 0. 391355121984242604327164372080005705357
 0. 391355121984242604327164372080005705357
 0. 191877715214637978302647525197244249284
 -0. 021255965443284792482092626642042887397
 -0. 085611751306674921391248744839685969055
 -0. 02019719422775444889195384234881203156
 0. 042349361155728501571182675888849189505
 0. 029216940020626670782011302662795060314
 -0. 015946518131217442965086306116972991731
 -0. 025779624933500097649918814113334519789
 0. 002316865275779686830781578521509800339
 0. 025148888112610387479683993205981096253
 0. 020667893101735827776632703489667619579
 0. 005015861152363371849860484985583752859
 -0. 002964894749042235391756072715452319244

(ii)





(b)



可以看到在精度為 8 左右就開始收斂了

我採用精度為 15

➔ SNR loss=0 dB

(3)presim:

```
daisy.ee.nthu.edu.tw (m111064503)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/home/m111/m111064503/Foldi
Name
sim
src
syn

At index= 39979, output=56374, golden=56374, PASS !!
At index= 39980, output=60292, golden=60293, PASS !!
At index= 39981, output=65423, golden=65423, PASS !!
At index= 39982, output= 2318, golden= 2318, PASS !!
At index= 39983, output= 826, golden= 827, PASS !!
At index= 39984, output=62513, golden=62514, PASS !!
At index= 39985, output=58143, golden=58143, PASS !!
At index= 39986, output=53944, golden=53944, PASS !!
At index= 39987, output=50164, golden=50164, PASS !!
At index= 39988, output=47639, golden=47640, PASS !!
At index= 39989, output=46891, golden=46892, PASS !!
At index= 39990, output=47145, golden=47146, PASS !!
At index= 39991, output=47203, golden=47203, PASS !!
At index= 39992, output=47204, golden=47204, PASS !!
At index= 39993, output=48446, golden=48447, PASS !!
At index= 39994, output=51042, golden=51043, PASS !!
At index= 39995, output=52993, golden=52994, PASS !!
At index= 39996, output=52527, golden=52527, PASS !!
At index= 39997, output=50993, golden=50994, PASS !!
At index= 39998, output=51990, golden=51990, PASS !!
At index= 39999, output=57461, golden=57462, PASS !!
At index= 40000, output=65438, golden=65438, PASS !!
At index= 40001, output= 6330, golden= 6330, PASS !!
At index= 40002, output= 9374, golden= 9375, PASS !!
At index= 40003, output=10750, golden=10750, PASS !!
At index= 40004, output=13013, golden=13013, PASS !!
At index= 40005, output=16245, golden=16245, PASS !!
At index= 40006, output=18153, golden=18154, PASS !!
At index= 40007, output=17369, golden=17369, PASS !!
At index= 40008, output=15809, golden=15810, PASS !!
At index= 40009, output=16703, golden=16704, PASS !!
At index= 40010, output=20290, golden=20291, PASS !!
At index= 40011, output=22525, golden=22526, PASS !!
At index= 40012, output=19191, golden=19192, PASS !!
At index= 40013, output=10740, golden=10740, PASS !!
At index= 40014, output= 2290, golden= 2290, PASS !!
At index= 40015, output=64055, golden=64055, PASS !!
At index= 40016, output=64912, golden=64913, PASS !!
At index= 40017, output= 1316, golden= 1316, PASS !!
At index= 40018, output= 1583, golden= 1584, PASS !!
At index= 40019, output= 555, golden= 556, PASS !!
At index= 40020, output= 6, golden= 6, PASS !!
At index= 40021, output= 477, golden= 477, PASS !!
At index= 40022, output= 1066, golden= 1066, PASS !!
At index= 40023, output= 1000, golden= 1000, PASS !!
At index= 40024, output= 460, golden= 460, PASS !!
At index= 40025, output= 35, golden= 36, PASS !!
At index= 40026, output=65476, golden=65477, PASS !!

All pass!!!
$finish called from file "FIR_tb.v", line 68.
$finish at simulation time 429492745
VCS Simulation Report
Time: 4294927450 ps
CPU Time: 13.040 seconds; Data structure size: 0.0Mb
Tue Jan 10 16:16:43 2023
CPU time: .543 seconds to compile + .579 seconds to elab + .467 seconds to link + 13.105 seconds in simulation
[m111064503@ws44 src]$
```

(4)gate level simulation:

```
daisy.ee.nthu.edu.tw (m111064503)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/home/m111/m111064503/Foldi
Name
sim
src
syn

At index= 39979, output=56374, golden=56374, PASS !!
At index= 39980, output=60292, golden=60293, PASS !!
At index= 39981, output=65423, golden=65423, PASS !!
At index= 39982, output= 2318, golden= 2318, PASS !!
At index= 39983, output= 826, golden= 827, PASS !!
At index= 39984, output=62513, golden=62514, PASS !!
At index= 39985, output=58143, golden=58143, PASS !!
At index= 39986, output=53944, golden=53944, PASS !!
At index= 39987, output=50164, golden=50164, PASS !!
At index= 39988, output=47639, golden=47640, PASS !!
At index= 39989, output=46891, golden=46892, PASS !!
At index= 39990, output=47145, golden=47146, PASS !!
At index= 39991, output=47203, golden=47203, PASS !!
At index= 39992, output=47204, golden=47204, PASS !!
At index= 39993, output=48446, golden=48447, PASS !!
At index= 39994, output=51042, golden=51043, PASS !!
At index= 39995, output=52993, golden=52994, PASS !!
At index= 39996, output=52527, golden=52527, PASS !!
At index= 39997, output=50993, golden=50994, PASS !!
At index= 39998, output=51990, golden=51990, PASS !!
At index= 39999, output=57461, golden=57462, PASS !!
At index= 40000, output=65438, golden=65438, PASS !!
At index= 40001, output= 6330, golden= 6330, PASS !!
At index= 40002, output= 9374, golden= 9375, PASS !!
At index= 40003, output=10750, golden=10750, PASS !!
At index= 40004, output=13013, golden=13013, PASS !!
At index= 40005, output=16245, golden=16245, PASS !!
At index= 40006, output=18153, golden=18154, PASS !!
At index= 40007, output=17369, golden=17369, PASS !!
At index= 40008, output=15809, golden=15810, PASS !!
At index= 40009, output=16703, golden=16704, PASS !!
At index= 40010, output=20290, golden=20291, PASS !!
At index= 40011, output=22525, golden=22526, PASS !!
At index= 40012, output=19191, golden=19192, PASS !!
At index= 40013, output=10740, golden=10740, PASS !!
At index= 40014, output= 2290, golden= 2290, PASS !!
At index= 40015, output=64055, golden=64055, PASS !!
At index= 40016, output=64912, golden=64913, PASS !!
At index= 40017, output= 1316, golden= 1316, PASS !!
At index= 40018, output= 1583, golden= 1584, PASS !!
At index= 40019, output= 555, golden= 556, PASS !!
At index= 40020, output= 6, golden= 6, PASS !!
At index= 40021, output= 477, golden= 477, PASS !!
At index= 40022, output= 1066, golden= 1066, PASS !!
At index= 40023, output= 1000, golden= 1000, PASS !!
At index= 40024, output= 460, golden= 460, PASS !!
At index= 40025, output= 35, golden= 36, PASS !!
At index= 40026, output=65476, golden=65477, PASS !!

All pass!!!
$finish called from file "FIR_syn_tb.v", line 68.
$finish at simulation time 5664657880
VCS Simulation Report
Time: 980.450 seconds; Data structure size: 1.1Mb
CPU Time: 2.233 seconds;
Tue Jan 10 15:12:01 2023
CPU time: .799 seconds to compile + .835 seconds to elab + .835 seconds to link + 980.550 seconds in simulation
[m111064503@ws44 syn]$
```


(5) synthesis Report

1.area report:

從原本 cell area 22 萬降到 7 萬，少了 3 倍，達到預期規格面積少 2 倍以上。

```
area.log
1
2 *****
3 Report : area
4 Design : FIR
5 Version: R-2020.09-SP5
6 Date   : Tue Jan 10 15:02:48 2023
7 *****
8
9 Library(s) Used:
10
11     slow (File: /home/m111/m111064503/cad/CBDK/CBDK_IC_Constest_v2.1/SynopsysDC/db/slow.db)
12
13 Number of ports:          35
14 Number of nets:          4747
15 Number of cells:         4287
16 Number of combinational cells: 3717
17 Number of sequential cells:   570
18 Number of macros/black boxes: 0
19 Number of buf/inv:         747
20 Number of references:      137
21
22 Combinational area:      51449.891363
23 Buf/Inv area:            7762.210212
24 Noncombinational area:   18608.595634
25 Macro/Black Box area:    0.000000
26 Net Interconnect area:   448188.984436
27
28 Total cell area:         70058.486998
29 Total area:              518247.471434
30
31 Hierarchical area distribution
32 -----
33
34                               Global cell area          Local cell area
35                               -----
36 Hierarchical cell            Absolute   Percent   Combi-   Noncombi-   Black-   Design
37                               Total      Total     national national   boxes
38                               -----
39 FIR                          70058.4870   100.0    51449.8914 18608.5956 0.0000   FIR
40                               -----
41 Total                        -----
42                               51449.8914 18608.5956 0.0000
43 1
44
```

2.timing report:

```
`timescale 1ns/10ps
`define CYCLE 4.88
```

從 timing report 看出 critical path 只剩下乘法器，

所以有成功在乘法和加法器之間切 pipeline，6-

4.88=1.12ns，也有達成預期規格少 1ns 的要求。

12	Operating Conditions: slow	Library: slow
13	Wire Load Model Mode: top	
14		
15	Startpoint: index_reg[4]	
16	(rising edge-triggered flip-flop clocked by clk)	
17	Endpoint: D_in_reg[11]	
18	(rising edge-triggered flip-flop clocked by clk)	
19	Path Group: clk	
20	Path Type: max	
21		
22	Des/Clust/Port	Wire Load Model Library
23	-----	-----
24	FIR	tsmc13_wl10 slow
25		
26	Point	Incr Path
27	-----	-----
28	clock clk (rise edge)	0.00 0.00
29	clock network delay (ideal)	0.50 0.50
30	index_reg[4]/CK (DFFRX4)	0.00 0.50 r
31	index_reg[4]/Q (DFFRX4)	0.54 1.04 f
32	U4686/Y (NOR2X8)	0.16 1.20 r
33	U5302/Y (NAND2X8)	0.14 1.35 f
34	U3975/Y (INVX12)	0.09 1.43 r
35	U4123/Y (NAND2X8)	0.09 1.53 f
36	U4122/Y (INVX20)	0.15 1.68 r
37	U4096/Y (NAND2X6)	0.09 1.77 f
38	U4842/Y (NAND4X6)	0.14 1.90 r
39	U4231/Y (NOR3X8)	0.10 2.00 f
40	U4055/Y (NAND3X8)	0.11 2.11 r
41	U4177/Y (XOR2X4)	0.24 2.35 r
42	U4167/Y (AND2X8)	0.23 2.58 r
43	U4165/Y (INVX12)	0.08 2.66 f
44	U4201/Y (BUF2X8)	0.12 2.78 f
45	U3251/Y (INVX12)	0.06 2.84 r
46	U5433/Y (NAND2X4)	0.07 2.91 f
47	U3165/Y (NAND3X4)	0.13 3.04 r
48	U5098/Y (NOR2X8)	0.09 3.13 f
49	U4205/Y (INVX4)	0.08 3.21 r
50	U5182/Y (NAND2X6)	0.07 3.28 f
51	U3056/Y (NAND2X6)	0.08 3.36 r
52	U5179/Y (XOR2X4)	0.13 3.49 r
53	U5138/Y (XNOR2X4)	0.24 3.73 r
54	U5137/Y (INVX12)	0.10 3.83 f
55	U2913/Y (BUF2X8)	0.14 3.97 f
56	U5873/CO (ACHCINX4)	0.35 4.32 f
57	U5874/Y (NAND2X2)	0.26 4.58 r
58	U5875/Y (NAND2X2)	0.13 4.71 f
59	U5877/Y (NAND3X2)	0.14 4.86 r
60	U5878/Y (XNOR2X4)	0.16 5.02 f
61	U2833/Y (NOR2X4)	0.10 5.12 r
62	D_in_reg[11]/D (DFFRX2)	0.00 5.12 r
63	data arrival time	5.12
64		
65	clock clk (rise edge)	4.88 4.88
66	clock network delay (ideal)	0.50 5.38
67	clock uncertainty	-0.10 5.28
68	D_in_reg[11]/CK (DFFRX2)	0.00 5.28 r
69	library setup time	-0.16 5.12
70	data required time	5.12
71	-----	-----
72	data required time	5.12
73	data arrival time	-5.12
74	-----	-----
75	slack (MET)	0.00
76		

3. power report:

```

1 timing.log x timing.log x power.log x
2 Information: Propagating switching activity (high effort zero delay simulation). (PWR-6)
3 Warning: Design has unannotated primary inputs. (PWR-414)
4 Warning: Design has unannotated sequential cell outputs. (PWR-415)
5 *****
6 Report : power
7 -analysis_effort high
8 -verbose
9 Design : FIR
10 Version: R-2020.09-SP5
11 Date : Tue Jan 10 15:02:50 2023
12 *****
13
14
15 Library(s) Used:
16
17 slow (File: /home/m111/m11064503/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)
18
19
20 Operating Conditions: slow Library: slow
21 Wire Load Model Mode: top
22
23 Design Wire Load Model Library
24 -----
25 FIR tsmc13_wl10 slow
26
27
28 Global Operating Voltage = 1.08
29 Power-specific unit information :
30 Voltage Units = 1V
31 Capacitance Units = 1.000000pf
32 Time Units = 1ns
33 Dynamic Power Units = 1mW (derived from V,C,T units)
34 Leakage Power Units = 1pW
35
36
37 Cell Internal Power = 2.6329 mW (82%)
38 Net Switching Power = 586.1702 uW (18%)
39
40 Total Dynamic Power = 3.2191 mW (100%)
41
42 Cell Leakage Power = 64.7248 uW
43
44
45 Power Group Internal Power Switching Power Leakage Power Total Power ( % ) Attrs Count
46 -----
47 io_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%) 0
48 memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%) 0
49 block_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%) 0
50 clock_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%) 0
51 register 2.4479 1.8097e-02 1.6887e+07 2.4829 ( 75.61%) 570
52 sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%) 0
53 combinational 0.1850 0.5681 4.7837e+07 0.8009 ( 24.39%) 3717
54 -----
55 Total 2.6329 mW 0.5862 mW 6.4725e+07 pW 3.2838 mW
56 1
57

```

4. Throughput=117M bits/sec

(6) 設計前與設計後比較

設計	Direct Form FIR(前)	Folding FIR(後)
Clock speed	6.0	4.88
Hardware cost (cell area)	226242	70058
Throughput	2.6 G bits/sec	117M bits/sec
power	13.4765mW	3.2837mW

(7)設計想法

原本的設計是 Direct Form FIR 但會需要用到 28 個乘法器和加法器，這樣會造成面積過大，所以我採用 Folding 來讓只需要一個乘法器和加法器，但這就表示採樣頻率會變成原本的 1/28，造成 Latency 變長。這裡我設一個 reg index 來控制，當 index=28 時候 buffer 接 input 進來，index=0 時，multiplexer 根據 index 選出 d_input[0]和 tap[0]，然後進行乘法

$D_in = d_input[0] * tap[0]$ ，乘完之後會有一個 delay 進行累加

$temp_output = temp_output + D_in$ ，index=1，multiplexer 根據 index 選出

d_input[0]和 tap[0]，然後進行乘法 $D_in = d_input[1] * tap[1]$ ，乘完之後會有一個 delay 加進行累加 $temp_output = temp_output + D_in$ ，以此類推，最後到 index=28 輸出 dout。