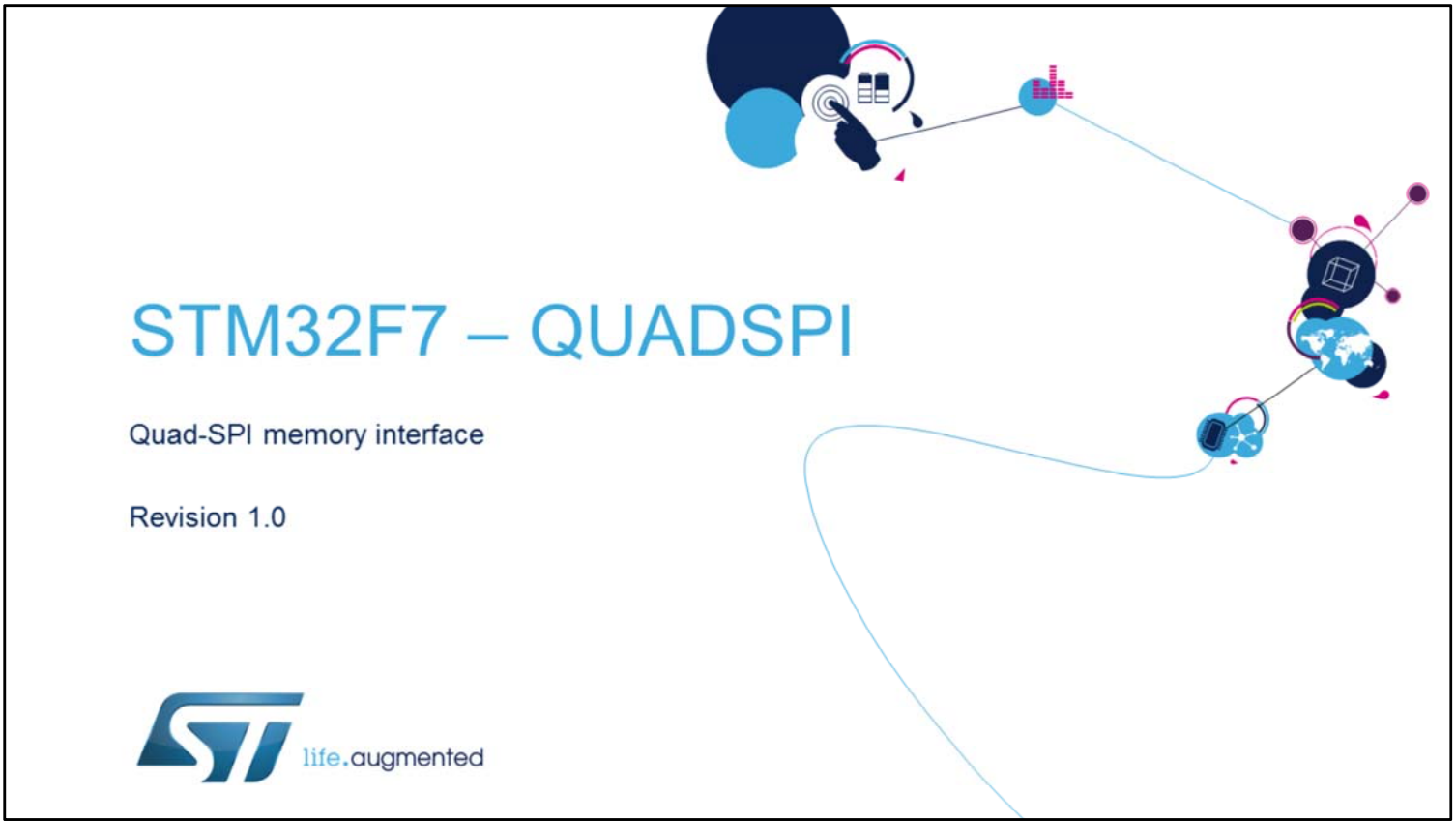


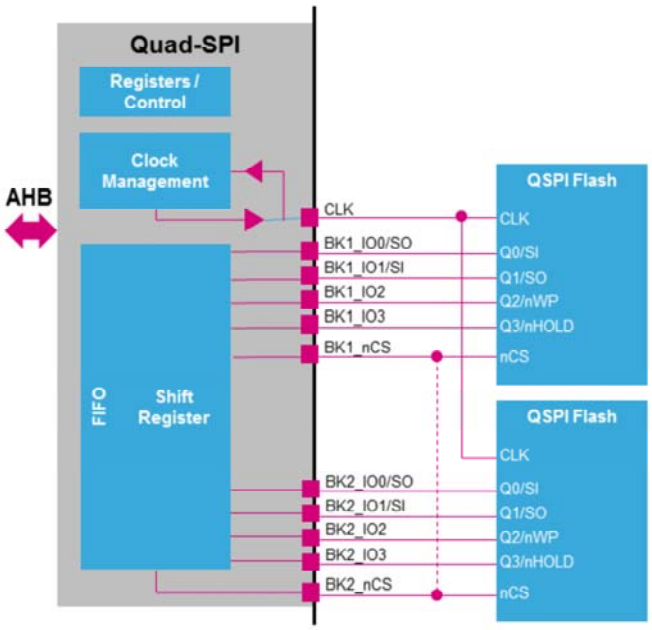
Hello, and welcome to this presentation of the STM32 Quad-SPI memory interface. It covers the features of this interface, which is widely used for connecting external memories to the microcontroller.

Single or dual Quad-SPI access?

2

Flexible selection between number of pins and performance

- Quad-SPI supports single and dual external Flash operation(*)
- 4-bit or 8-bit data bus



* : depends on part numbers

The Quad-SPI memory interface integrated inside STM32F7 microcontrollers provides a communication interface, allowing the microcontroller to communicate with external SPI and Quad-SPI memories.
The Quad-SPI memory interface supports the connection of one or two external memories. This means that data can be transferred over a 4- or 8-bit data bus in between the memory and the microcontroller. It gives the user flexibility to choose between the number of pins required for connection (6 for a single and 10 for a double connection) and the performance of the data transfer (4 bits for a single or 8 bits for a double connection).

Key features

- Three operating modes
  - Indirect
  - Status-polling
  - Memory-mapped
- Optimized operations up to 100 MHz(**)
  - Dual-Flash mode* (8 bits for accessing two Flash memories in parallel)
  - Single data rate (SDR) and Dual data rate (*) (DDR) support

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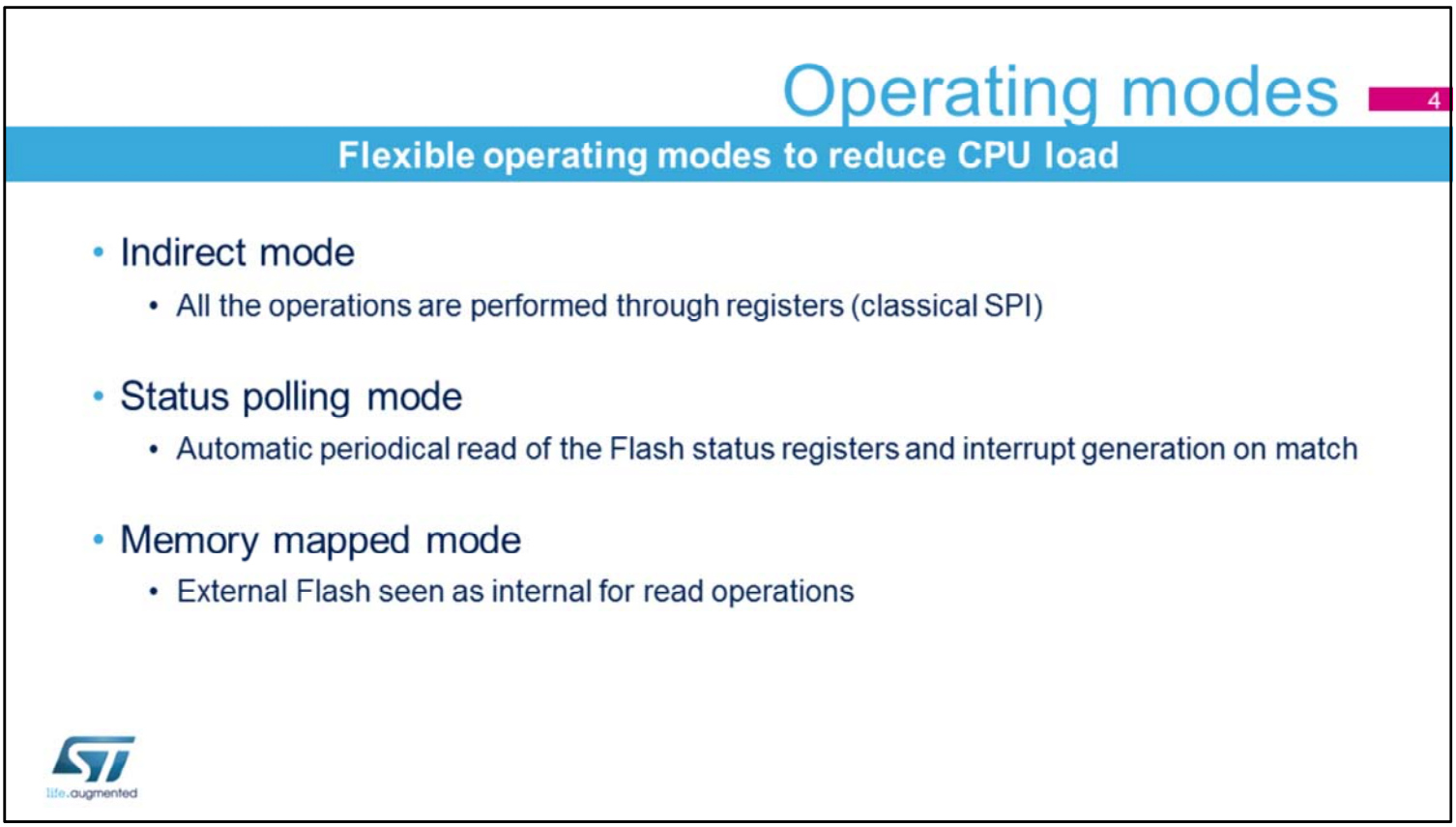
* : Depends on part numbers
** : For the full range of VDD from 1.71 to 3.6 V

The Quad-SPI memory interface offers three operating modes. It is optimized for communication with external memories with support for Dual-Flash mode, allowing to access 8 bits in a single reading cycle. It also supports both single- and dual-data rate operation.



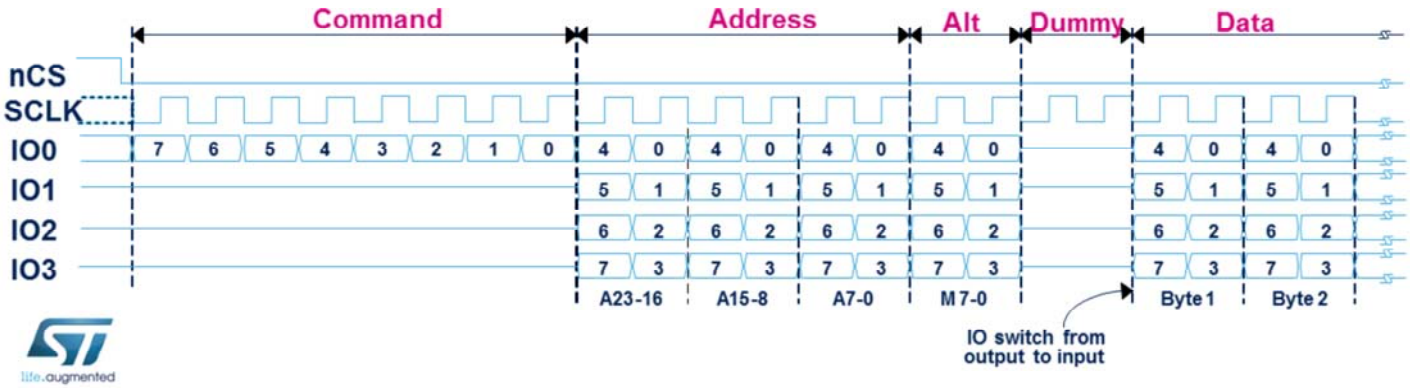
The Quad-SPI memory interface operates in three different modes:
1. Indirect mode, where it behaves as classical SPI interface and all operations are performed through registers,
2. Status-polling mode, where the Flash status registers are read periodically with interrupt generation,
3. Memory-mapped mode, where the external memory is seen as an internal memory for read operations.

Frame format

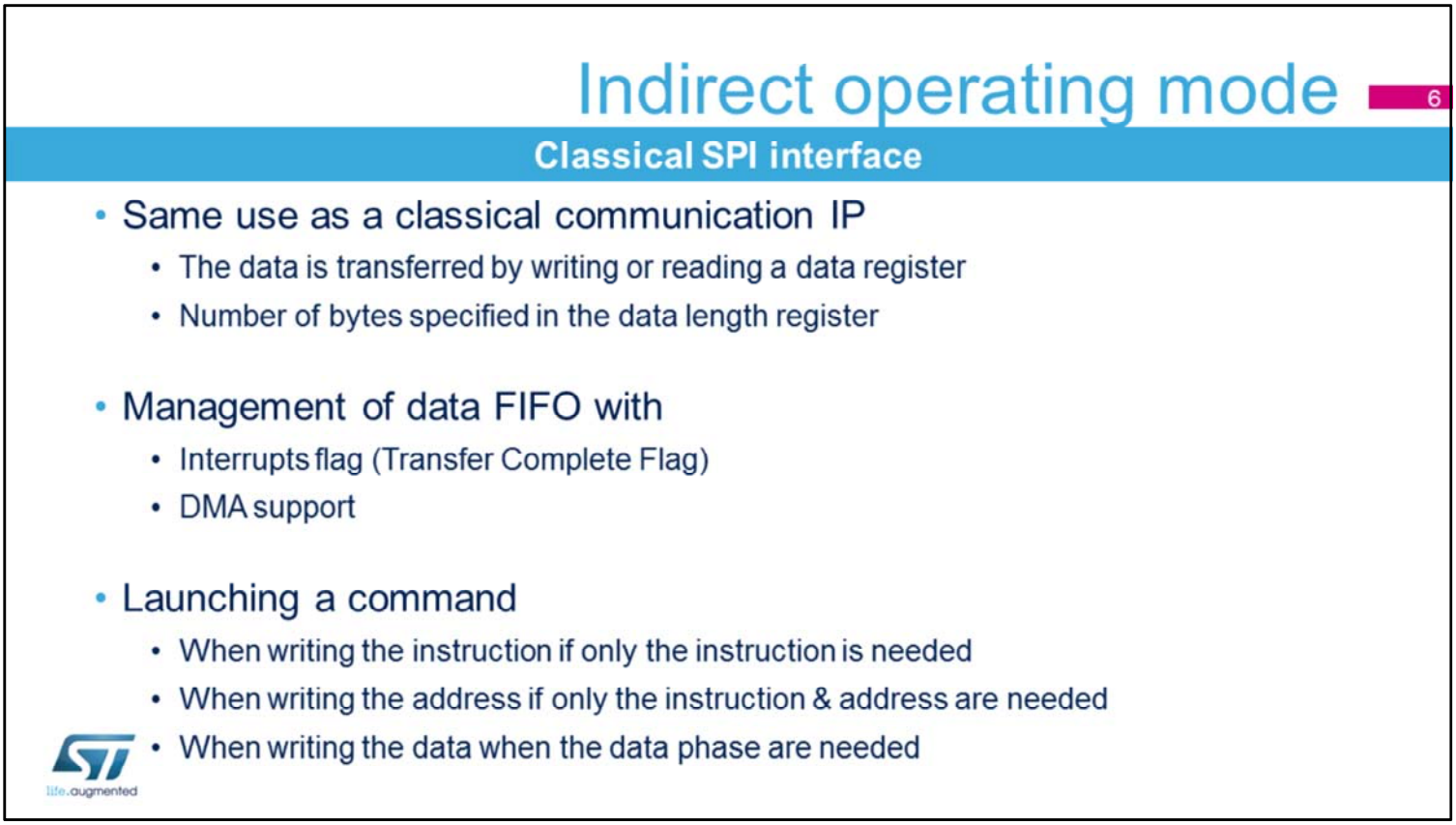
5

Compatible with any single/dual/quad SPI serial Flash memory

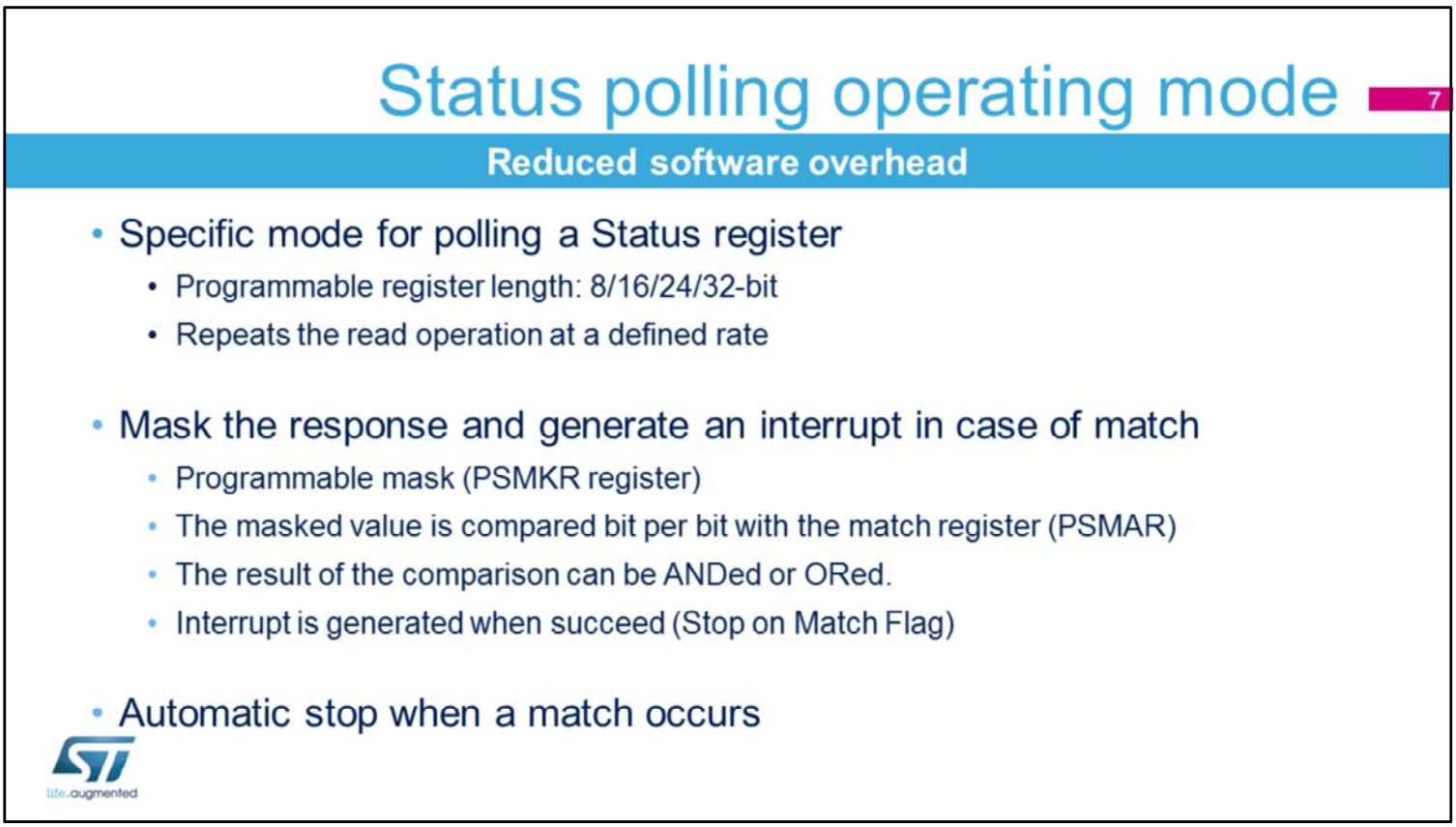
- Quad-SPI commands contain up to 5 configurable phases
  - Each phase could be enabled or disabled
  - Configurable length for each phase
  - Configurable number of lines for each phase



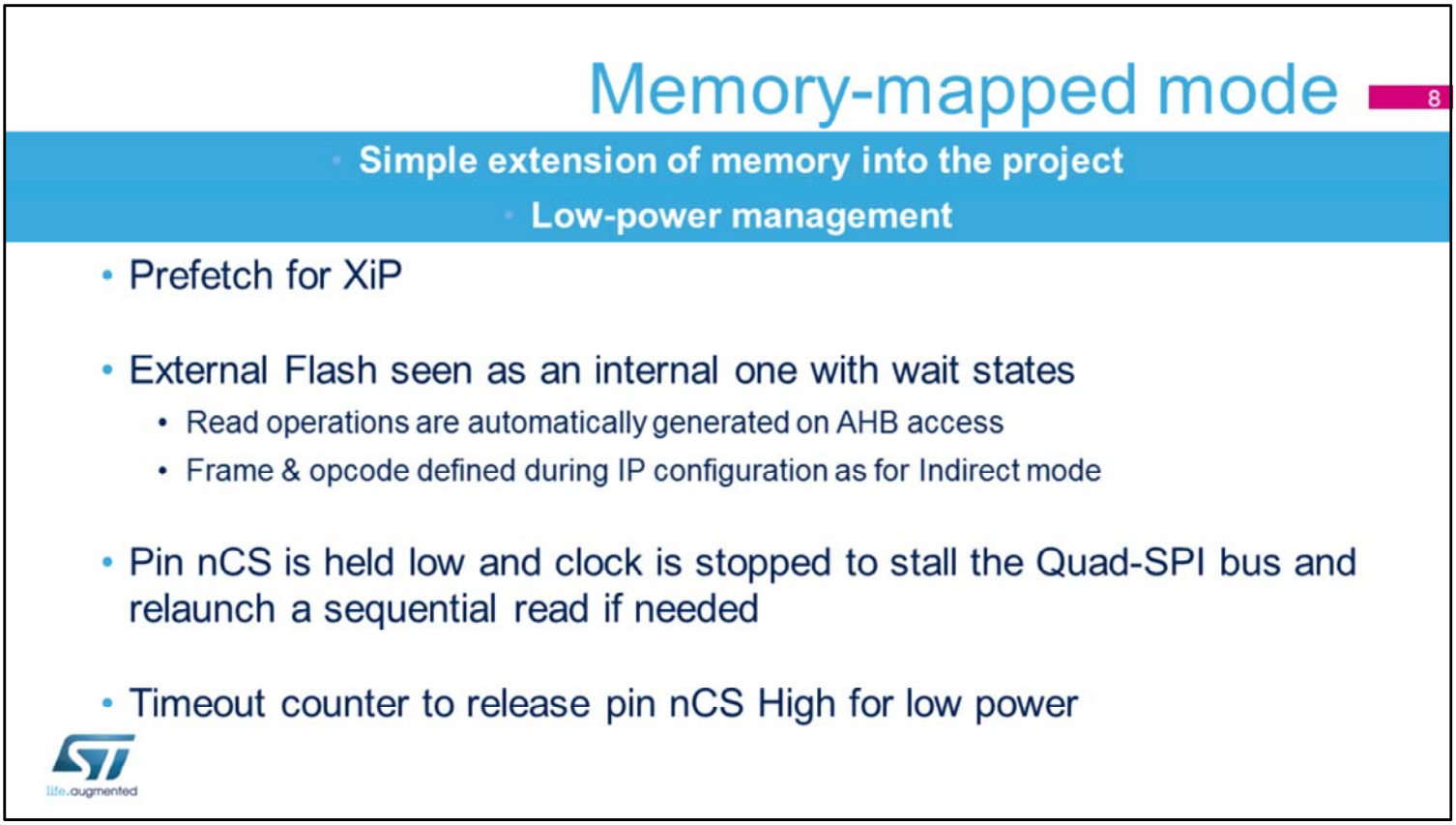
The Quad-SPI memory interface offers high flexibility in frame format configuration. This flexibility allows it to address any serial Flash memory. Users can enable or disable each of the five phases and configure the length of each phase as well as the number of lines used for each phase.



The Quad-SPI memory interface used in indirect operating mode behaves like a classical SPI interface. Transferred data goes through the data register with FIFO. Data exchanges are driven by software or by the DMA controller, using related interrupt flags in the Quad-SPI status registers. Each command is launched by writing the instruction, address or data, depending on the instruction context.

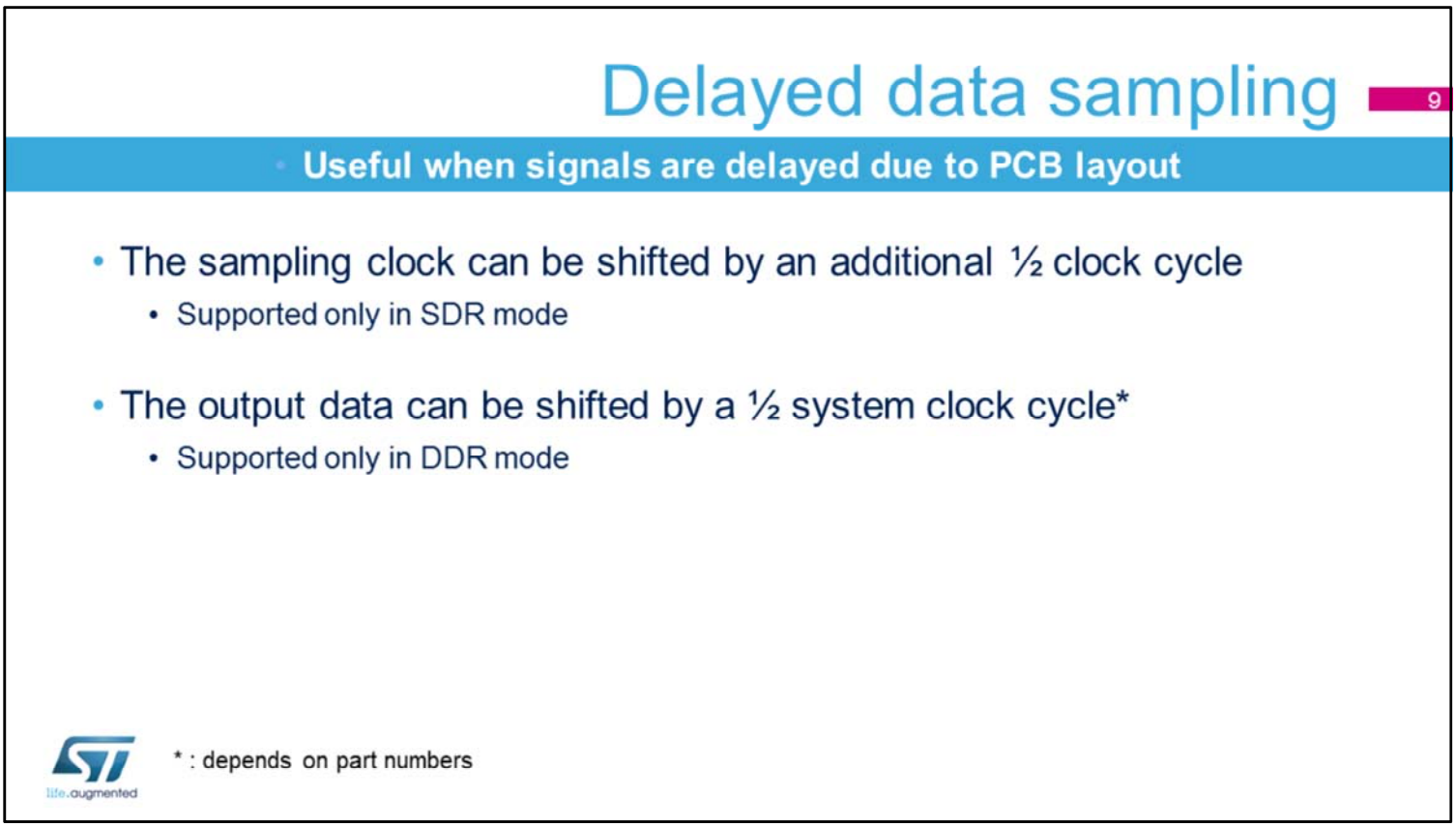


A specific mode has been implemented in the Quad-SPI interface to autonomously poll the status registers in the external Flash memory. The Quad-SPI interface can also be configured to periodically read a register in the external Flash memory. The returned data can be masked to select the bits to be evaluated. The selected bits are compared with their required values stored in the match register. The result of the comparison can be treated in two ways: in ANDed mode, if all the selected bits are matching, an interrupt is generated. In ORed mode, if one of the selected bits is matching, an interrupt is generated. When a match occurs, the Quad-SPI interface can stop automatically.



The Quad-SPI memory interface also has a Memory-mapped mode. The main application benefit introduced by this mode is the simple integration of an external memory extension thanks to there being no difference between the read accesses of internal or externally-connected memories, except for the number of wait states.
This mode is only suitable for read operations and the external Flash memory is seen as internal one with wait states included to compensate for the lower speed of the external memory. The maximum size supported by this mode is limited to 256 Mbytes.
The prefetch buffer supports execution in place, therefore code can be executed directly from the external memory without having to download it into the internal RAM.
This mode also supports SIOO mode [“S” “I” “O” “O”] (Send Instruction Only Once) supported by certain Flash memories, which allows the controller to send an instruction only once and to remove the instruction phase for following

accesses.



Delayed data sampling allows users to compensate for the delay of the signals due to constraints on the PCB layout optimization. It allows applications to shift the data sampling time by an additional ½ clock cycle when operating in SDR mode. In DDR mode, the output data can be shifted by a ½ system clock cycle to relax hold constraints.

Interrupts and DMA

Interrupt event	Description
Timeout	Set when timeout occurs.
Status match	Set in automatic Polling mode when the masked received data matches the corresponding bits in the match register.
FIFO threshold	Set in Indirect mode when the FIFO threshold has been reached.
Transfer complete	Set in Indirect mode when the programmed number of data has been transferred or in any mode when the transfer has been aborted.
Transfer error	Set in Indirect mode when an Invalid address is being accessed.

- DMA requests can be generated in Indirect mode when FIFO threshold is reached.

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The Quad-SPI memory interface has 5 interrupt sources: Timeout, Status Match when the masked received data matches the corresponding bits in the match register in Automatic Polling mode, FIFO Threshold, Transfer Complete and Transfer Error.
DMA requests can be generated in Indirect mode when the FIFO threshold is reached.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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The Quad-SPI memory interface is active in Run and Sleep modes. A Quad-SPI interrupt can cause the device to exit Sleep mode. In Stop mode, the Quad-SPI memory interface is frozen and its registers content is kept. In Standby mode, the Quad-SPI is powered-down and it must be reinitialized afterwards.

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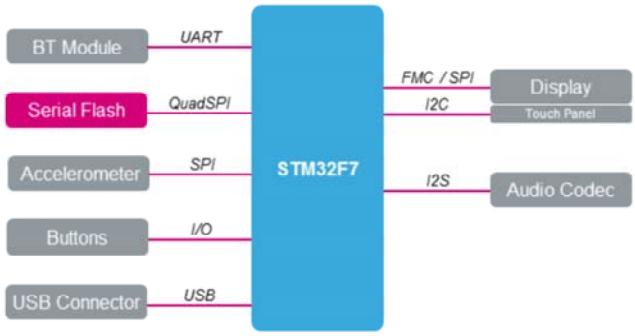
Application examples

- Wearable applications including connectivity and user interface:



- External Quad-SPI can store graphical (icons, fonts…etc…) and audio data required for user interface.

Wearable applications require low-power management functions together with a high-quality user interface. This can be achieved using the STM32F7's Quad-SPI interface to store in an external Flash memory all the graphical content needed including background images, high resolution icons, or fonts to support multiple languages. Additional audio data for ringtones can also benefit from the large space offered by an external Flash memory. The low pin-count needed to drive such devices allows for a highly optimized system integration.

Related peripherals

- Refer to these trainings related to this peripheral:
  - RCC (Quad-SPI clock control, Quad-SPI enable/reset)
  - Interrupts (Quad-SPI interrupt mapping)
  - DMA (Quad-SPI data transfer)
  - GPIO (Quad-SPI input/output pins)

You can refer to the training slides related to the RCC, interrupts, DMA and GPIOs for additional information.

Comparison across STM32 series

QUADSPI features	STM32L4	STM32F0	STM32F1	STM32F2	STM32F3	STM32F4	STM32F7
Number of instances	1	0	0	0	0	1	1
Maximum speed	48 MHz	N/A	N/A	N/A	N/A	90 MHz	100 MHz
Dual Flash	N	N/A	N/A	N/A	N/A	Y	Y
Software compatibility	N/A	N/A	N/A	N/A	N/A		

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Low-level drivers software compatibility:

- Full or almost full
- Partial
- No compatibility

The Quad-SPI is also implemented in some STM32F4 and STM32L4 devices, however, the STM32F4 and STM32F7 offer Dual-Flash support and higher I/O speeds.