PSoC® Creator™
Project Datasheet for SELVoltageMonitor

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Table of Contents

1 Overview

The Cypress PSoC 6 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M4 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 63 series member PSoC 6 device. For details on all the systems listed above, please refer to the PSoC 6 Technical Reference Manual .

Figure 1. PSoC 63 Device Series Block Diagram

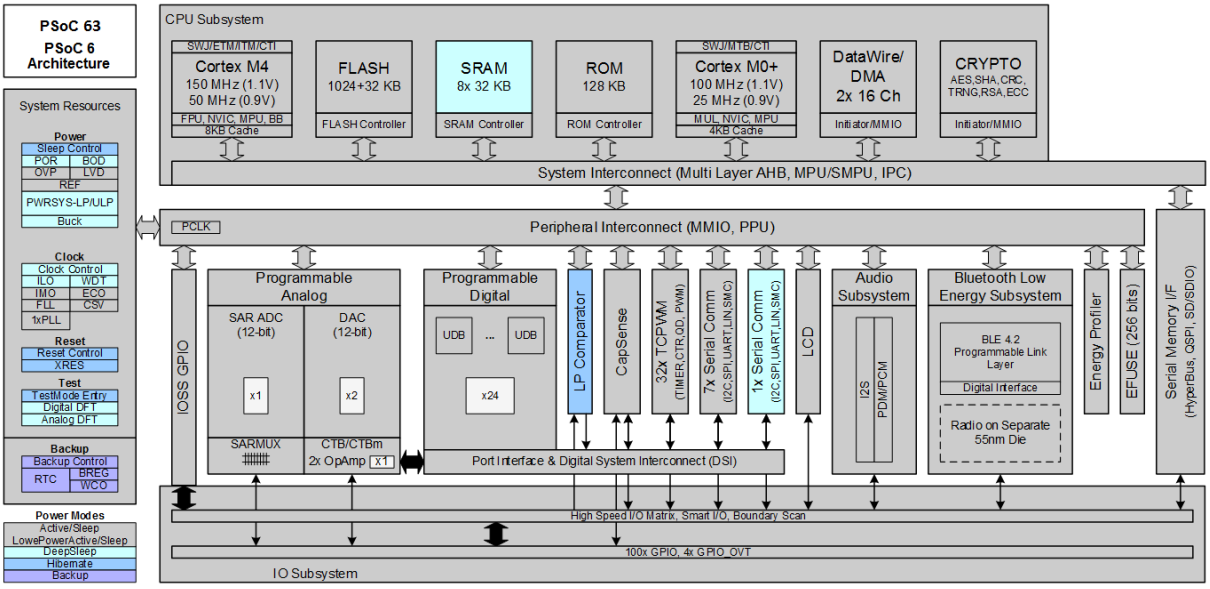


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CYBLE-416045-02
Package Name	43-SMT
Family	PSoC 6
Series	PSoC 63
Max CPU speed (MHz)	150
Flash size (kB)	1024
SRAM size (kB)	288
Vdd range (V)	1.7 to 3.6
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

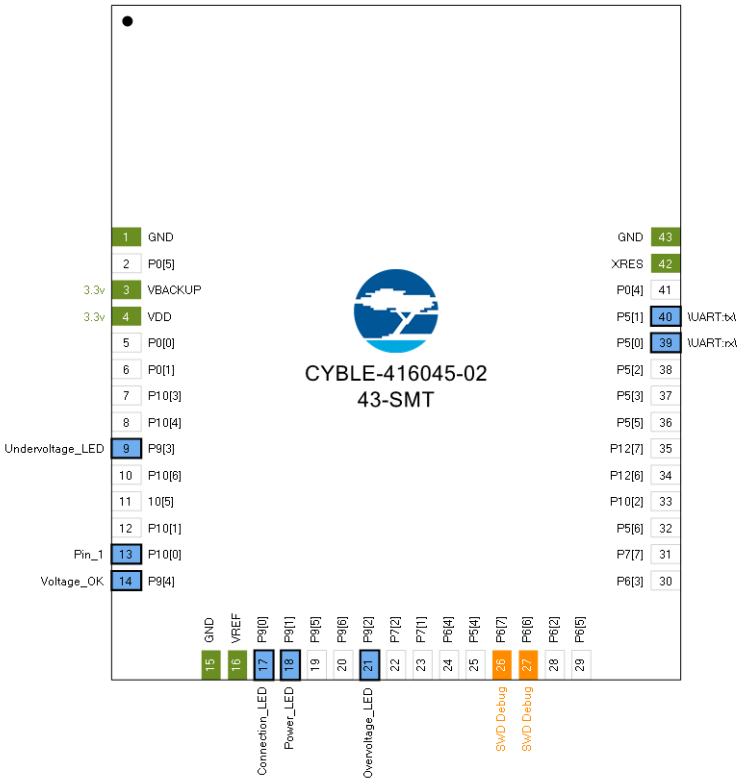
Resource Type	Used	Free	Max	% Used
Digital Clocks	1	7	8	12.50 %
Crypto Accelerator	0	1	1	0.00 %
Interrupts [CM0+]	6	26	32	18.75 %
Interrupts [CM4]	4	143	147	2.72 %
IO	10	26	36	27.78 %
Interprocessor Communication	0	16	16	0.00 %
MCWDT	0	2	2	0.00 %
CapSense	0	1	1	0.00 %
Energy Profiler	0	1	1	0.00 %
Real Time Clock	0	1	1	0.00 %
Bluetooth Low Energy	1	0	1	100.00 %
I2S	0	1	1	0.00 %
PDM/PCM	0	1	1	0.00 %
SCB	1	8	9	11.11 %
Serial Memory Interface	0	1	1	0.00 %
DMA Channels	0	32	32	0.00 %
LCD	0	1	1	0.00 %
SmartIO	0	2	2	0.00 %
TCPWM	0	32	32	0.00 %
UDB				
Macrocells	1	95	96	1.04 %
Unique P-terms	0	192	192	0.00 %
Total P-terms	0			
Datapath Cells	0	12	12	0.00 %
Status Cells	0	12	12	0.00 %
Control Cells	0	12	12	0.00 %
7-Bit IDAC	0	2	2	0.00 %
Continuous Time DAC	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
Opamp	0	2	2	0.00 %
Sample and Hold	0	1	1	0.00 %
SAR ADC	1	0	1	100.00 %

Resource Type	Used	Free	Max	% Used
DieTemp Sensor	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
6	GND	GND	Power, Dedicated	
15	P10[6]	GPIO [unused]		
16	10[5]	GPIO [unused]		
17	P10[1]	GPIO [unused]		
18	P10[0]	Pin_1	Analog	HiZ analog
19	P9[4]	Voltage_OK	Software In/Out	Strong drive
20	GND	GND	Power, Dedicated	
21	VREF	VREF	Dedicated	
22	P9[0]	Connection_LED	Software In/Out	Strong drive
23	P9[1]	Power_LED	Software In/Out	Strong drive
24	P9[5]	GPIO [unused]		
7	P0[5]	GPIO [unused]		
25	P9[6]	GPIO [unused]		
26	P9[2]	Overvoltage_LED	Software In/Out	Strong drive
27	P7[2]	GPIO [unused]		
28	P7[1]	GPIO [unused]		
29	P6[4]	GPIO [unused]		
30	P5[4]	GPIO [unused]		
31	P6[7]	GPIO [unused]	Dgtl In	Res pull down
32	P6[6]	GPIO [unused]	Dgtl In	Res pull up
33	P6[2]	GPIO [unused]		
34	P6[5]	GPIO [unused]		
8	VBACKUP	VBACKUP	Power	
35	P6[3]	GPIO [unused]		
36	P7[7]	GPIO [unused]		
37	P5[6]	GPIO [unused]		
38	P10[2]	GPIO [unused]		
39	P12[6]	GPIO [unused]		
40	P12[7]	GPIO [unused]		
41	P5[5]	GPIO [unused]		
42	P5[3]	GPIO [unused]		
43	P5[2]	GPIO [unused]		
44	P5[0]	\UART:rx\	Dgtl In	HiZ analog
9	VDD	VDD	Power	
45	P5[1]	\UART:tx\	Dgtl Out	Strong drive
46	P0[4]	GPIO [unused]		
47	XRES	XRES	Dedicated	
48	GND	GND	Power, Dedicated	

Pin	Port	Name	Type	Drive Mode
10	P0[0]	GPIO [unused]		
11	P0[1]	GPIO [unused]		
12	P10[3]	GPIO [unused]		
13	P10[4]	GPIO [unused]		
14	P9[3]	Undervoltage_LED	Software In/Out	Strong drive

Abbreviations used in Table 3 have the following meanings:

- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- Res pull down = Resistive pull down
- Res pull up = Resistive pull up
- Dgtl Out = Digital Output

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
10[5]	16	GPIO [unused]		
P0[0]	10	GPIO [unused]		
P0[1]	11	GPIO [unused]		
P0[4]	46	GPIO [unused]		
P0[5]	7	GPIO [unused]		
P10[0]	18	Pin_1	Analog	HiZ analog
P10[1]	17	GPIO [unused]		
P10[2]	38	GPIO [unused]		
P10[3]	12	GPIO [unused]		
P10[4]	13	GPIO [unused]		
P10[6]	15	GPIO [unused]		
P12[6]	39	GPIO [unused]		
P12[7]	40	GPIO [unused]		
P5[0]	44	\UART:rx\	Dgtl In	HiZ analog
P5[1]	45	\UART:tx\	Dgtl Out	Strong drive
P5[2]	43	GPIO [unused]		
P5[3]	42	GPIO [unused]		
P5[4]	30	GPIO [unused]		
P5[5]	41	GPIO [unused]		
P5[6]	37	GPIO [unused]		
P6[2]	33	GPIO [unused]		
P6[3]	35	GPIO [unused]		
P6[4]	29	GPIO [unused]		
P6[5]	34	GPIO [unused]		
P6[6]	32	GPIO [unused]	Dgtl In	Res pull up
P6[7]	31	GPIO [unused]	Dgtl In	Res pull down
P7[1]	28	GPIO [unused]		
P7[2]	27	GPIO [unused]		
P7[7]	36	GPIO [unused]		
P9[0]	22	Connection_LED	Software In/Out	Strong drive
P9[1]	23	Power_LED	Software In/Out	Strong drive
P9[2]	26	Overvoltage_LED	Software In/Out	Strong drive
P9[3]	14	Undervoltage_LED	Software In/Out	Strong drive
P9[4]	19	Voltage_OK	Software In/Out	Strong drive
P9[5]	24	GPIO [unused]		
P9[6]	25	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- Dgtl Out = Digital Output

- Res pull up = Resistive pull up
- Res pull down = Resistive pull down

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\UART:rx\	P5[0]	Dgtl In
\UART:tx\	P5[1]	Dgtl Out
Connection_LED	P9[0]	Software In/Out
GPIO [unused]	P10[2]	
GPIO [unused]	P5[6]	
GPIO [unused]	P7[7]	
GPIO [unused]	P6[2]	
GPIO [unused]	P6[6]	Dgtl In
GPIO [unused]	P6[3]	
GPIO [unused]	P0[0]	
GPIO [unused]	P5[2]	
GPIO [unused]	P0[4]	
GPIO [unused]	P6[5]	
GPIO [unused]	P5[3]	
GPIO [unused]	P12[6]	
GPIO [unused]	P12[7]	
GPIO [unused]	P5[5]	
GPIO [unused]	P0[1]	
GPIO [unused]	P10[3]	
GPIO [unused]	P0[5]	
GPIO [unused]	P9[5]	
GPIO [unused]	10[5]	
GPIO [unused]	P10[6]	
GPIO [unused]	P10[4]	
GPIO [unused]	P10[1]	
GPIO [unused]	P6[7]	Dgtl In
GPIO [unused]	P6[4]	
GPIO [unused]	P5[4]	
GPIO [unused]	P7[1]	
GPIO [unused]	P9[6]	
GPIO [unused]	P7[2]	
Overvoltage_LED	P9[2]	Software In/Out
Pin_1	P10[0]	Analog
Power_LED	P9[1]	Software In/Out
Undervoltage_LED	P9[3]	Software In/Out
Voltage_OK	P9[4]	Software In/Out

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Embedded Trace (ETM)	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

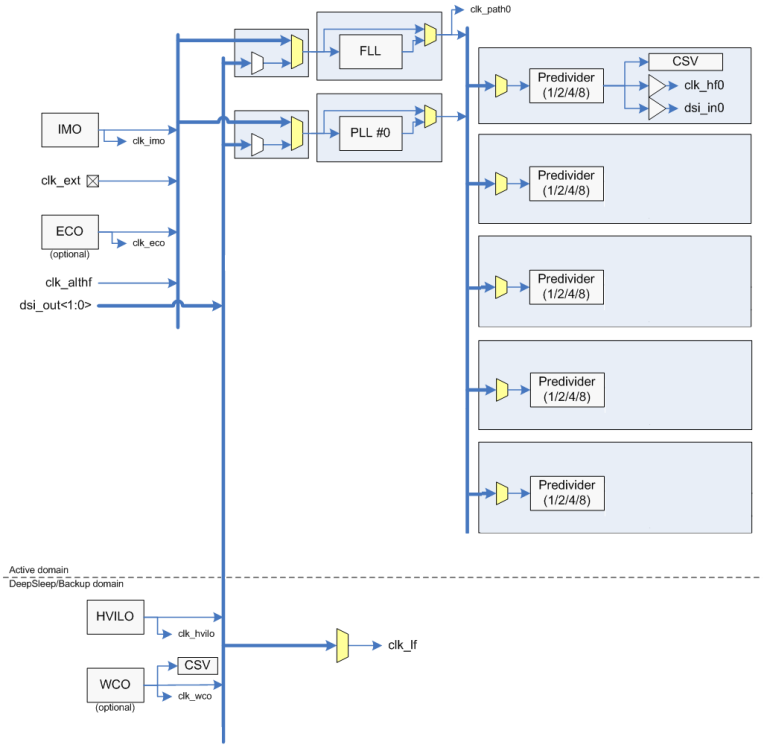
Name	Value
Power Mode	1.1V LDO Linear Regulator
External PMIC Output	Disabled
vBackup Source	VDDD
VBACKUP (V)	3.3
VDD (V)	3.3
Variable VDDA	False

4 Clocks

The clock system includes these clock resources:

- Multiple internal clock sources:
  - 8 MHz Internal Main Oscillator (IMO) ±1%
  - 32 kHz Internal Low Speed Oscillator (ILO) ±30% output
  - 32.768 kHz Precision Internal Low Speed Oscillator (PILO) ±2% output
- Internal FLL and PLL can be used to increase frequency generated by HF clock sources
- Source clocks, FLL, and PLL can be used to drive 5 separate HF clocks
- HFCLK0 can be used to drive peripherals and UDBs
- LFCLK is typically used for DeepSleep wakeup timer

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clk_HF0	NONE	FLL	100 MHz	100 MHz	±2.4	True	True
FLL	NONE	PathMux0	100 MHz	100 MHz	±2.4	True	True
Clk_Fast	NONE	Clk_HF0	100 MHz	100 MHz	±2.4	True	True
Clk_Slow	NONE	Clk_Peri	50 MHz	50 MHz	±2.4	True	True
Clk_Peri	NONE	Clk_HF0	50 MHz	50 MHz	±2.4	True	True
Clk_Pump	NONE	FLL	25 MHz	25 MHz	±2.4	True	True
PathMux4	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_Timer	NONE	IMO	8 MHz	8 MHz	±1	True	True
IMO	NONE		8 MHz	8 MHz	±1	True	True
PathMux3	NONE	IMO	8 MHz	8 MHz	±1	True	True
AltHF	NONE		8 MHz	8 MHz	±0	False	True
PathMux0	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux2	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux1	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_LF	NONE	PILO	32.768 kHz	32.768 kHz	±2	True	True
PILO	NONE		32.768 kHz	32.768 kHz	±2	False	True
Clk_Bak	NONE	Clk_LF	32.768 kHz	32.768 kHz	±2	True	True
Clk_AltSysTick	NONE	Clk_LF	32.768 kHz	32.768 kHz	±2	True	True
ILO	NONE		32 kHz	32 kHz	±10	True	True
ExtClk	NONE		24 MHz	? MHz	±0	False	False
Clk_HF1	NONE	FLL	? MHz	? MHz	±0	False	False
WCO	NONE		32.768 kHz	? MHz	±0.015	False	False
Clk_HF2	NONE	FLL	? MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
PLL0	NONE	PathMux1	100 MHz	? MHz	±0	False	False
Clk_HF3	NONE	FLL	? MHz	? MHz	±0	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
Clk_HF4	NONE	FLL	? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

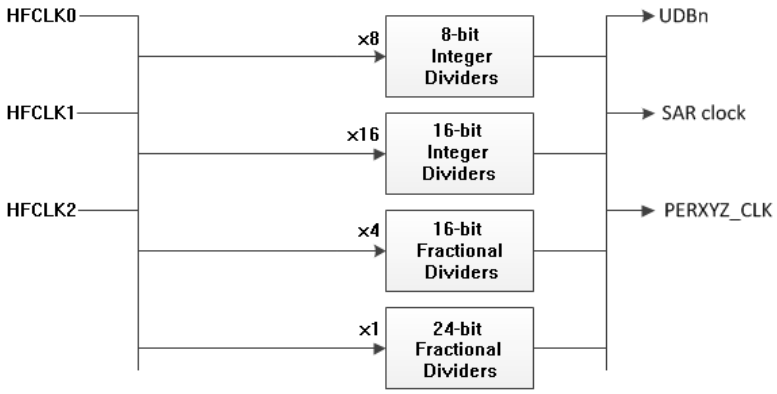


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
UART_SCBCLK	UNKNOWN	Clk_Peri	1.382 MHz	1.389 MHz	±2.4	True	True
ADC_-intSarClock	UNKNOWN	Clk_Peri	1 MHz	1 MHz	±2.4	True	True
Clock_1	UNKNOWN	Clk_Peri	4.32 kHz	4.32 kHz	±2.4	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 6 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	CortexM0p Vector	CortexM0p Priority	CortexM4 Vector	CortexM4 Priority	Deep Sleep Wakeup Capable
BLE_1_bless_isr	24	3	3			CortexM0p
UART_SCB_IRQ	46			46	7	No
ADC_INT	122			122	7	No
SCAN_INT	123			123	7	No
ADC_IRQ	138			138	7	No

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 6 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 6 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

This design has no flash protection specified; all blocks are unprotected.

For more information on Flash memory and protection, please refer to:

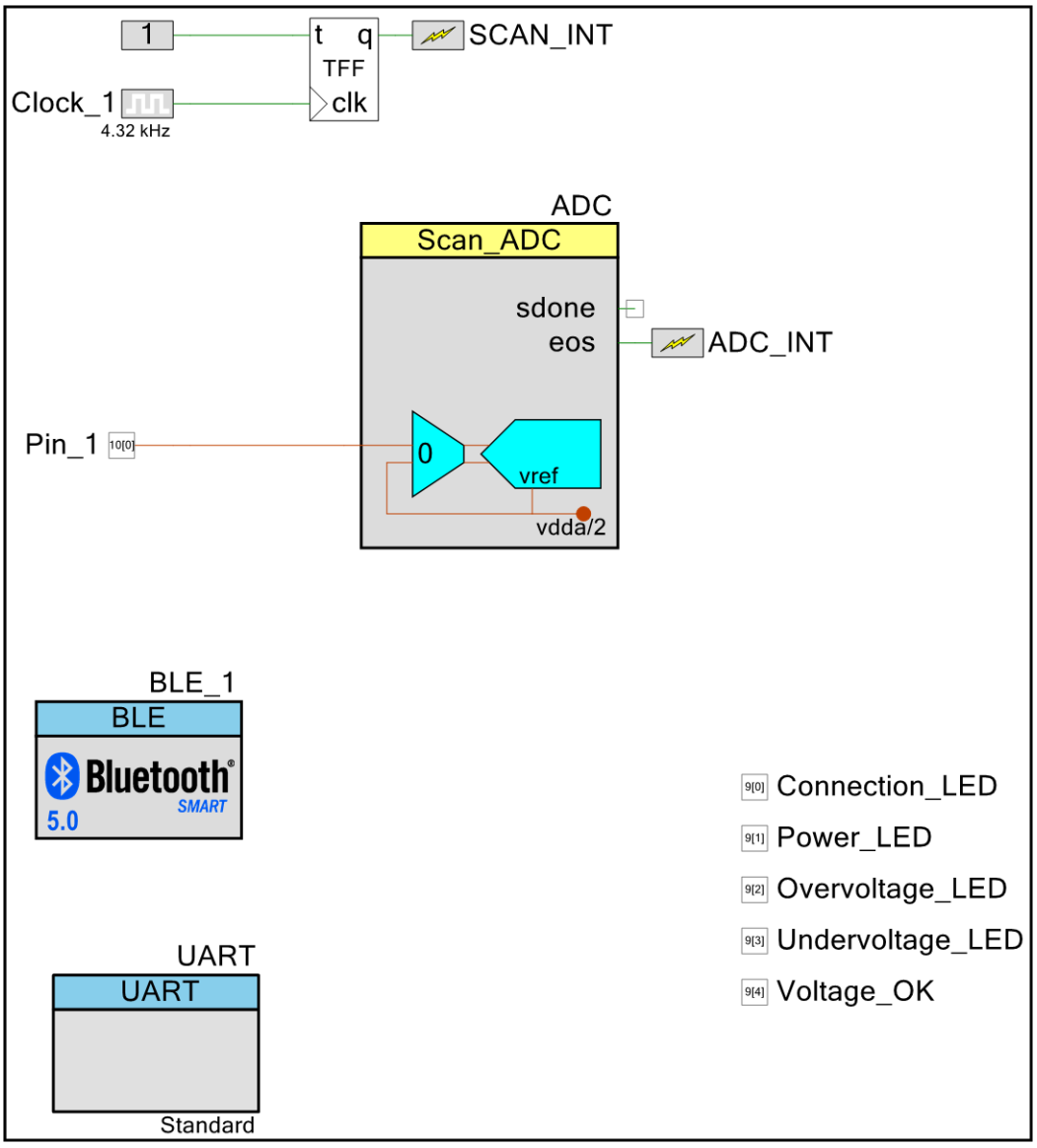
- Flash Protection chapter in the PSoC 6 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance ADC (type: Scan_ADC_v2_10)
- Instance BLE_1 (type: BLE_PDL_v2_0)
- Instance cy_tff_1 (type: cy_tff_v1_0)
- Instance UART (type: SCB_UART_PDL_v2_0)

8 Components

8.1 Component type: BLE_PDL [v2.0]

8.1.1 Instance BLE_1

Description: Bluetooth Low Energy (BLE)
Instance type: BLE_PDL [v2.0]
Datasheet: online component datasheet for BLE_PDL

Table 12. Component Parameters for BLE_1

Parameter Name	Value	Description
AddQdepthPerConn	0	Additional stack queue depth per connection for better throughput. Default queue is defined by CYBLE_L2CAP_-STACK_Q_DEPTH_PER_-CONN macro.
AutopopulateWhitelist	true	Provides an option to link the whitelist to the bonded device list.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
ConnectionCount	1	The number of BLE connections / links.
Enable LE 2 Mbps	false	Enable LE 2 Mbps feature.
Enable Link Layer Privacy	true	Enables LL Privacy 1.2 feature of Bluetooth 4.2.
EnableExternalLnaRxOutput	false	When selected, ext_lna_rx_ctl_-out signal from the BLE radio is routed on a GPIO.
EnableExternalPaLnaOutput	false	Enables external PA and LNA chip enable control pins and automatically enables routing the BLESS Tx and Rx enable signals on the dedicated GPIO lines.
EnableExternalPaTxOutput	false	When selected, ext_pa_tx_ctl_-out signal from the BLE radio is routed on a GPIO.
EnableExternalPrepWriteBuff	false	Enables application to provide dynamically allocated buffer for prepare write request. The buffer should be allocated and provided after CYBLE_EVT_-MEMORY_REQUEST event from stack.
EnableL2capLogicalChannels	true	Enables L2CAP logical channels support.
HalBaudRate	115200	UART baud rate
HalCtsEnable	true	In the HCI mode, the parameter enables the cts output in the UART.

Parameter Name	Value	Description
HalCtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output cts signal of the UART.
HalOversampling	13	UART oversampling
HalRtsEnable	true	In the HCI mode, the parameter enables the rts output in the UART.
HalRtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output rts signal of the UART.
HalRtsTriggerLevel	120	In the HCI mode, the parameter specifies the number of entries in the RX FIFO to activate the rts output signal of the UART.
HciContrCore	CortexM0p	Defines the core for the Controler in HCI mode.
HostCore	CortexM0p	Defines the core for the Host. For DUAL core device Controller will be compiled for different core.
ImportFilePath		The path to the file shared by another BLE component instance.
KeypressNotifications	false	Provides an option for a keyboard-only device during the LE secure pairing process to send key press notifications when the user enters or deletes a key.
L2capMpsSize	23	The maximum size of payload data that the L2CAP layer is capable of accepting.
L2capMtuSize	23	The maximum SDU size of an L2CAP packet.
L2capNumChannels	1	The number of LE L2CAP connection oriented logical channels required by the application.
L2capNumPsm	1	The number of PSMs required by the application.
Link layer max RX payload size (bytes)	27	The maximum link layer receive payload size to be used in the design.
Link layer max TX payload size (bytes)	27	The maximum link layer transmit payload size to be used in the design.
MaxBondedDevices	16	The maximum number of bonded devices to be supported by this device.
MaxResolvableDevices	16	The maximum number of peer devices whose addresses should be resolved by this device.
MaxWhitelistSize	16	The maximum number of devices that can be added to the whitelist.

Parameter Name	Value	Description
Mode	Profile	Defines the component operating mode.
Radio Power Calibration	false	Enables TX Power Calibration Retention
SharingMode	None	Defines if some parts of code are shared between two BLE components.
StackMode	Release	Determines the internal stack mode. Is used to switch the operation for debugging. Release - Host and Controller on single core with software interface DualIPC - Host and Controller on dual core with IPC interface HostOnly - Host with UART interface HostOnlyIPC - Host with IPC interface DualUart - Host and Controller on dual core with UART interface
StrictPairing	false	Provides an option to use only the selected security features and doesn't fallback to an unsecure connection if the peer device doesn't support the selected security features.
UseDeepSleep	false	Indicates whether deep sleep mode is used.
User Comments		Instance-specific comments.

8.2 Component type: cy_tff [v1.0]

8.2.1 Instance cy_tff_1

Description: Toggle Flip Flop
Instance type: cy_tff [v1.0]
Datasheet: online component datasheet for cy_tff

Table 13. Component Parameters for cy_tff_1

Parameter Name	Value	Description
ArrayWidth	1	Width of t and q terminals. Must be between 1 and 32.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
User Comments		Instance-specific comments.

8.3 Component type: Scan_ADC [v2.10]

8.3.1 Instance ADC

Description: Scanning SAR ADC
Instance type: Scan_ADC [v2.10]
Datasheet: online component datasheet for Scan_ADC

Table 14. Component Parameters for ADC

Parameter Name	Value	Description
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Debug	false	
ExternalClk	false	
ExternalSoc	false	
FilterConfigMuxSelect_0	1	
FilterConfigMuxSelect_1	1	
FilterConfigMuxSelect_2	2	
FilterConfigMuxSelect_3	3	
FilterVinMuxSelect_1_0	0	
FilterVinMuxSelect_2_0	0	
FilterVinMuxSelect_2_1	0	
FilterVinMuxSelect_3_0	0	
FilterVinMuxSelect_3_1	0	
FilterVinMuxSelect_3_2	0	
NumConfigs	1	
Test_ConfigSpacing	15	
Test_ExposeTestTerminals	false	
User Comments		Instance-specific comments.

8.4 Component type: SCB_UART_PDL [v2.0]

8.4.1 Instance UART

Description: UART (SCB) communications interface
Instance type: SCB_UART_PDL [v2.0]
Datasheet: online component datasheet for SCB_UART_PDL

Table 15. Component Parameters for UART

Parameter Name	Value	Description
Baud Rate (bps)	115200	This parameter specifies the baud rate in bps. The actual baud rate may differ based on the available clock frequency and Component settings. Range: 1 - 1000000 bps.
Bit Order	LSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Break Signal Bits	11	This parameter specifies the break width in bits. The range: 7-16.
Com Mode	Standard	This parameter defines the sub-mode of UART as: Standard, SmartCard or IrDA.

Parameter Name	Value	Description
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
CTS	false	This parameter enables the cts input.
Data Width	8 bits	This option defines the width of a single data element in bits. The range: 4-9.
Drop on Frame Error	false	This parameter determines if the data is dropped from the RX FIFO on a frame error event.
Enable Clock from Terminal	false	This parameter allows choosing between an internally configured clock (by the component) or an externally configured clock (by the user) for the component operation.
Enable Digital Filter	false	This parameter applies a digital 3-tap median filter to the UART input lines.
Interrupt	Internal	This parameter allows choosing between Internal and External placement of the Interrupt Component.
Oversample	12	This parameter defines how many Component clocks oversample the selected baud rate. The range: 8 - 16 (except IrDA mode). The oversample values are predefined for IrDA mode.
Parity	None	This parameter defines the functionality of the parity bit location in the transfer as None, Odd or Even.
RTS	false	This parameter enables the rts output.
RX Output	false	This parameter enables the RX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
Show UART Terminals	false	This parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Stop Bits	1	This parameter defines the number of stop bits.
TX Output	false	This parameter enables the TX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
TX/RX Mode	TX + RX	This parameter enables the receiver or transmitter functionality or both simultaneously.

Parameter Name	Value	Description
TX-Enable	false	This parameter enables TX_EN output.
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 6 register map is covered in the PSoC 6 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 6 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 6 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines