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ROUTER 1X3 -RTL DESIGNING USING VERILOG

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ABSTRACT

Routing is the process of transporting a packet of data from a source to a destination, allowing messages to flow from one computer to another until they reach their goal. A router is a networking device that sends data packets from one computer network to another. In contrast to a network switch, which joins data lines from a single network, it is connected to two or more data lines from distinct networks. This paper focuses on the router device, its top-level architecture, and how several sub-modules of the router, such as Register, FIFO, FSM, and Synchronizer, are synthesised, simulated, and finally coupled to the top module. A million transistors can be integrated on a single chip with System on Chip.

Keywords: Routing, Router, Data Packets, Verilog, Xilinx I$E, Questasim.

I. INTRODUCTION

In addition to forwarding and transmitting data packets between computer networks, a router is a networking equipment. In contrast to a network switch, which links data lines from one network to several networks, a router connects two or more data lines from one network to many networks. The router checks and verifies the address information in the data packet to send and determine its ultimate destination when it comes from one of the lines. It redirects the packet to the next network on its path if it uses information from its own routing table or routing policy. An overlay internetwork is created by these types of packets. Routers serve numerous roles on the Internet, including "traffic redirection."

II. BACKGROUND THEORY

In 1963, General Microelectronics released the first commercial MOS integrated circuit. MOS integrated ckt technology allowed the integration of more than 10,000 transistors in a single chip in the early 1980s. In the 1970s and 1980s, this cleared the way for VLSI, which began with 10,000 MOS transistors on a single chip and grew to hundreds of thousands, millions, and now many . Each of the original semiconductor chips had two transistors. As a result of the addition of more transistors, more separate functions or systems were integrated over time. The initial integrated circuit (IC) contained only a few devices, as many as ten diodes, transistors, resistors, and capacitors, allowing one or more logic gates to be created on a single device.

III. OBJECTIVE

Routing Packets – Sending and Receiving Packets, The packet is routed and forwarded from the input port to any one of the output ports based on the destination network packet's ip address.

Parity Checking is an error-detection technique that checks the integrity of digital data sent between server and client device networks. This technique ensures that data sent by the server network device is received by the client network device in a non-corrupted state. It is an active low synchronous ip that resets the router when certain operations are performed. The router FIFOs are empty under test conditions, and the valid output signals are low, suggesting that no valid packets are identified on the output data bus.

IV. METHODOLOGY

4.1 Existing methodology

High power 1x3 router Switches and routers are the only critical building blocks of a successful network and infrastructure to route the data in the network if it is consuming the very high power because of using the switches & bridges in between the multiple devices. This High power 1x3 router doesn't use any clocking gate because it is increasing the dynamic power dissipation.

4.2 Proposed methodology

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A router is a simple device that sends data packets from one location to another through a network. It is connected to at least two networks, typically two LANs or WANs, or a LAN and its ISP's network, and is positioned at gateways, which are points where two or more networks joined. It's a layer 3 OSI routing device. It forwards an incoming packet to an output network based on the ip address fields contained in the packet header and its length.

V. IMPLEMENTATION

5.1 Top level architecture description

Clock: Active high clocking event

Pkt_Valid:pkt_valid is an active high input signal that detects an arrival of a new packet from a sourc network

Resetn: Active low synchronous reset

Data_in:8 bit input data bus that transmits the packet from source network to router

Read_enb_0: Active high input signal for reading the packet through output data bus data_out_0

Read_enb_1: Active high input signal for reading the packet through output data bus data_out_1

Read_enb_2: Active high input signal for reading the packet through output data bus data_out_2

Data_out_0: 8 bit output data bus that transmits the packet from the router to destination clent network 1

Data_out_1: 8 bit output data bus that transmits the packet from the router to destination clent network 2

Data_out_2: 8 bit output data bus that transmits the packet from the router to destination clent network 3

Vld_out_0: Active high signal that detects that a valid byte is available for destination client network1

Vld_out_1: Active high signal that detects that a valid byte is available for destination client network2

Vld_out_2: Active high signal that detects that a valid byte is available for destination client network3

Busy: Active high signal that detects a busy state for the router that stops accepting any new byte

Err: Active high signal that detects the mismatch between packet parity and internal parity

Router top-sub-blocks:

- 3 FIFOs
- Synchronizer
- Register
- Fine state Machine

5.2 Router:FIFO

In the router's design, three FIFOs are used. Each FIFO has a width of 9 bits and a depth of 16 bits. The FIFO is reset with a synchronizer active low reset value and runs on the system clock. Soft reset, an internally reset signal, also resets the FIFO. Soft reset is an active high signal created by the SYNCHRONIZER block when the ROUTER is in the time out state. Full=0, empty=1 and data out=0 if resetn is low.The size of the FIFO memory is 16X9. In order to detect the packet's header byte, an additional bit is appended to the data width. The header byte of a packet is detected by Lfd state. The 9th bit is set to 1 for the header byte and 0 for the rest of the bytes.

Write Operation:

When write enb is high, signal data in is sampled at the rising edge of the edge of the clock. Write operations are only performed when the FIFO is not full to avoid an over running condition.

Read operation:

When read enb is set to high, data is read from data out on the rising edge of the clock. In order to avoid underrunning conditions, read operations are only performed when the FIFO is not empty.

5.3 Router:Synchronizer

Synchronization between router FSM and router FIFO modules is provided by this module. It ensures that the one input port and three output ports are in constant communication. The detect add and data in signals are used to choose a FIFO until the packet routing for that FIFO is complete. The signal fifo full is asserted when the full status of fifo 0, FIFO 1, or FIFO 2 is true.

fifo _full=full_ 0 if data in =2'b00

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If data in=2b01, fifo_ full=full_ 1 is the result.

Fifo _full=full _2 if data in=2b10, otherwise fifo _full=0.

The vld out x signal is created dependent on the FIFO's empty status, as seen below:

- vld _out_ 0=empty_ 0, vld _ out_1=empty _1, vld _out _2=empty_ 2
- The write enb register signal is used to create the write enb signal for the selected FIFO's write operation.
- For each FIFO, there are three internal reset signals (soft reset 0, soft reset 1, and soft reset 2). If read enb X (read enb 0,read out 1,read out 2) is not asserted within 30 clocks per cycles of vld out X(vld out 0,vld out 1 or vld out 2) being asserted, the relevant internal reset signals go high.

5.4 Router:Register

A header byte, FIFO full state byte, internal parity, and packet parity byte are all stored in this module's internal registers. The rising edge of the clock latches all of the registers in this module. The signals (dout,err,parity done, and low pkt valid) are all low if resetn is low.

Under the following conditions, the signal parity done is high:

- When the ld state signal is high and the [fifo full and pkt valid] signals are low.
- The previous value of parity done is low when the signals laf state and low pkt valid are both high.
- The low pkt valid signal is reset using the rst int reg signal.
- The parity done signal is reset using the detect add signal.

➢ When ld state is high and pkt valid is low, the signal low pkt valid is high. Low packet valid indicates that pkt valid has been deasserted for the current condition.

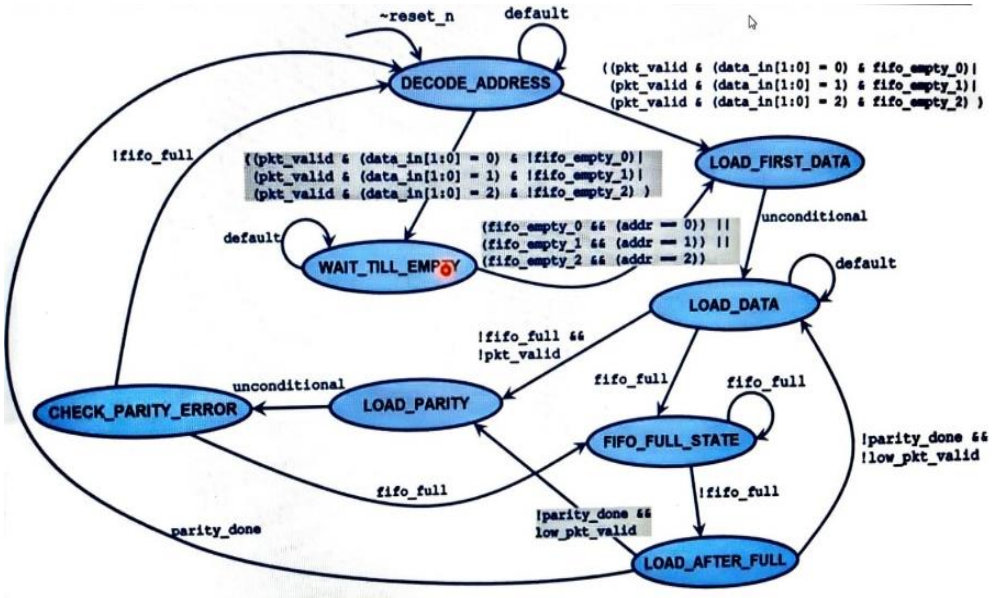
➢ When the detect add and pkt valid signals are high, the first data byte, or header, is latched inside an internal register. When lfd state is high, this data is (latched to the output dout.)

- If the ld state signal is high & the fiifo full signal is low then the payload is latched to dout.
- When ld state and! fifo full are high, the signal +data in is latched to an internal register.
- When laf state goes high, this data is latched to output dout. Internal parity is calculated using Full state

➢ Internal parity is stored in another internal regiser for parity matching. The bit-wise xor operation between the header byte, payload byte, and prior parity values is used to determine internal parity, as demonstrated below:

parity_reg=parity_ reg_ previou^sheader byte-t1cycle
parity_ reg=parity_ reg_ previous^payload byte1-t2cycle
parity_ reg=parity_ reg_ previous^payload byte2-t3 cycle
The last byte of the payload is Only after the packet parity is loaded is the err calculated, and it gets high if the packet parity does not match the internal parity.

5.5 Router:FSM



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VI. TEST RESULTS

The Verilog code for all the modules is written and instantiated in the top module and simulation is done using the modelsim and different packet lengths of size 14 and 16 are observed in waveforms and it is synthesized using xillinx vivado software and the rtl schematic is obtained.

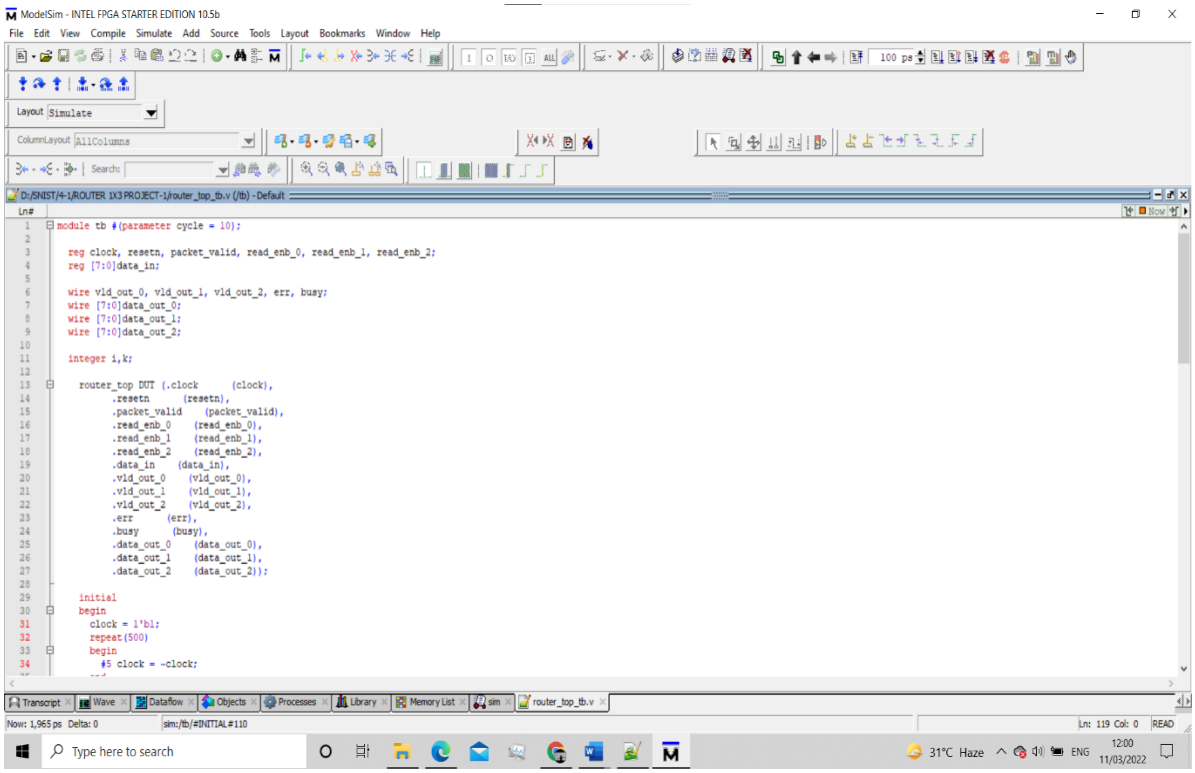

Figure: Running the program

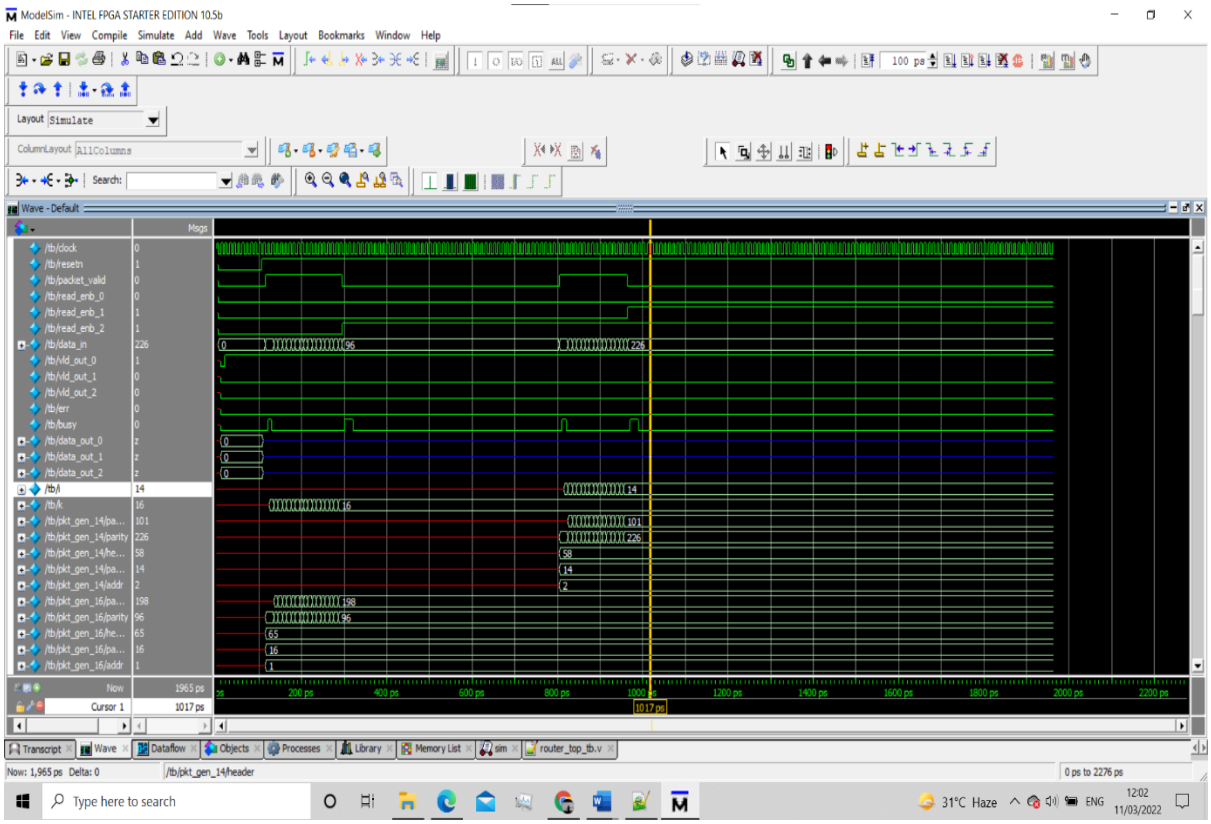

Figure: Simulated output

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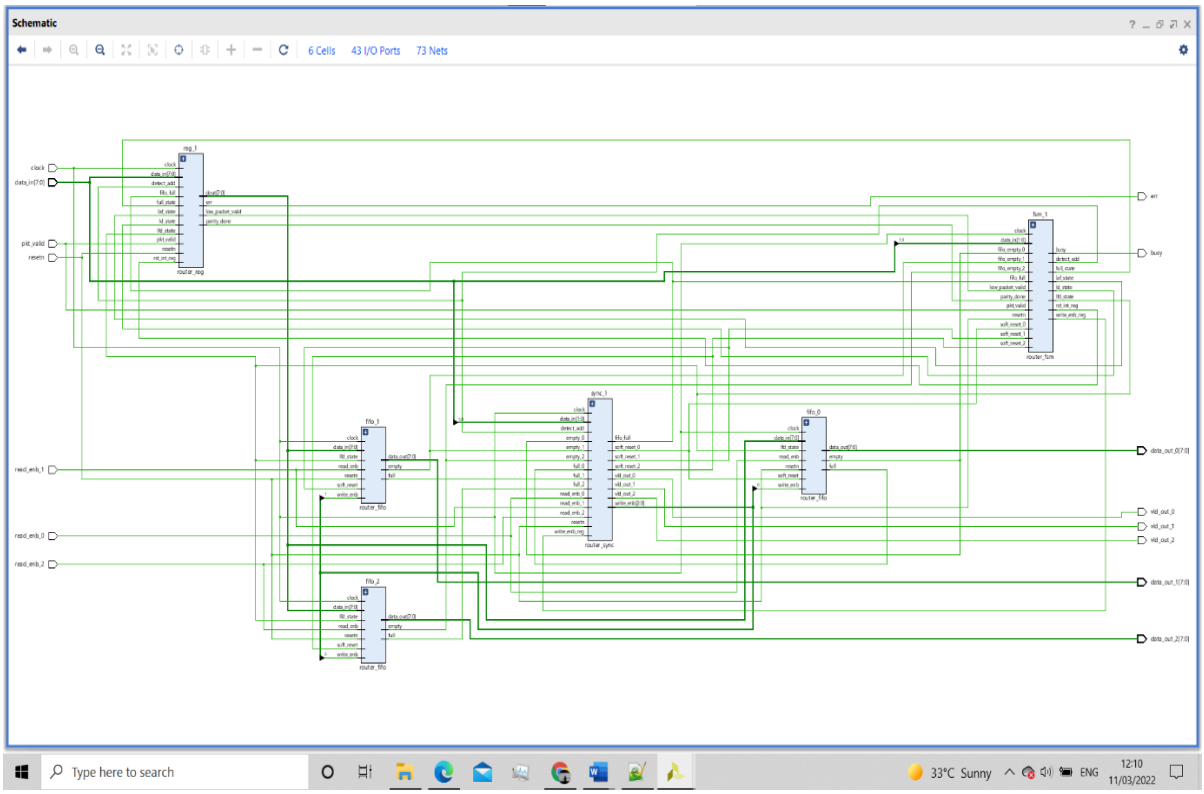

Figure: Synthesized rtl schematic

VII. CONCLUSION

The Router1X3 is a successfully designed by using the verilog hardware description language . During the simulation in the modelsim and synthesis in the Xillinx vivado software, many coding flaws ,errors and warnings are discovered and rectified .Packets with a long & different payload length like below examples of scenarios as 14 bytes packet length,16 bytes packet length are generated and Full FIFO state i.e (observing busy signal) & which is a good packet packet and observed read a read/write operation are happening at the same time ,different bad packets or a packet that has been corrupted were derived from the testbench in order to assess the design's reliability. And according to Questasim's coverage report, it was working flawlessly, with 100% FSM state coverage, 80.81 percent FSM transition coverage, 95.2 percent toggle coverage, and 91.31 percent statement coverage. It is proved that the router 1x3 is designed very efficiently with lower constant by using the available resources.

VIII. REFERENCES

[1] M. Pirretti, G. M. Link, R. R. Brooks, N. Vijaykrishnan, M. Kandemir, and M. J. Irwin, "F@ult tolerant algorithms$ for network-on-chip interconnect," Proceedin$. IEEE Computer society Annual Symposium on VLSI, pp.46-51, Feb. 2004.

[2] Salminen, E., Kulmala, A., & Hamalainen, T. D. (2008).

[3] Cota, É., de Morais Amory, A., & Lubaszew$ki, M. S. (2012). NoC Basics. In Reliability, Availability and Serviceability of Networks-on-Chip (pp. 11-24). $pringer US.

[4] Swapna, S., Swain, A. K., & Mahapatra, K. K. (2012, December). Design and analysis of f5 port router for network on chip. In Microelectronics and Electronics (PrimeA$ia), 2012 Asia Pacific Conference on Postgraduate Re$earch in (pp. 51-55). IEEE.

[5] Choudhari, E. M., & Dakhole, P. K. (2014, April). Design and verification of five port router for network on chip. In Communications and Signal Processing (ICCSP), 2014 International Conference on (pp. 607-611). IEEE [6] Gopal N., Router 1x3 RTL Design Journal of Engineering.