CHANDRA PRAKASH S

chandraprakashs2003@gmail.com | LinkedIn | GitHub | Medium

PROFESSIONAL EXPERIENCE

Freelance Digital designer Jan,2023 - Present

Small scale project development.

- Designed and verified a streamlined **Single stage RISC** processor architecture using Verilog, resulting in 15% reduction in critical path.
- Design a range of **communication protocols** and **Arduino** based projects as a small-scale project for college level project displays. The project's success contributed to a 10% increase in the overall evaluation scores.

Research Intern - IIT Palakkad Mar,2023 - Aug,2023

Research based on Hardware Security.

- Spearheaded revolutionary methodologies for the **detection and elimination of hardware-based malware** within the **Network on Chip (NoC)** infrastructure, resulting in an 25% reduction in security vulnerabilities.
- Expertly assimilated these pioneering techniques into the industry-leading **Xilinx Vivado** platform, thereby **reinforcing digital ecosystems and bolstering network resilience.**

EDUCATION

Maven Silicon Jul,2023 - Present

Advanced VLSI Design and Verification.

Relevant Coursework: FPGA, CMOS, RISC-V, RTL & SoC design verification.

PSG Institute of Technology and Applied Research Aug,2021 - Apr,2024

Bachelors, Electronics and Communication Engineering. CGPA: 8.02

Relevant Coursework: Digital Design, Computer Architecture, VLSI design.

PROJECTS

MIPS Processor Verification Personal | Oct,2023-Nov,2023

- Led the comprehensive **verification of MIPS processor** by applying **Universal Verification Methodology**, validating and ensuring the integrity of processor designs, resulting in a 20% reduction in bug density and a 15% improvement in overall verification efficiency.
- Implemented advanced **UVM techniques** to scrutinize critical facets of the MIPS architecture, This effort directly led to a 10% reduction in post-release defects.
- **Software used:** Xilinx Vivado 2023, Icarus.

1x3 Router Design Academic | Sep, 2023

- Executed the **design and implementation** of a high-performance 1x3 router project in **Verilog.** Also optimized **data routing and distribution** within intricate systems, resulting in an uninterrupted data flow and a 20% reduction in latency compared to prior designs, leading to a substantial enhancement in overall system efficiency.
- **Hardware used:** Zedboard Zynq 7000.
- **Software used:** Modelsim 18.1, Quartus prime.

Drowsiness detection system Academic | Apr, 2023-May, 2023

- Championed the deployment of cutting-edge **computer vision algorithms** to maintain vigilant monitoring of driver behavior. Our innovative approach has not only revolutionized road safety but has also driven a **remarkable 75% reduction** in the incidence of accidents.
- Implementation of this technology not only provides **real-time alerts** to drivers, preventing potential accidents arising from **fatigue-related impairment**, but also fosters a culture of safer driving practices, thereby transforming the way we navigate our roads.
- **Tech stack used:** Python, IBM Watson IoT, Node-RED.

TECHNICAL SKILLS

Verilog	C	System Verilog	Perl	Python	VHDL
SVA	STA	UVM	DFT	TCL	Linux
AXI	APB	AMBA	PCIe	DDR	UART

PUBLICATION

Co-authored a book chapter on **Low power CMOS circuits for Enhanced Performance** for the book **Low power designs in Nanodevices and circuits for Emerging Application** published by **CRC Taylor & Francis**. Aug,2022-Mar,2023

ACCOMPLISHMENTS

- Conducted and organized a Workshop on **Embedded systems using Arduino** for **Yuktaha 2023** (National level Symposium) for about 80+ participants and Served as the **Executive member** for **ECE association** for the year 21-22.
- **Outstanding student** for 2021 & **Best outgoing student** of the year 2021 award.
- **Best Project award** among the department for 2021.
- **Techfest-2020 |** CIT Sandwich Polytechnic College.
  - **Winner - Circuit Debugging** among 25 teams.
  - **Winner - Technical Quiz** among 70 students.