National Semiconductor

January 1989

27C16
16,384-Bit (2048 x 8) UV Erasable CMOS PROM Military Qualified

General Description

The 27C16 is a high speed 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The 27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

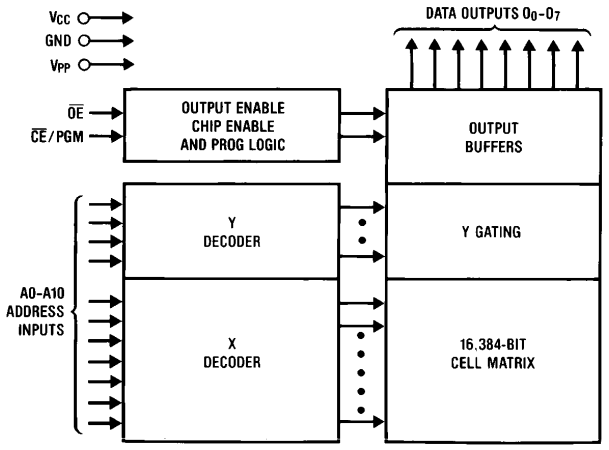
This EPROM is fabricated with the reliable, high volume, time proven, P²CMOS™ silicon gate technology.

The 27C16 specified on this data sheet is fully compliant with MIL-STD-883, Revision C.

Features

- Access time down to 450 ns
- Low CMOS power consumption
  - — Active Power: 26.25 mW max
  - — Standby Power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible to MM2716 and higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output
- Windowed DIP Package
- Specifications guaranteed over full military temperature range (−55°C to +125°C)

Block Diagram



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Pin Names

A0–A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

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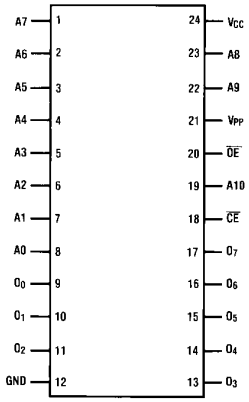
Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

Dual-In-Line Package
27C16Q



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Top View

27C32 2732	27C64 2764	27C128 27128	27256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the 27C16 pins.

Military Temp Range ($-55°C$ to $+125°C$) $V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time (ns)
27C16Q450/883	450
27C16Q550/883	550

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground (Note 11)	V_{CC} +0.3V to GND −0.3V
V_{PP} Supply Voltage with Respect to Ground during Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 Seconds)	300°C

Operating Conditions (Note 9)

Temperature Range (T_{case})	−55°C to +125°C
V_{CC} Power Supply (Notes 2 and 3)	5V ±10%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or V_{IL}			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{IL}, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		2	30	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		1	25	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	4.4			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	27C16				Units
			450		550		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		450		550	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		450		550	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		120		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

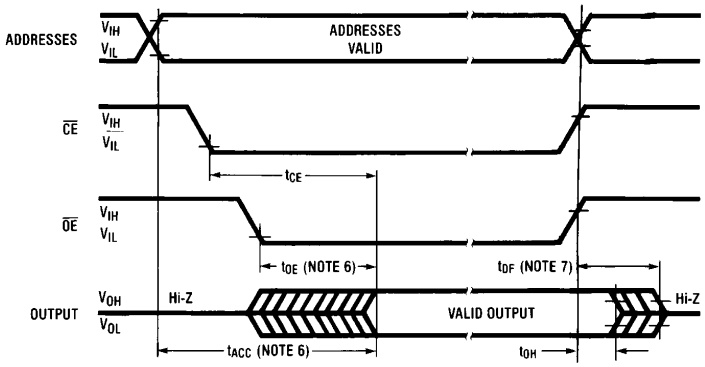
Capacitance $T_A = +25°C$, f = 1 MHz (Note 5)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF	Timing Measurement Reference Level	
Input Rise and Fall Times	$\leq$ 20 ns	Inputs	1V and 2V
Input Pulse Levels	0.8V to 2.2V	Outputs	0.8V and 2V

AC Waveforms (Notes 2, 8, 9, 10)



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Note 1: Stresses above those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} $\leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $- 0.10V$
Low to TRI-STATE, the measured V_{OL1} (DC) $+ 0.10V$

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The 27C16 requires one address transition after initial power-up to reset the outputs.

Note 11: The outputs must be restricted to $V_{CC} + 0.3V$ to avoid latch-up and device damage.

PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 & 3)

(T_A = +25°C ±5°C, V_{CC} = 5V ±10%, V_{PP} = 25V ±1V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	μA
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}$/PGM = V_{IH}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} +1	V

AC Programming Characteristics (Notes 2 & 3)

(T_A = +25°C ±5°C, V_{CC} = 5V ±10%, V_{PP} = 25V ±1V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μS
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$/PGM = V_{IL}	0		120	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM = V_{IL}			100	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

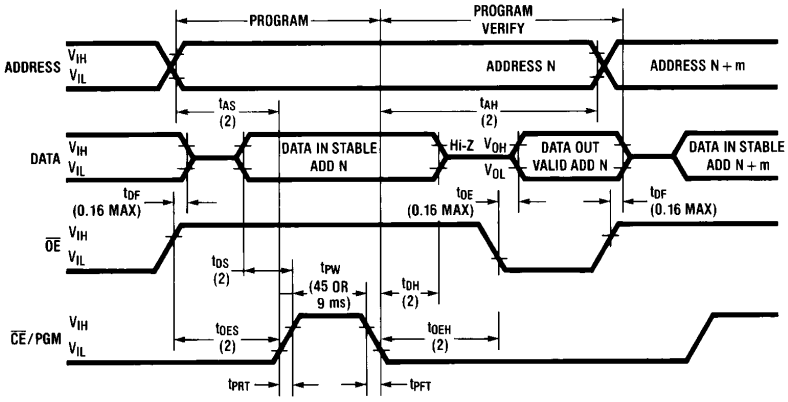
AC Test Conditions

V_{CC}	5V ±10%
V_{PP}	25V ±1V
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V

Timing Measurement Reference Level

Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms V_{PP} = 25V ±11V, V_{CC} = 5V ±5% (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 27C16 must not be inserted into or removed from a board with V_{PP} at 25V ±1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The six modes of operation of the 27C16 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The 27C16 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. The 27C16 requires one address transition after initial power-up to reset the outputs.

Standby Mode

The 27C16 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The 27C16 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because 27C16s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the 27C16.

Initially, and after each erasure, all bits of the 27C16 are in the ''1'' state. Data is introduced by selectively programming ''0s'' into the desired bit locations. Although only ''0s'' will be programmed, both ''1s'' and ''0s'' can be presented in the data word. The only way to change a ''0'' to a ''1'' is by ultraviolet light erasure.

The 27C16 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The 27C16 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Functional Description (Continued)

Programming multiple 27C16s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 27C16s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 27C16s.

Program Inhibit

Programming multiple 27C16s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 27C16s may be common. A TTL level program pulse applied to an 27C16's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 27C16. A low level $\overline{CE}$/PGM input inhibits the other 27C16 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C16 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Opaque labels should be placed over the 27C16 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the 27C16 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 27C16 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The 27C16-550 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

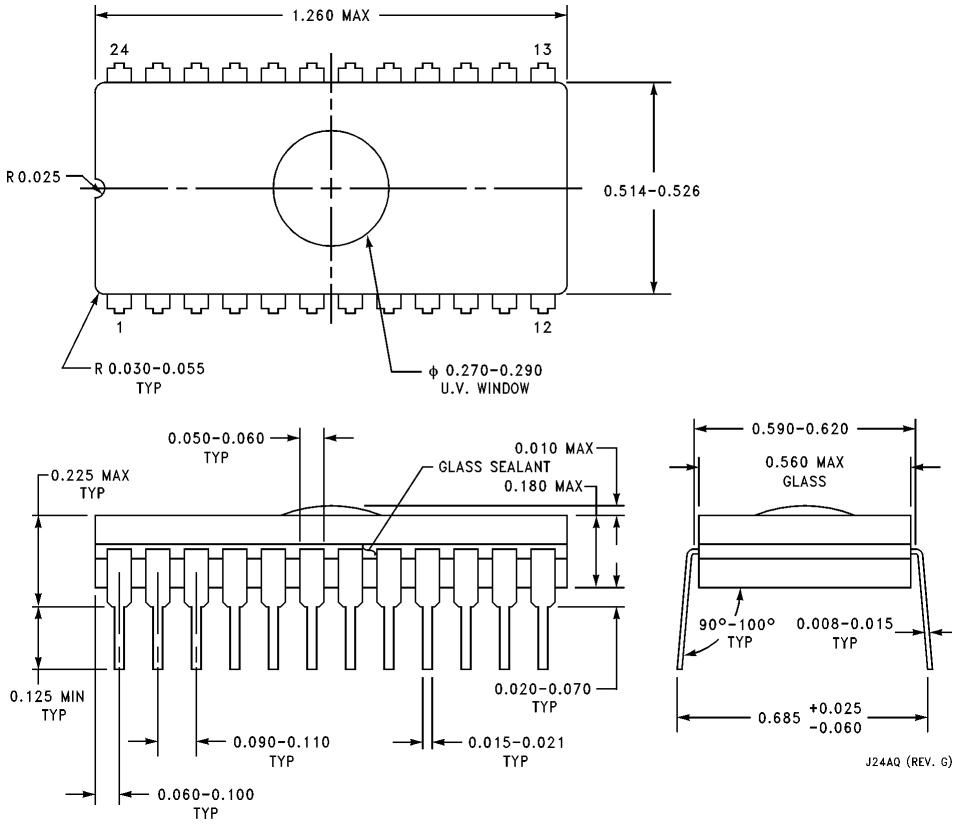
The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Pins Mode	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_P (21)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z
Output Disable	X	V_{IH}	V_{CC}	5	Hi-Z

Physical Dimensions inches (millimeters)

Lit. # 114700



24 Lead Ceramic Dual-In-Line Package (J)
Order Number 27C16Q450/883 or 27C16Q550/883
NS Package Number J24AQ

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