%mul.i.i = shl i64 %5, 8 %cmp288.i = icmp sgt i32 %3, 1, !llvm.access.group !12 %wide.trip.count.i = zext i32 %3 to i64 br i1 %cmp288.i, label %pregion for entry.entry.i.us.preheader, label ... %adi kernel1.exit pregion for entry.entry.i.us.preheader: %scevgep19 = getelementptr float, float\* %2, i64 %wide.trip.count.i %scevgep24 = getelementptr float, float\* %1, i64 %wide.trip.count.i %9 = trunc i64 %5 to i32 %10 = mul i32 %9, %3 %11 = shl i32 %10, 8 %bound0 = icmp ugt float\* %scevgep24, %2 %bound1 = icmp ugt float\* %scevgep19, %1 %found.conflict = and i1 %bound0, %bound1 br label %pregion for entry.entry.i.us pregion for entry.entry.i.us:  $\%_{local_{id_{x}.0.us}} = phi i64 [ \%37, \%if.end.i.us ], [ 0, ]$ ... %pregion\_for\_entry.entry.i.us.preheader ] %12 = trunc i64 %\_local\_id\_x.0.us to i32 %13 = mul i 32 %12, %3%14 = add i32 %13, %11 %15 = sext i 32 % 14 to i 64%scevgep27 = getelementptr float, float\* %2, i64 %15 %scevgep28 = getelementptr float, float\* %1, i64 %15 %add1.i.i.us = add nuw nsw i64 % local id x.0.us, %mul.i.i, ...!llvm.access.group!12 %conv.i.us = trunc i64 %add1.i.i.us to i32, !llvm.access.group !12 %cmp.i.us = icmp slt i32 %conv.i.us, %3, !llvm.access.group !12 br il %cmp.i.us, label %for.body.lver.check.i.us, label %if.end.i.us, ...!llvm.access.group!12 for.body.lver.check.i.us: %mul.i.us = mul nsw i32 %conv.i.us, %3, !llvm.access.group !12 %16 = sext i32 %mul.i.us to i64, !llvm.access.group !12 %scevgep.i.us = getelementptr float, float\* %2, i64 %16, !llvm.access.group %17 = add nsw i64 %16, %wide.trip.count.i, !llvm.access.group !12 %scevgep94.i.us = getelementptr float, float\* %2, i64 %17, ...!llvm.access.group!12 %scevgep96.i.us = getelementptr float, float\* %1, i64 %16, ...!llvm.access.group!12 %scevgep98.i.us = getelementptr float, float\* %1, i64 %17, ...!llvm.access.group!12 %bound0.i.us = icmp ult float\* %scevgep.i.us, %scevgep98.i.us, ...!llvm.access.group!12 %bound1.i.us = icmp ult float\* %scevgep96.i.us, %scevgep94.i.us, ...!llvm.access.group!12 %found.conflict.i.us = and i1 %bound0.i.us, %bound1.i.us, !llvm.access.group br i1 %found.conflict.i.us, label ... %for.body.lver.orig.lver.orig.i.us.lver.check, label %for.body.ph.i.us, ...!llvm.access.group!12 for.body.ph.i.us: for.body.lver.orig.lver.orig.i.us.lver.check: %load initial.i1.us13 = load float, float\* %scevgep.i.us, align 4, br i1 %found.conflict, label ...!llvm.access.group!12
%load\_initial102.i2.us14 = load float, float\* %scevgep96.i.us, align 4, ... %for.body.lver.orig.lver.orig.i.us.lver.orig.preheader, label ... %for.body.lver.orig.lver.orig.i.us.ph ...!llvm.access.group!12 F br label %for.body.i.us, !llvm.access.group !12 for.body.i.us: %indvars.iv.next.i10.us = phi i64 [ %indvars.iv.next.i.us, %for.body.i.us ], ... [ 1, %for.body.ph.i.us ] %sub18.i8.us = phi float [ %sub18.i.us, %for.body.i.us ], [ ... %load\_initial.i1.us13, %for.body.ph.i.us ] %sub42.i6.us = phi float [ %sub42.i.us, %for.body.i.us ], [ ... %load\_initial102.i2.us14, %for.body.ph.i.us ] %27 = add nsw i64 %indvars.iv.next.i10.us, %16, !llvm.access.group !12 %arrayidx.i.us = getelementptr inbounds float, float\* %2, i64 %27, ...!llvm.access.group!12
%28 = load float, float\* %arrayidx.i.us, align 4, !tbaa!14, ...!llvm.access.group!12 %arrayidx11.i.us = getelementptr inbounds float, float\* %0, i64 %27, ...!llvm.access.group!12
%29 = load float, float\* %arrayidx11.i.us, align 4, !tbaa!14, .. !llvm.access.group !12 %mul12.i.us = fmul float %sub18.i8.us, %29, !llvm.access.group !12 %div.i.us = fdiv float %mul12.i.us, %sub42.i6.us, !fpmath !18, ...!llvm.access.group!12 for.body.lver.orig.lver.orig.i.us.ph:
%load\_initial = load float, float\* %scevgep27, align 4 %sub18.i.us = fsub float %28, %div.i.us, !llvm.access.group !12 store float %sub18.i.us, float\* %arrayidx.i.us, align 4, !tbaa !14, for.body.lver.orig.lver.orig.i.us.lver.orig.preheader: %load initial 29 = load float, float\* %scevgep 28, align 4 br label %for.body.lver.orig.lver.orig.i.us.lver.orig ...!llvm.access.group!12 br label %for.body.lver.orig.lver.orig.i.us %arrayidx26.i.us = getelementptr inbounds float, float\* %1, i64 %27, ...!llvm.access.group!12
%30 = load float, float\* %arrayidx26.i.us, align 4, !tbaa!14, "...!llvm.access.group!12"

%31 = load float, float\* %arrayidx11.i.us, align 4, !tbaa!14, ...!llvm.access.group!12
%mul35.i.us = fmul float %31, %31, !llvm.access.group!12
%div41.i.us = fdiv float %mul35.i.us, %sub42.i6.us, !fpmath!18, ...!llvm.access.group!12
%sub42.i.us = fsub float %30, %div41.i.us,!llvm.access.group!12
store float %sub42.i.us, float\* %arrayidx26.i.us, align 4,!tbaa!14, ...!llvm.access.group!12
%indvars.iv.next.i.us = add nuw nsw i64 %indvars.iv.next.i10.us, 1, ...!llvm.access.group!12 %exitcond.not.i.us = icmp eq i64 %indvars.iv.next.i.us, %wide.trip.count.i, ...!llvm.access.group!12 br i1 %exitcond.not.i.us, label %if.end.i.us.loopexit36, label ... %for.body.i.us, !llvm.loop !19, !llvm.access.group !12 for.body.lver.orig.lver.orig.i.us.lver.orig: %indvars.iv.next.lver.orig.lver.orig.i12.us.lver.orig = phi i64 [ ... %indvars.iv.next.lver.orig.lver.orig.i.us.lver.orig, ... %for.body.lver.orig.lver.orig.i.us.lver.orig ], [ 1, .. %for.body.lver.orig.lver.orig.i.us.lver.orig.preheader ] for.body.lver.orig.lver.orig.i.us: %18 = add nsw i64 %indvars.iv.next.lver.orig.lver.orig.i12.us.lver.orig, %store forwarded32 = phi float [ %load initial29, ... %16, !llvm.access.group !12 ... %for.body.lver.orig.lver.orig.i.us.ph ], [~sub42.lver.orig.lver.orig.i.us, %arrayidx.lver.orig.lver.orig.i.us.lver.orig = getelementptr inbounds float, ... %for.body.lver.orig.lver.orig.i.us ]
%store\_forwarded = phi float [ %load\_initial, ... float\* %2, i64 %18, !llvm.access.group !12 %19 = load float, float\* %arrayidx.lver.orig.lver.orig.i.us.lver.orig, align ... %for.body.lver.orig.lver.orig.i.us.ph J, [ %sub18.lver.orig.lver.orig.i.us, ... 4, !tbaa !14, !llvm.access.group !12 %20 = add nsw i64 %18, -1, !llvm.access.group !12 .. %for.body.lver.orig.lver.orig.i.us %indvars.iv.next.lver.orig.lver.orig.i12.us = phi i64 [ 1, %arrayidx7.lver.orig.lver.orig.i.us.lver.orig = getelementptr inbounds ... %for.body.lver.orig.lver.orig.i.us.ph ], [ .. float, float\* %2, i64 %20, !llvm.access.group !12 ... %indvars.iv.next.lver.orig.lver.orig.i.us, %for.body.lver.orig.lver.orig.i.us %21 = load float, float\* %arrayidx7.lver.orig.lver.orig.i.us.lver.orig, ... align 4, !tbaa !14, !llvm.access.group !12` %32 = add nsw i64 %indvars.iv.next.lver.orig.lver.orig.i12.us, %16, %arrayidx11.lver.orig.lver.orig.i.us.lver.orig = getelementptr inbounds ... float, float\* %0, i64 %18, !llvm.access.group !12 ...!llvm.access.group!12 %arrayidx.lver.orig.lver.orig.i.us = getelementptr inbounds float, float\* %22 = load float, float\* %arrayidx11.lver.orig.lver.orig.i.us.lver.orig, ... %2, i64 %32, !llvm.access.group !12 %33 = load float, float\* %arrayidx.lver.orig.lver.orig.i.us, align 4, !tbaa ... align 4, !tbaa !14, !llvm.access.group !12 %mul12.lver.orig.lver.orig.i.us.lver.orig = fmul float %21, %22, ...!14,!llvm.access.group!12 ..!llvm.access.group!12 %arrayidx11.lver.orig.lver.orig.i.us = getelementptr inbounds float, float\* %arrayidx17.lver.orig.lver.orig.i.us.lver.orig = getelementptr inbounds ... float, float\* %1, i64 %20, !llvm.access.group !12 ... %0, i64 %32, !llvm.access.group !12 %34 = load float, float\* %arrayidx11.lver.orig.lver.orig.i.us, align 4, %23 = load float, float\* %arrayidx17.lver.orig.lver.orig.i.us.lver.orig, ...!tbaa!14,!llvm.access.group!12 .. align 4, !tbaa !14, !llvm.access.group !12 %mul12.lver.orig.lver.orig.i.us = fmul float %store forwarded, %34, %div.lver.orig.lver.orig.i.us.lver.orig = fdiv float ... %mul12.lver.orig.lver.orig.i.us.lver.orig, %23, !fpmath !18, ...!llvm.access.group!12 %div.lver.orig.lver.orig.i.us = fdiv float %mul12.lver.orig.lver.orig.i.us, ... %store\_forwarded32, !fpmath !18, !llvm.access.group !12 ...!llvm.access.group!12 %sub18.lver.orig.lver.orig.i.us.lver.orig = fsub float %19, %sub18.lver.orig.lver.orig.i.us = fsub float %33, ... %div.lver.orig.lver.orig.i.us.lver.orig, !llvm.access.group !12 ... %div.lver.orig.lver.orig.i.us, !llvm.access.group !12 store float %sub18.lver.orig.lver.orig.i.us.lver.orig, float\* store float %sub18.lver.orig.lver.orig.i.us, float\* ... %arrayidx.lver.orig.lver.orig.i.us.lver.orig, align 4, !tbaa !14, ... %arrayidx.lver.orig.lver.orig.i.us, align 4, !tbaa !14, !llvm.access.group !12 %arrayidx26.lver.orig.lver.orig.i.us = getelementptr inbounds float, float\* ...!llvm.access.group!12 %arrayidx26.lver.orig.lver.orig.i.us.lver.orig = getelementptr inbounds ... float, float\* %1, i64 %18, !llvm.access.group !12 .. %1, i64 %32, !llvm.access.group !12 %35 = load float, float\* %arrayidx26.lver.orig.lver.orig.i.us, align 4, %24 = load float, float\* %arrayidx26.lver.orig.lver.orig.i.us.lver.orig, ...!tbaa!14,!llvm.access.group!12 .. align 4, !tbaa !14, !llvm.access.group !12 %36 = load float, float\* %arrayidx11.lver.orig.lver.orig.i.us, align 4, %25 = load float, float\* %arrayidx11.lver.orig.lver.orig.i.us.lver.orig, .. !tbaa !14, !llvm.access.group !12 ... align 4, !tbaa !14, !llvm.access.group !12 %mul35.lver.orig.lver.orig.i.us = fmul float %36, %36, !llvm.access.group !12 %mul35.lver.orig.lver.orig.i.us.lver.orig = fmul float %25, %25, %div41.lver.orig.lver.orig.i.us = fdiv float .. !llvm.access.group !12 ... %mul35.lver.orig.lver.orig.i.us, %store\_forwarded32, !fpmath !18, %26 = load float, float\* %arrayidx17.lver.orig.lver.orig.i.us.lver.orig, ...!llvm.access.group!12 ... align 4, !tbaa !14, !llvm.access.group !12 %sub42.lver.orig.lver.orig.i.us = fsub float %35, %div41.lver.orig.lver.orig.i.us.lver.orig = fdiv float ... %div41.lver.orig.lver.orig.i.us, !llvm.access.group !12 ... %mul35.lver.orig.lver.orig.i.us.lver.orig, %26, !fpmath !18, store float %sub42.lver.orig.lver.orig.i.us, float\* ...!llvm.access.group!12 ... %arrayidx26.lver.orig.lver.orig.i.us, align 4, !tbaa !14, !llvm.access.group %sub42.lver.orig.lver.orig.i.us.lver.orig = fsub float %24, ... !12 ... %div41.lver.orig.lver.orig.i.us.lver.orig, !llvm.access.group !12 %indvars.iv.next.lver.orig.lver.orig.i.us = add nuw nsw i64 store float %sub42.lver.orig.lver.orig.i.us.lver.orig, float\* ... %indvars.iv.next.lver.orig.lver.orig.i12.us, 1, !llvm.access.group !12 ... %arrayidx26.lver.orig.lver.orig.i.us.lver.orig, align 4, !tbaa !14, %exitcond.not.lver.orig.lver.orig.i.us = icmp eq i64 ...!llvm.access.group!12 ... %indvars.iv.next.lver.orig.lver.orig.i.us, %wide.trip.count.i, %indvars.iv.next.lver.orig.lver.orig.i.us.lver.orig = add nuw nsw i64 ...!llvm.access.group!12 ... %indvars.iv.next.lver.orig.lver.orig.i12.us.lver.orig, 1, !llvm.access.group br i1 %exitcond.not.lver.orig.lver.orig.i.us, label %if.end.i.us.loopexit35, ... label %for.body.lver.orig.lver.orig.i.us, !llvm.loop !19, !llvm.access.group %exitcond.not.lver.orig.lver.orig.i.us.lver.orig = icmp eq i64 ... !12 ... %indvars.iv.next.lver.orig.lver.orig.i.us.lver.orig, %wide.trip.count.i, ...!llvm.access.group!12 br i1 %exitcond.not.lver.orig.lver.orig.i.us.lver.orig, label ... %if.end.i.us.loopexit, label %for.body.lver.orig.lver.orig.i.us.lver.orig, ...!llvm.loop!19,!llvm.access.group!12 if.end.i.us.loopexit35: if.end.i.us.loopexit36: if.end.i.us.loopexit: br label %if.end.i.us br label %if.end.i.us br label %if.end.i.us if.end.i.us: %37 = add nuw nsw i64 % local id x.0.us, 1%exitcond.not = icmp eq i64 %37, 256 br i1 %exitcond.not, label %adi\_kernel1.exit.loopexit, label ... %pregion for entry.entry.i.us, !llvm.loop!21 adi\_kernel1.exit.loopexit: br label %adi\_kernel1.exit adi kernel1.exit:

ret void