Design of High Speed Link System

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Abstract— A high speed data link with total length over twenty inches is proposed in this paper. With feed forward equalizer (FFE), and decision feed-back equalizer(DFE), the data rate can goes up to 20Gbps. The passive channel consists of bonding wire for package to printed circuit board (PCb) transition, total 12 inches of PCB lines, and two top-to-bottom via transition in PCB. With carefully designed matching network for each discontinuity, the overall performance of passive channel has -5dB insertion loss at 10GHz. Combined with DFE and FFE, the resulting eye has 98% eye width and 92% eye height at 3Gbps, and 66% eye width and 81.5% eye height at 20Gbps.

1. INTRODUCTION

With increasing speed, the urgent demand on higher performance for high speed link has become a critical problem in signal integrity. High-speed backplane serial I/O interconnections such as PCI-Express [1], Serial ATA (SATA) [2], Thunderbolt [3] amazed us years ago. However, the dawning mobile age shows even higher demand on high speed data link. Fig. 1 shows the increasing data rate of PCI Express [1].

	Raw Bit Rate	Link BW	BW/Lane/Way	Total BW x16
PCIe 1.x	2.5GT/s	2Gb/s	~250MB/s	~8GB/s
PCIe 2.x	5.0GT/s	4Gb/s	~500MB/s	~16GB/s
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s

Figure 1: Data rate of PCI Express in different generations [4].

To improve the signal integrity (SI) of high speed link, several techniques has been proposed. Matching network, passive equalizers, analog equalizers, and digital equalizers were proposed in several different scenarios. However, because fo simplicity, FFE and DFE are the two most used finite impulse response (FIR) filter to equalize the desired channel.

This report is organized as follow, first we will give a system level preview. Then the design procedure of channel and equalizers are described in following sections. Finally the overall systems will be simulated in Cadence Virtuoso.

2. SYSTEM LEVEL DESIGN

The high speed link we built consists of three main subsystems, namely the transmitter (TX) block, the channel block and the receiver (RX) block. Two paths are designed to transmit the bit stream and the clock signal separately.

In the TX block, signal path is composed of a data transmitter and a feed-forward equalizer (FFE) implemented with Verilog, whereas the clock path has a clock transmitter connected to the external clock generator. Both transmitters can be implemented using transistor level inverters.

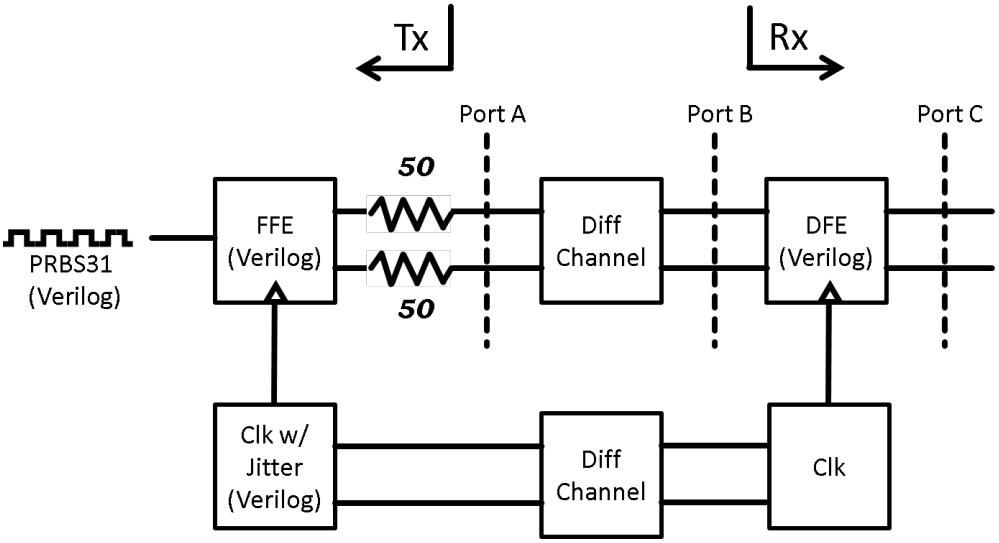


Figure 2: Block diagram of entire high speed link.

The channel block consists of bonding wire and the actual signal traces. Since the channel we built is largely symmetric, in order to speed up the simulation, we adopt 'divide and conquer' strategy. We split our channel into 24 small blocks. It turns out that there are only four distinct type of structures we need to simulate, namely the PCB trace, the via transition, package trace and bonding wire transition. After obtaining the S-parameter data for each individual block, we cascade the S-parameter using Keysight ADS and quickly obtain the S-parameter for the entire channel.

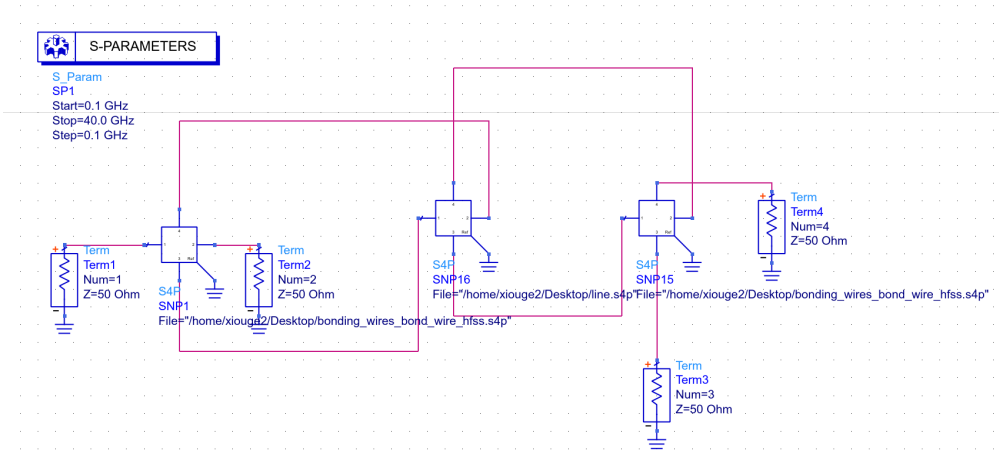


Figure 3: Partial ADS Schematics for S-parameter Cascade.

In the RX block, signal path is composed of a transistor level data amplifier to make up for signal loss in the channel, and a decision feedback equalizer (DFE) implemented with Verilog. Whereas the clock path has a transistor level clock amplifier and a Verilog clock deskew block. Decision output from the DFE will be the output for the RX block and the entire high speed link.

To test the system, a random bit stream is generated using the PRBS unit in Cadence Virtuoso and fed into the input of FFE in the TX block. Eye diagrams at the input of channel, input and

output of the DFE are plotted to evaluate performance of the high speed link.

3. CHANNEL DESIGN

Since the target bit rate is quite high (3Gbps), we used one of the low loss substrate to design our PCB. The RO4003 from Rogers company is widely used to design various high frequency circuit [5]. We use PCB of 9 layers of metal. Fig. 4 shows the dimensions of each layers. The top and bottom layer are the signal layer, and the rest 7 layers at the middle of the PCB are simulated as ground layer. These ground layers were later connected using grounded vias. Each layer is of 19 mil height, and the thickness of metal is 1 mil.

As for package, we use one layer of thin-film ceramic from Murawa [6]. The substrate is far more thinner than those used in PCB. Table. 1 shows the material properties used for PCB and package.

Usage	Substrate	Trace	Metal Layers	ε_r	$\tan\delta$
PCB	RO4003 [5]	Copper	9	3.8	0.02
Package	Alumina [6]	Copper	2	9.8	0.02

Table 1: Material properties used for channel design.

3.1. PCB Traces

The differential PCB traces are designed such that the single line impedance is 50 Ω, and the differential impedance is 100 Ω. Fig. 5 and Table. 2 shows the design parameters to achieve the desired impedance. The 2D extraction tool, Ansys Q2D is used to analyze and fine-tune the parameters. Fig. 6 shows the impedance of the differential line up to 40GHz. It shows that the differential impedance is 96Ω while the common impedance is 25Ω at 10GHz.

Parameters	Value	Parameters	Value	Parameters	Value	Parameters	Value
W_{PCB}	40 mil	D_{PCB}	80 mil	H_{PCB}	19 mil	T_{PCB}	1 mil

Table 2: Design parameter of PCB trace.

3.2. Via Transition

Since there will be a via transition from top to the bottom of the PCB, the strong discontinuity of this via transition will cause strong reflection, as shown in Fig. 4. The entire structure, however, can be modeled using quasi-static approach. The via itself can be modeled as lumped resistance and inductance, and the parasitic capacitance distributed around the via to the ground plane surrounded. Fig. 7b shows the quasi-static models of via transition, and Fig. 7c shows the lumped model of via transition of differential line.

The 3D quasi-static extraction tool Ansys Q3D [7] is used to extract the lumped element of these conductor. Fig. 7a shows the via transition model for Q3D extraction. Since the structure is symmetry, to lower the reflection, a simple approximation can be used. The lumped differential impedance defined in 1 is set to be 100 Ω. This can be achieved through adjusting the radius of anti-pad, r_anti in Fig. 4.

$$Z_{diff}^{lump} \equiv \sqrt{\frac{L_{11} - L_{12}}{C_{11} + |C_{12}|}} = 100\Omega \tag{1}$$

Parameters	Value	Parameters	Value
R_{Anti}	75 mil	R_{Via}	20 mil

Table 3: Design parameter of PCB trace.

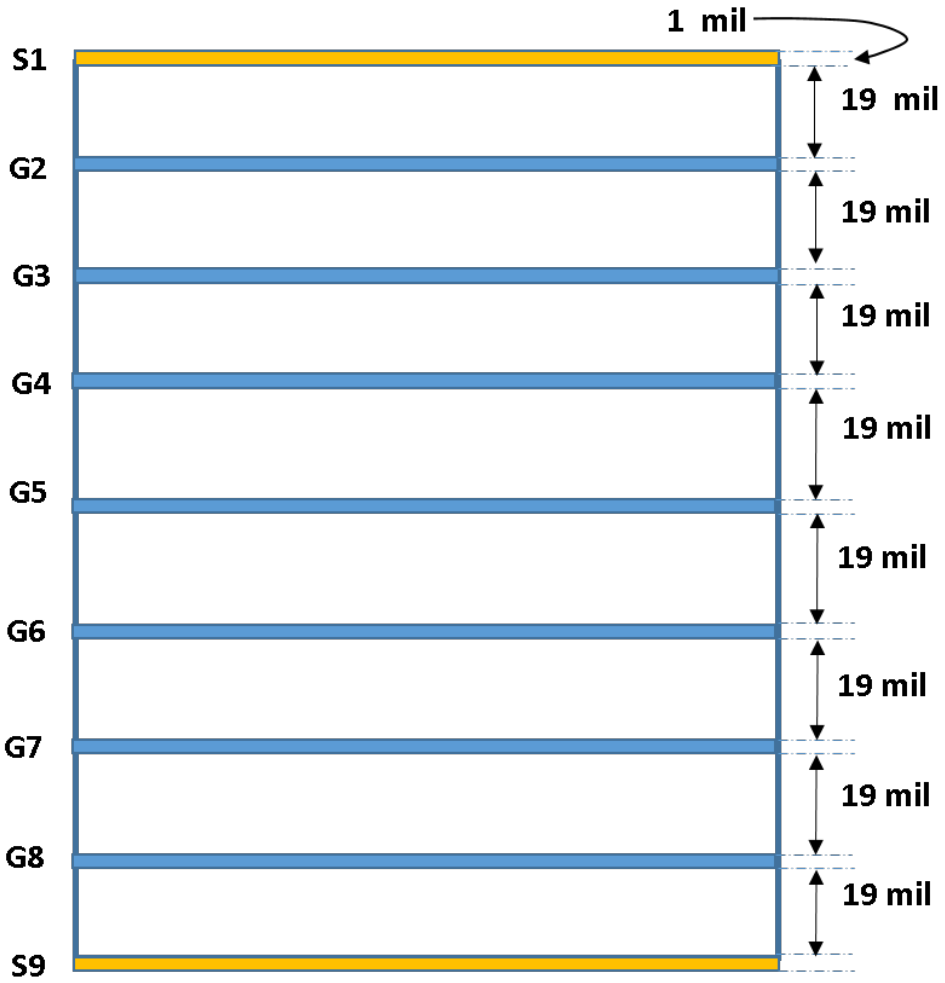


Figure 4: Dimension and layers in designated PCB. $r\_via = 20mil$ is the radius of both signal and ground via. The height of each PCB layer is 19 mil, and the thickness of copper is 1 mil.

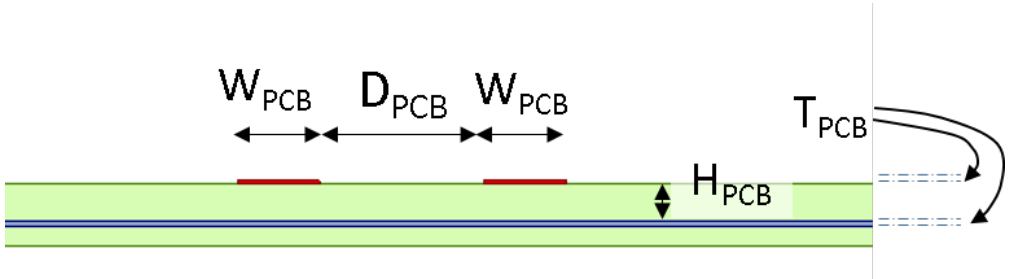


Figure 5: Design parameter of PCB traces.

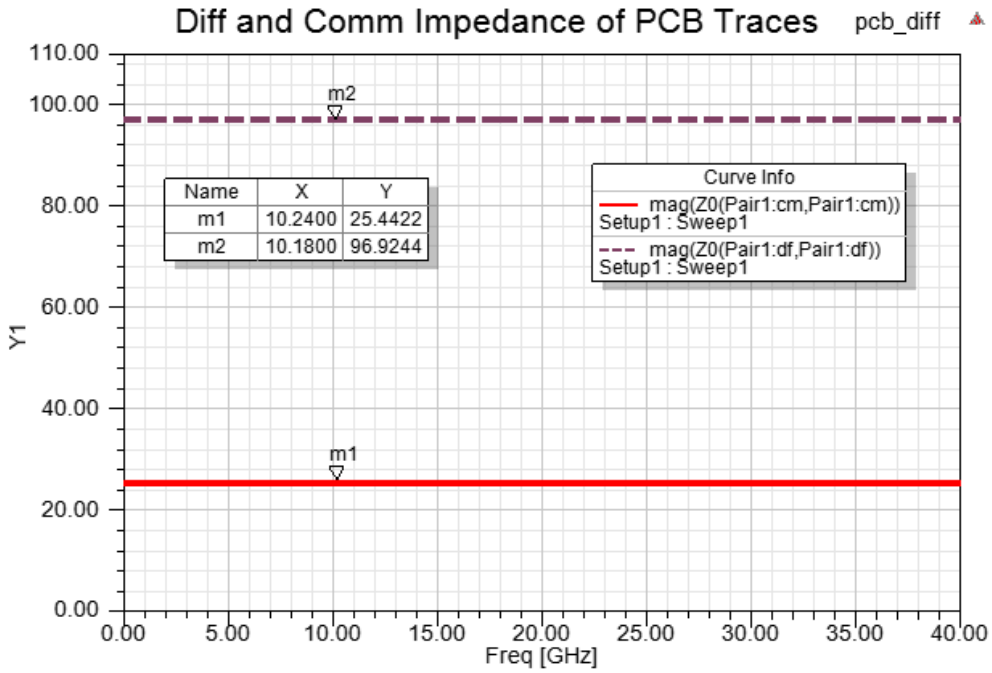


Figure 6: Differential and common impedance of designated PCB traces. Solid: common mode impedance; dash: differential mode impedance.

The preliminary result given in Q3D is later imported into HFSS for full-wave simulation. To eliminate the higher order mode around the discontinuity, 1 inch of microstrips are attached at both end of vias. Fig. 8 shows the structure used in HFSS, and Fig. 9 shows the S parameter of differential and common mode. The high level of S_{11}^{cc} shows good common mode rejection, around -10dB, below 10GHz, while the S_{11}^{dd} remains below -20dB below 10 GHz. Fig. 10 shows the smith chart of S_{11}^{dd}. The low reflection of differential mode can be observed that the reflection is below 0.26 with 10 GHz.

3.3. Package Traces

Similar procedure described in 3.1 can also be applied to the designation of traces on packages. The material properties of substrate used in package is described in Table. 1. Fig. 11 and Table. 4 shows the design parameters to achieve the desired impedance, and Fig. 12 shows the impedance of the differential line up to 40 GHz. It shows that the differential impedance is 96Ω while the common impedance is 25Ω at 10GHz.

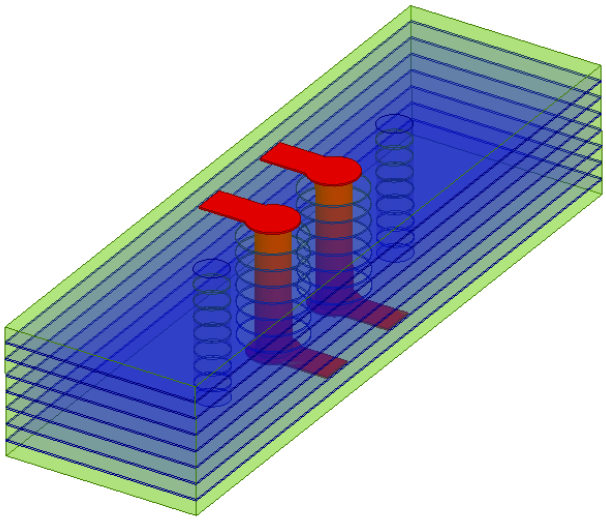
Parameters	Value	Parameters	Value	Parameters	Value	Parameters	Value
W_{PKG}	367 um	D_{PKG}	3.33 mm	H_{PKG}	400 um	T_{PKG}	17 um

Table 4: Design parameter of PCB trace.

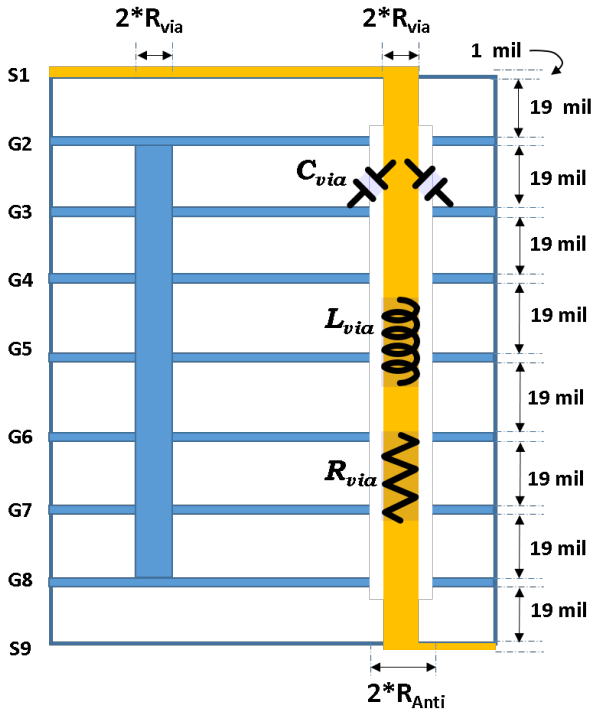
3.4. Bonding Wire Transition

The transition between package and PCB is through using bonding wire. Fig. 13 shows the transition structure of bonding wire, and Table. 5 shows the corresponding design parameter. Similar to via transition in PCB described in Sec.3.2, the lumped model shown in Fig. 7c also applied here. However, since the bonding wire is a very resistive and inductive, the additional patches were attached at the both side of bonding wire in order to decrease the differential impedance. Same equation in (1) can also be applied here.

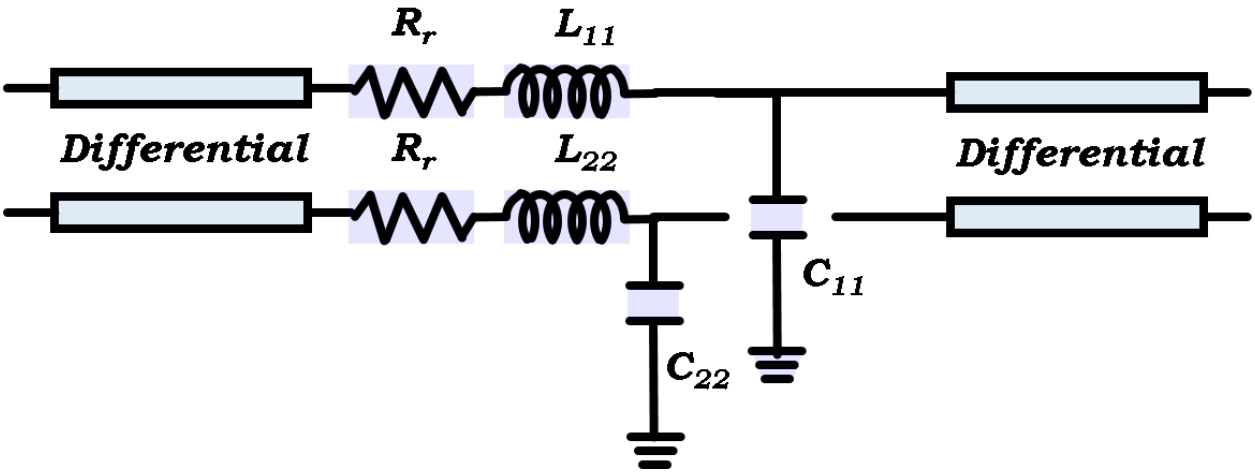
Fig. 14 shows the S parameter of both differential and common mode, and Fig.15 also shows the S_{11}^{dd} and S_{22}^{dd} on Smith chart. It can be observed that the reflection of differential modes from both ports have 0.1 reflection at 3GHz, whereas half the reflection at 10GHz. The high reflection at high



(a) Via transition simulated in Q3D for lumped element extraction.

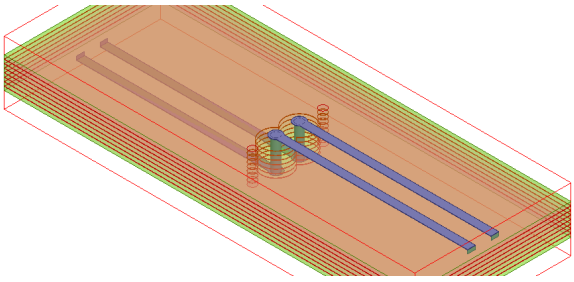


(b) Lumped model of via transition.

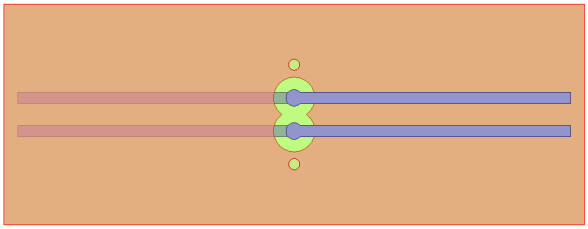


(c) Lumped model of via transition.

Figure 7: Via transition model for Q3D extraction.



(a) Tilted view.



(b) Top view.

Figure 8: Via transition simulated in HFSS.

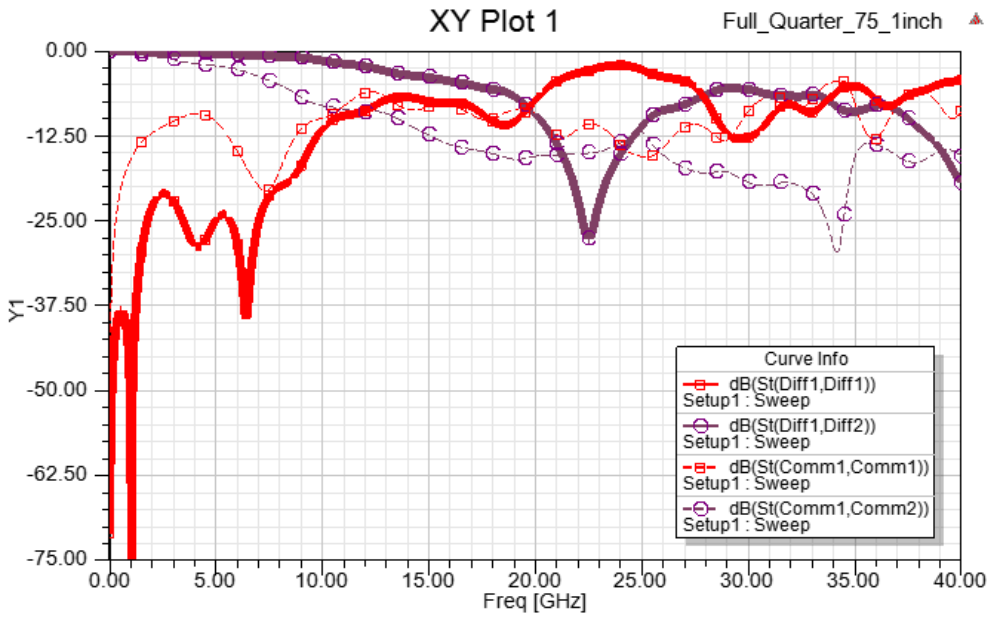


Figure 9: S parameter of via transition in PCB. $r\_anti = 75mil$. Solid: S11 and S12 of differential mode; dash: S11 and S12 of common mode.

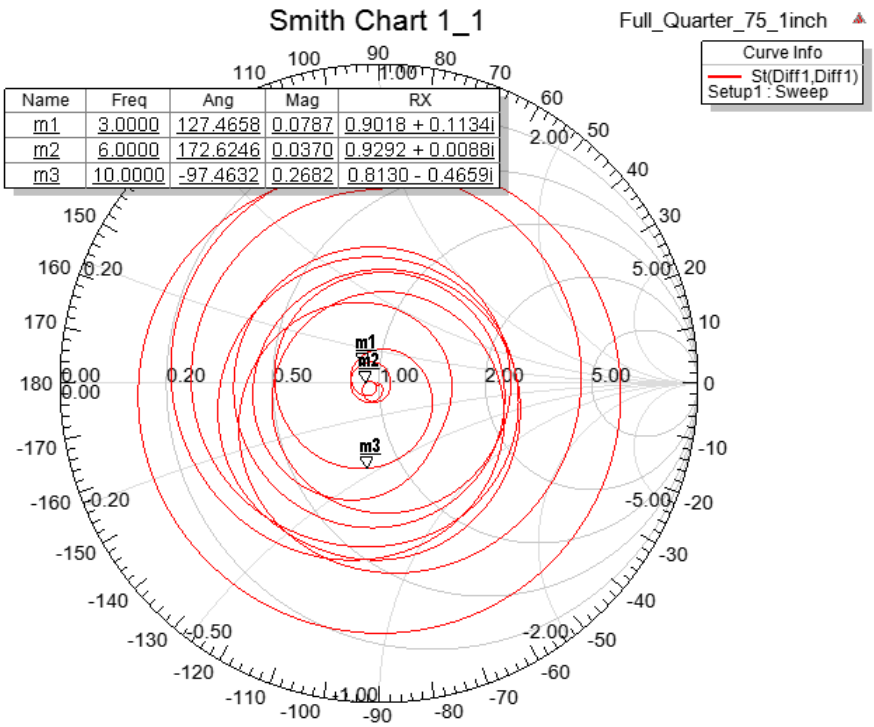


Figure 10: Smith chart of S_{11}^{dd} of via transition in PCB.

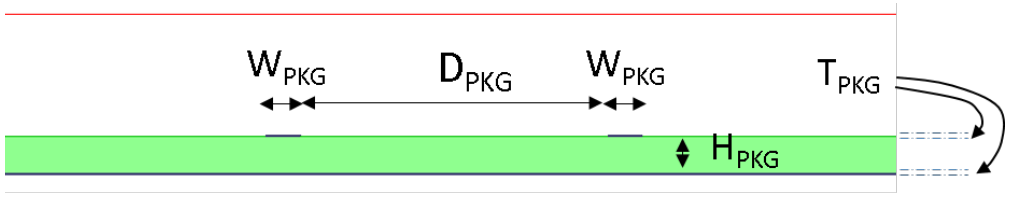


Figure 11: Design parameter of package traces.

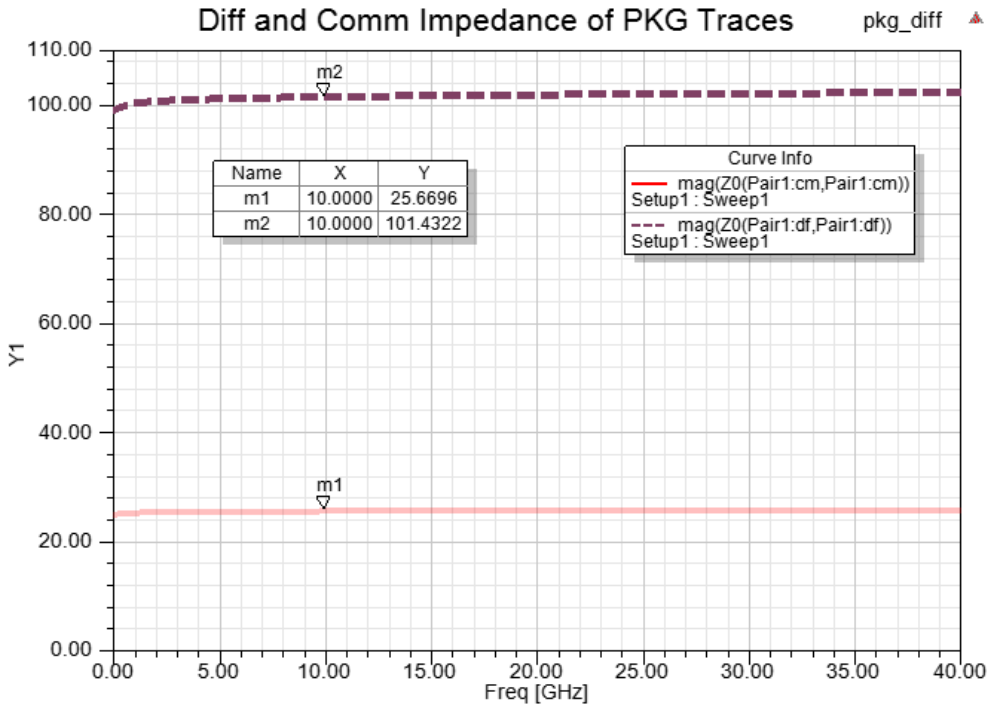


Figure 12: Differential and common impedance of designated PCB traces. Solid: common mode impedance; dash: differential mode impedance.

frequency is because adding patches can only be affective at low frequency. In [8], removing ground of both package and PCB will achieve better performance.

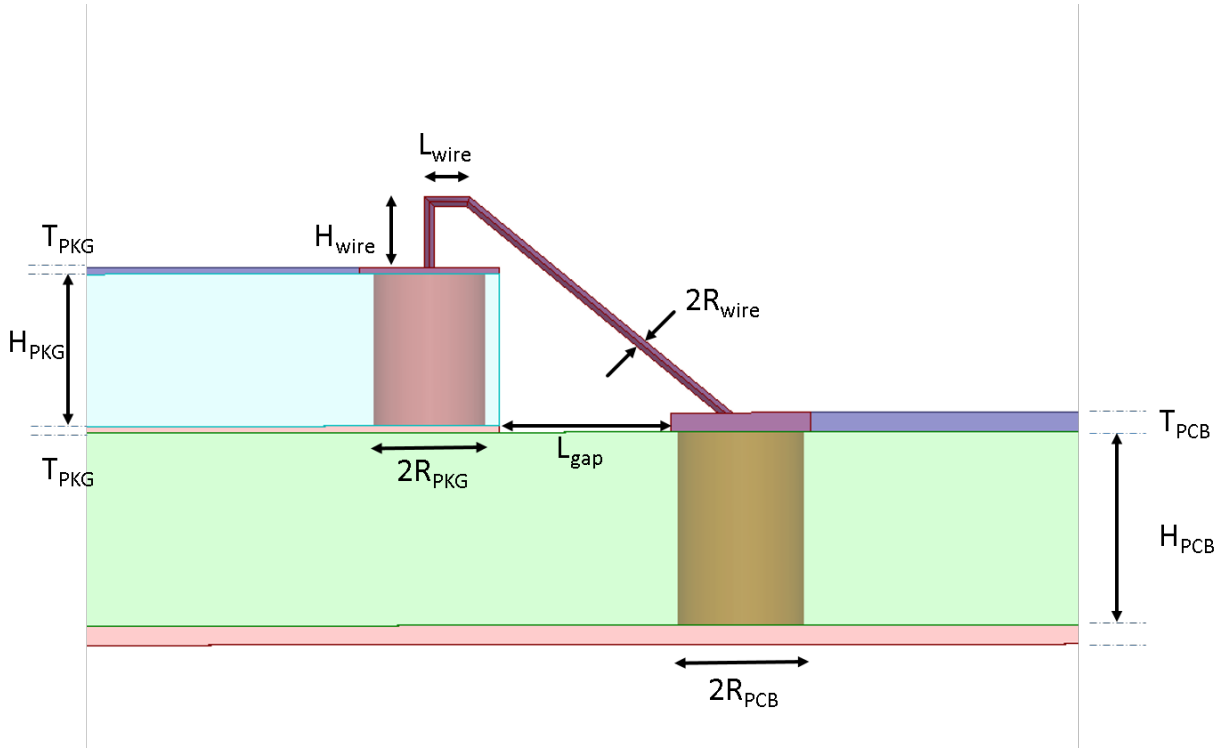
Parameters	Value	Parameters	Value	Parameters	Value	Parameters	Value
G_{PKG}	800 um	L_{Gap}	450 um	R_{PCB}	20 mil	R_{PKG}	20 mil
H_{Wire}	190 um	L_{Wire}	100 um	R_{Wire}	25 um	L_{Gap}	450 um
W_{PAD}	367 um	L_{PAD}	367 um	L_{PCB}	10 mm	L_{PKG}	6 mm
W_1	851 um	W_2	738 um	L_1	1653 um	L_2	1625 um

Table 5: Design parameter of bonding wire transition.

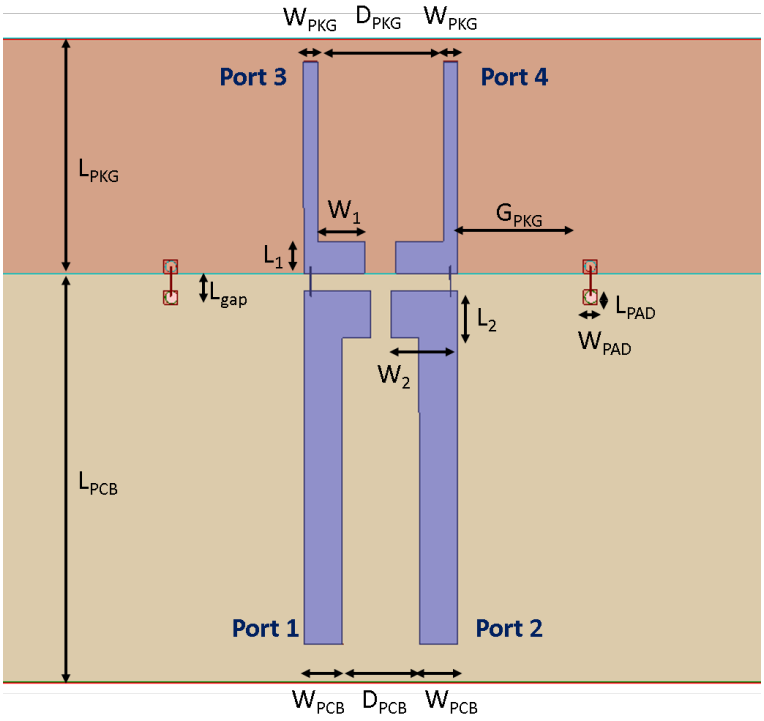
3.5. Channel Response without Equalization

After obtaining S-parameter for the entire channel from ADS cascade, we convert our 4 port S-parameters to Mixed Mode to observe the differential mode and common mode S-parameters respectively. Since our channel is designed to transmit differential signal, we want S_{11}^{dd} to be as small as possible to minimize reflection and S_{12}^{dd} to be as large as possible to minimize signal loss. Fig. 16 (a) confirms that our channel achieve the our goal and have very good performance.

In order to see the eye diagram and transient response for our channel at different bit rate, we also simulated our channel in Cadence Virtuoso with pseudo random bit sequence input for a long period of time. Fig. 17 and Fig. 19 shows the eye diagram of the input and output of the channel at 3 Gb/s and 20 Gb/s whereas Fig. 18 and Fig. 20 shows the transient response.



(a) Side view. The upper left side is package substrate, which is stacked on the PCB substrate.



(b) Top view. The upper side is package substrate.

Figure 13: Bonding wire transition simulated in HFSS.

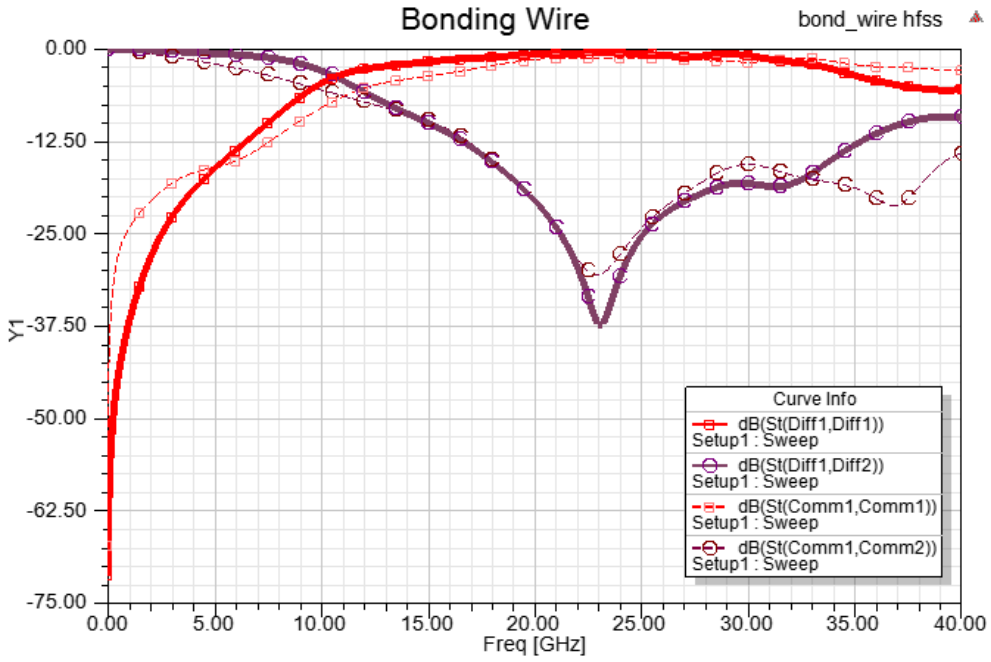
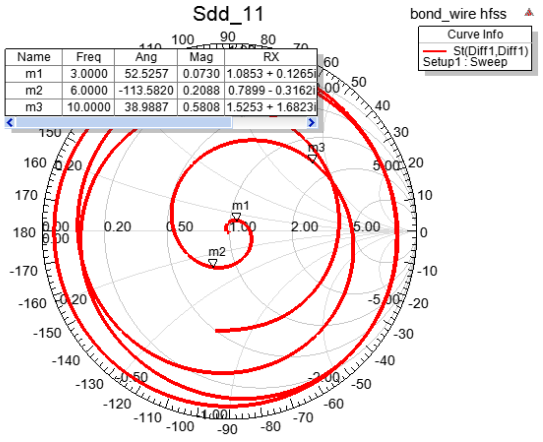
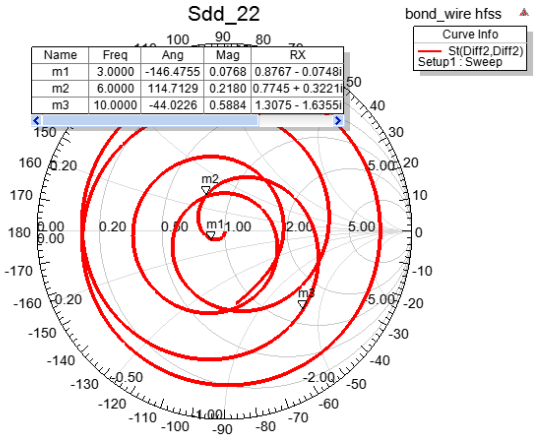


Figure 14: S parameter of bonding wire transition. Solid: S11 and S12 of differential mode; dash: S11 and S12 of common mode.

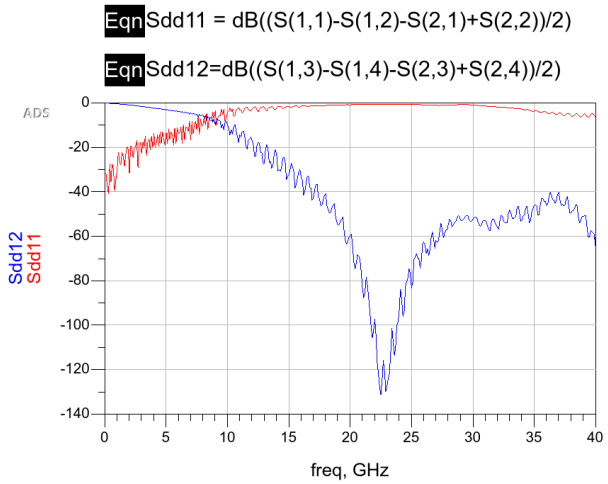


(a) Smith chart of S_{11}^{dd} of bonding wire.

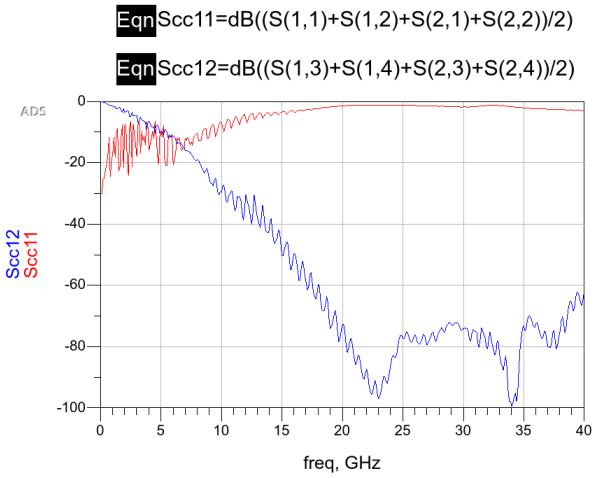


(b) Smith chart of S_{22}^{dd} of bonding wire.

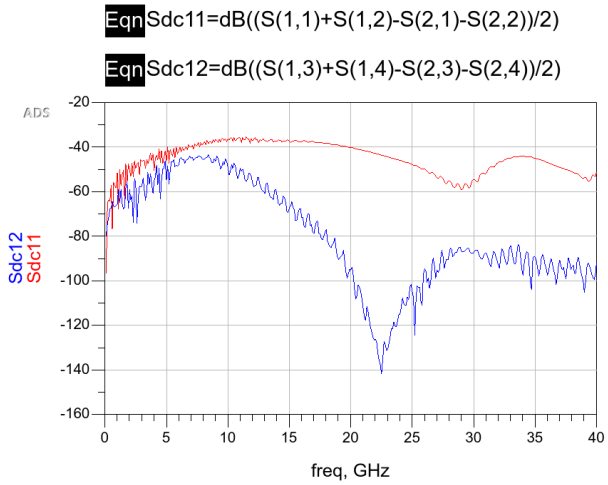
Figure 15: Smith chart of Sdd11 and Sdd22 of bonding wire transition.



(a) Differential Mode.

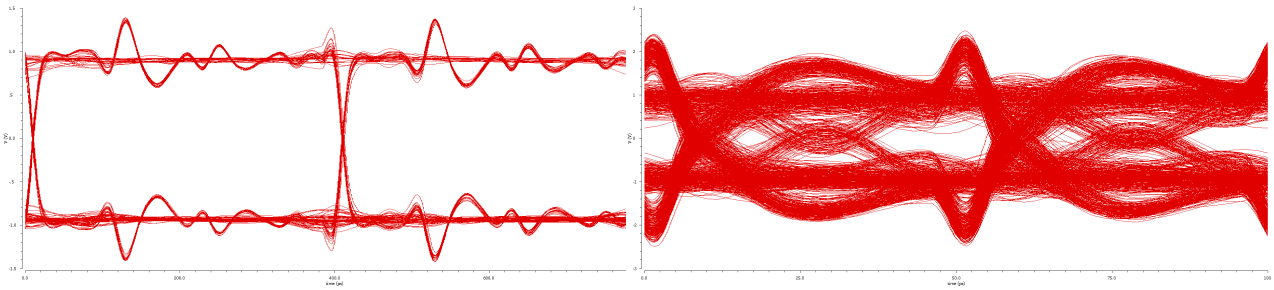


(b) Common Mode.



(c) Mixed Mode.

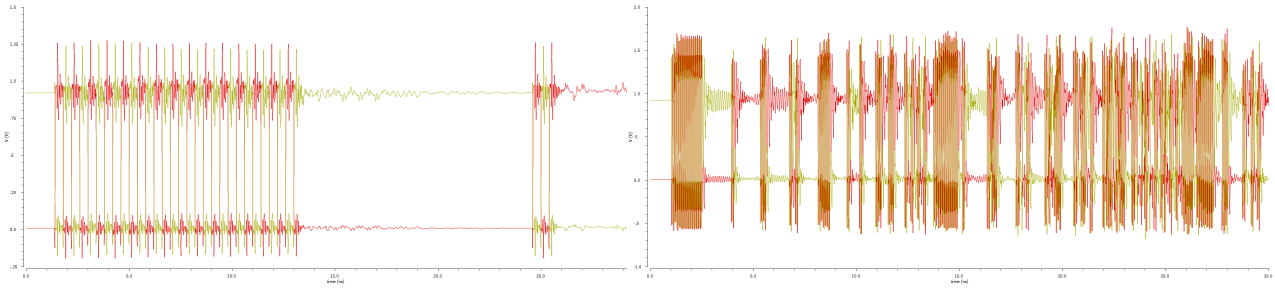
Figure 16: Mixed Mode S-parameter Response.



(a) 3 Gb/s.

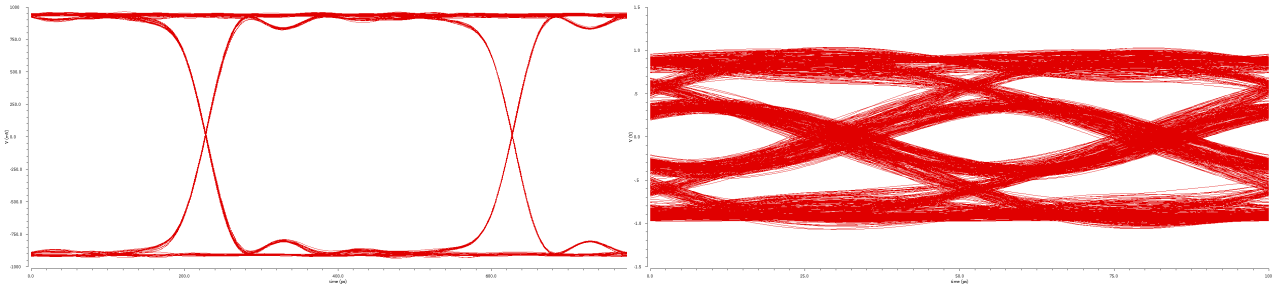
(b) 20 Gb/s.

Figure 17: Input Eye Diagram.



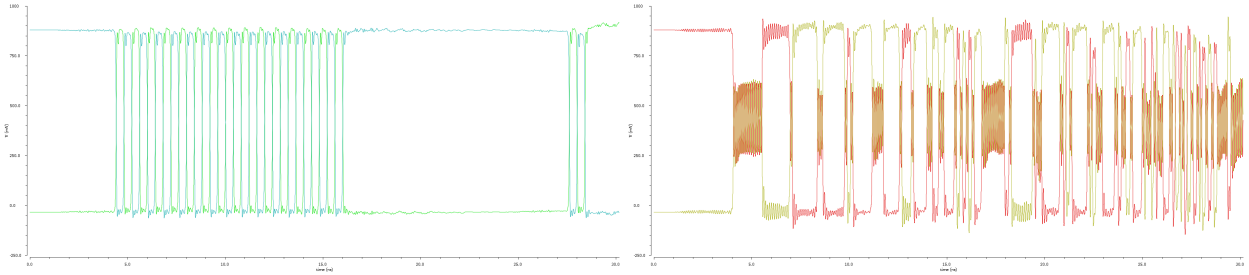
(a) 3 Gb/s. (b) 20 Gb/s.

Figure 18: Input Transient Response.



(a) 3 Gb/s. (b) 20 Gb/s.

Figure 19: Output Eye Diagram.

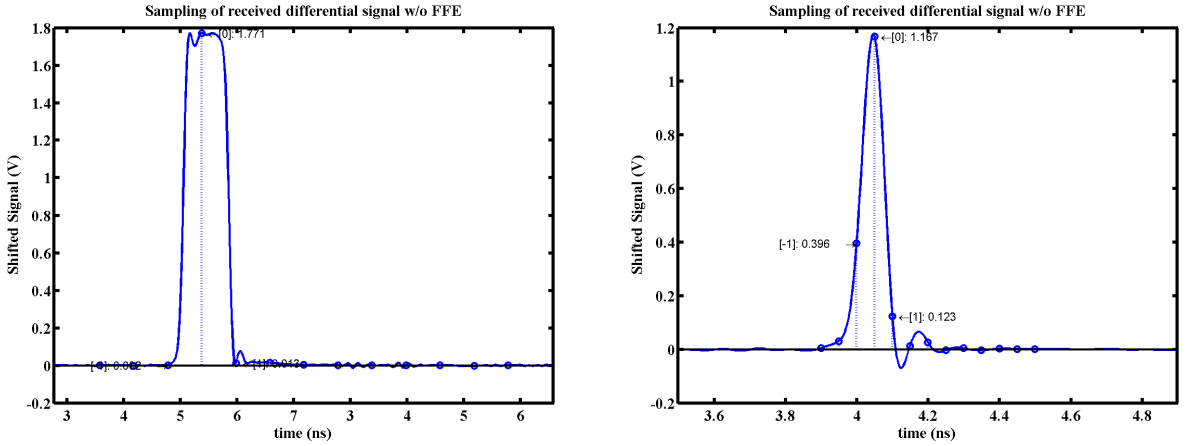


(a) 3 Gb/s. (b) 20 Gb/s.

Figure 20: Output Transient Response.

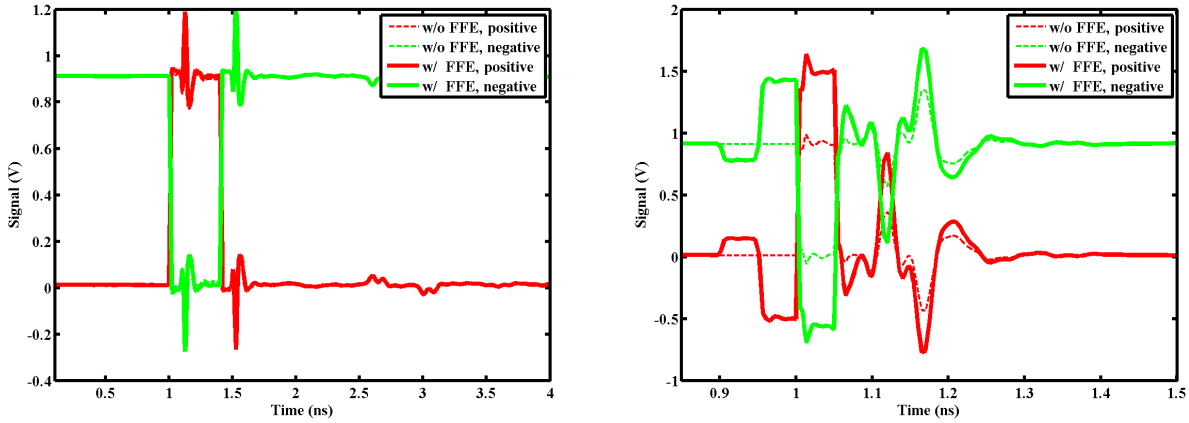
4. FEED FORWARD EQUALIZER

One of the FIR equalizer usually used is FFE. Since the FFE needs the "future" data bit, it is usually implemented in transmitted port. Fig. 21 shows the sampled plain channel differential response at received port. The discrete value of the sampled signal is listed at Table. 23c and Table. 24c. From Fig. 21 we can observe that there are two precursors in differential pulse response. Therefore, we will use two taps b_{-2}, b_{-1}, b_0 to eliminate it. Follow similar procedure described in [9], we may obtain the coefficient of each taps in FFE.



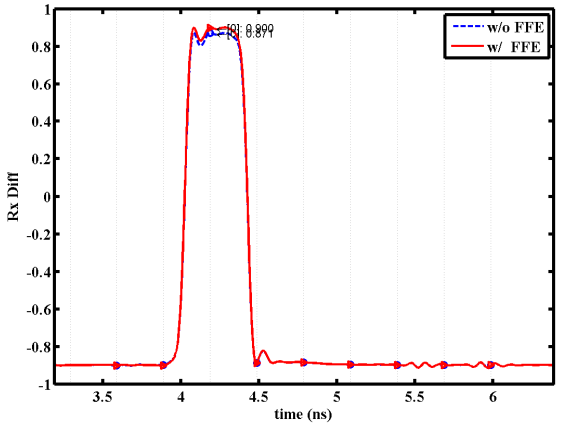
(a) 3 Gb/s. (b) 20 Gb/s.

Figure 21: Sampled received differential channel response w/o FFE.

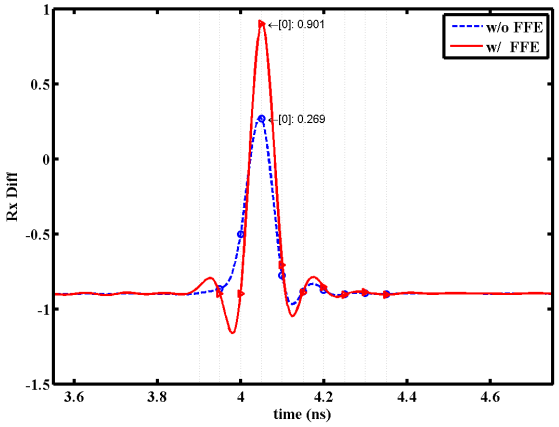


(a) 3 Gb/s. (b) 20 Gb/s.

Figure 22: Differential signal before channel w/ and w/o FFE.

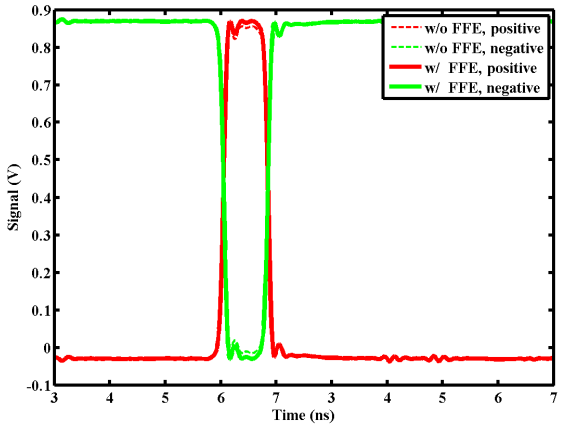


(c) 3 Gb/s.

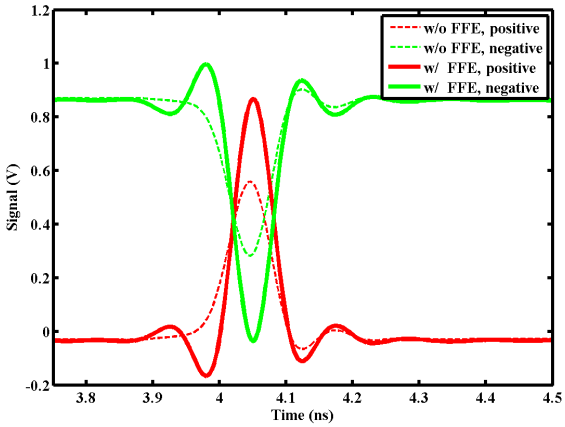


(d) 20 Gb/s.

Figure 22: Received differential channel response w/o or w FFE.



(e) 3 Gb/s.



(f) 20 Gb/s.

Figure 22: Terminal signal after channel w/ and w/o FFE.

b_{-2}	b_{-1}	b_0
0.000	-0.001	1.016

(a) Coefficient of FFE with 3Gb/s input.

n	-2	-1	0	1	2	3	4	5	6
V	-0.901	-0.898	0.871	-0.887	-0.885	-0.897	-0.898	-0.898	-0.899

(b) Sampled signal of received differential w/o FFE.

n	-2	-1	0	1	2	3	4	5	6
V	-0.9	-0.9	0.9	-0.886	-0.885	-0.897	-0.898	-0.898	-0.899

(c) Sampled signal of received differential with FFE.

Figure 23: FFE Coefficient and Effect of Equalization at 3 Gb/s

b_{-2}	b_{-1}	b_0
0.146	-0.558	1.599

(a) Coefficient of FFE with 20Gb/s input.

n	-2	-1	0	1	2	3	4	5	6
V	-0.867	-0.503	0.269	-0.775	-0.885	-0.872	-0.901	-0.894	-0.902

(b) Sampling signal of received differential w/o FFE.

n	-2	-1	0	1	2	3	4	5	6
V	-0.898	-0.898	0.901	-0.705	-0.892	-0.854	-0.906	-0.889	-0.905

(c) Sampling signal of received differential with FFE.

Figure 24: FFE Coefficient and Effect of Equalization at 20 Gb/s

c_1	c_2	c_3	c_4	c_5
0.014	0.015	0.004	0.003	0.002

(a) Coefficient of DFE with 3Gb/s input.

n	-2	-1	0	1	2	3	4	5	6
V	-0.9	-0.9	0.9	-0.886	-0.885	-0.897	-0.898	-0.898	-0.899

(b) Sampling signal of received differential w/o DFE.

n	-2	-1	0	1	2	3	4	5	6
V	-0.9	-0.9	0.9	-0.9	-0.9	-0.9	-0.9	-0.9	-0.899

(c) Sampling signal of received differential with DFE.

Figure 25: DFE Coefficient and Effect of Equalization at 3 Gb/s

c_1	c_2	c_3	c_4	c_5
0.194	0.007	0.046	-0.007	0.011

(a) Coefficient of DFE with 20Gb/s input.

n	-2	-1	0	1	2	3	4	5	6
V	-0.898	-0.898	0.901	-0.705	-0.892	-0.854	-0.906	-0.889	-0.905

(b) Sampling signal of received differential w/o DFE.

n	-2	-1	0	1	2	3	4	5	6
V	-0.898	-0.898	0.901	-0.899	-0.899	-0.899	-0.899	-0.899	-0.905

(c) Sampling signal of received differential with DFE.

Figure 26: DFE Coefficient and Effect of Equalization at 20 Gb/s

5. DECISION FEEDBACK EQUALIZER

Decision feedback equalizer (DFE) is a finite impulse response (FIR) filter based feedback scheme that reduces intersymbol Interference (ISI). The DFE consists of a slicer (Decision unit) and a FIR filter. The slicer makes symbol decisions and determine whether the FIR filter should be used to reduce the postcursors. By analyzing the input differential signal, we can predict the magnitude of postcursors and substract it ahead. Postcursors can then be reduced by making filter tap coefficients equal to postcursor magnitude but with an opposite sign.

$$c_i = V_d^{Rx}[n] - V_d^{Rx}[\infty], n = 1, 2, ..., 5, \tag{2}$$

where $V_d^{Rx}[n]$ is the n-th sampling of received differential signal with FFE enabled. Since there might be DC locc in the channel, the base level, or the steady state of the differential signal may not be exactly -0.9V and thus $V_d^{Rx}[\infty]$, the steady state of the received differential signal must be substracted before using 2. The sampling rate of DFE is the same to the system clock rate. When integrate the DFE unit into the entire channel, appropriate delay time needs to be added to ensure correct functioning of the DFE. In our case, we set our delay time to be 4.2 ns.

where $V_d^{Rx}[n]$ is the n-th sampling of received differential signal with FFE enabled. Since there might be DC locc in the channel, the base level, or the steady state of the differential signal may not be exactly -0.9V and thus $V_d^{Rx}[\infty]$, the steady state of the received differential signal must be substracted before using 2. The sampling rate of DFE is the same to the system clock rate.

However, there are several different delay scheme of DFE. The traditional delay scheme is one delay, as shown in left figure of 27. However, in [9, 10] suggests that only delay half of clock of first symbol may make eye diagram better. For example, Fig. 28a shows the eye diagram using full-delay scheme of DFE, while Fig. 28b shows the eye diagram using half-delay scheme of DFE. One may easily observed that half-delayed DFE may have better performance since the eye remains smooth at maximum and minimum of eye, which causes less jitter. On the other hand, the full-delayed DFE causes abrupt discontinuous right on the sampling time, and thus will be vulnerable to clock jitter.

In following section, we use half-delayed DFE scheme shown in Fig. 28b. The half-delayed feed back symbol can be achieved through utilizing the falling edge of clock, while rising edge of clock is used to sampling the input signal.

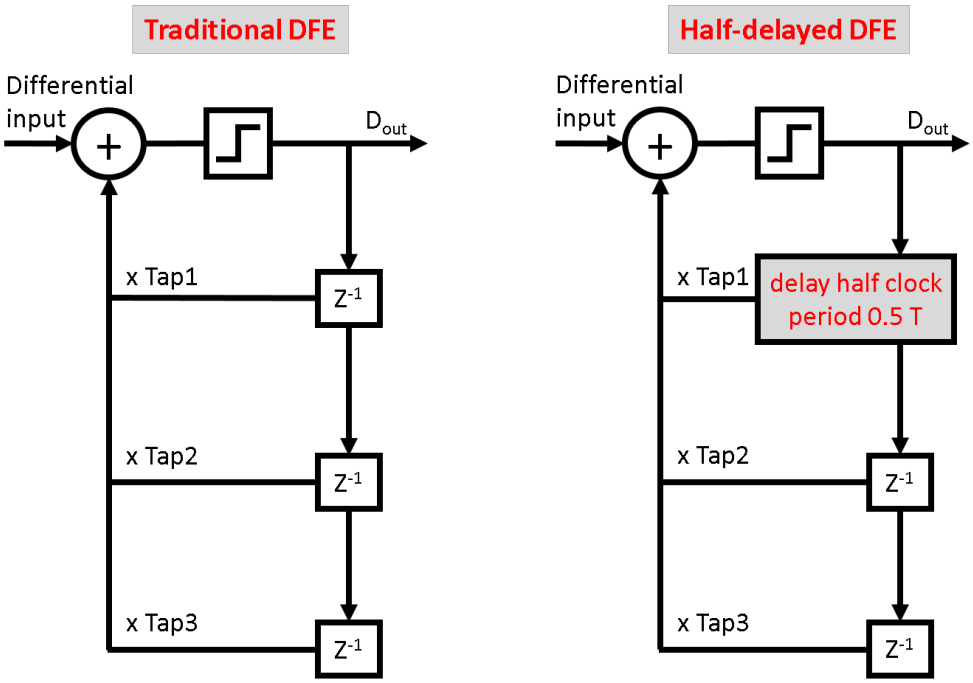
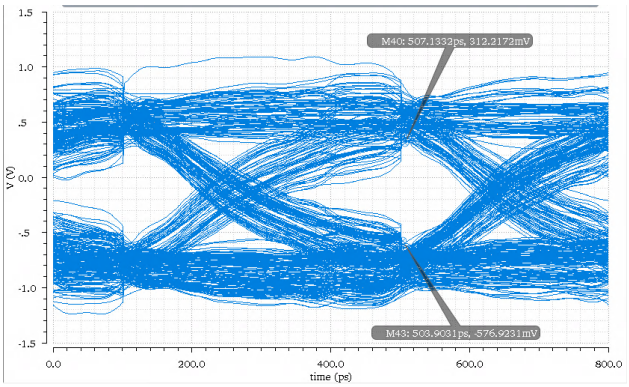
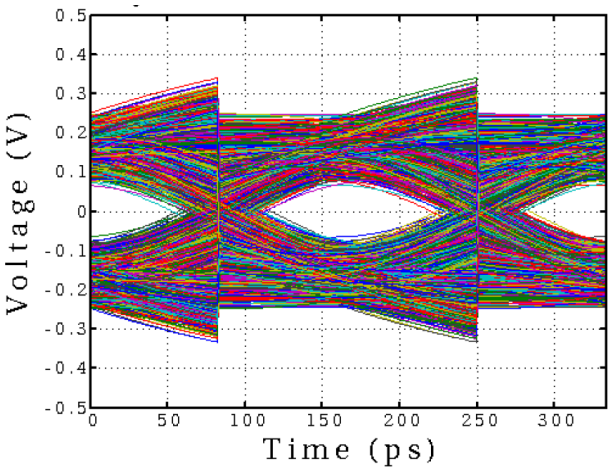


Figure 27: Different delay scheme of DFE.



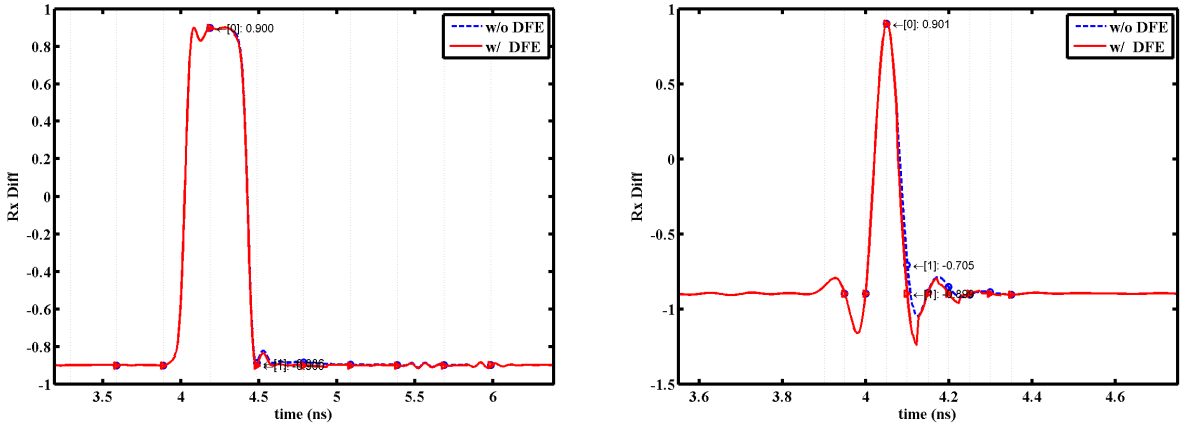
(a) Example eye diagram of full-delay scheme of DFE.



(b) Example eye diagram of half-delay scheme of DFE propsed in [9, 10].

Figure 28: Simulated eye at port A.

In Fig. 22 and Table. 26 shows the sampled differential channel response with FFE enabled. These channel responses can further be used to determine the 5-tap DFE. Fig. 29 shows the pulse response after applying the DFE. We can see that the pulse response abruptly drop or elevated at half of UI, so that the sampled signal will have no post cursors. Table. 26 also listed the sampled signal after DFE.



(a) 3Gb/s.

(b) 20Gb/s.

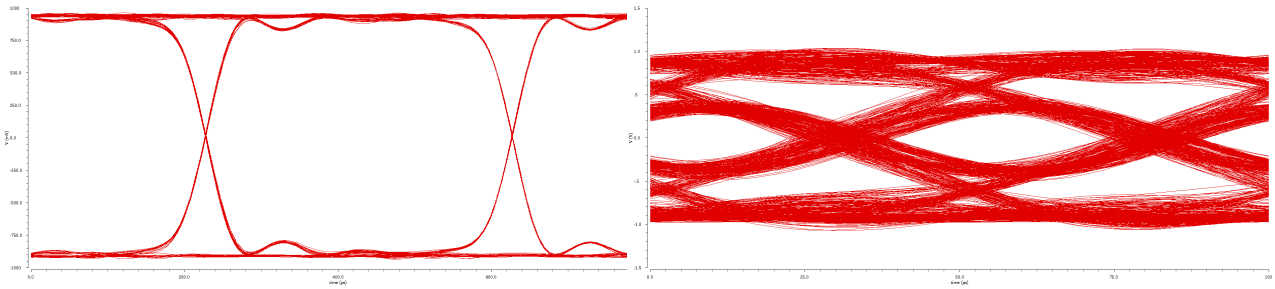
Figure 29: Pulse response after DFE.

6. RESULT

After integrating FFE and DFE into our channel, we simulate our entire system using Verilog AMS again in Cadence Virtuoso. We can see that at 20 Gb/s, our equalization scheme improve the eye height by 10%. This proves that our equalization scheme is effective in widening the eye width and maximum bit rate possible.

Bit Rate	3 Gb/s		20 Gb/s	
Dimension	Width	Height	Width	Height
Port A	95%	55%	Closed	Closed
Port B	99%	91%	66%	71%
Port C	98%	92%	66%	81%

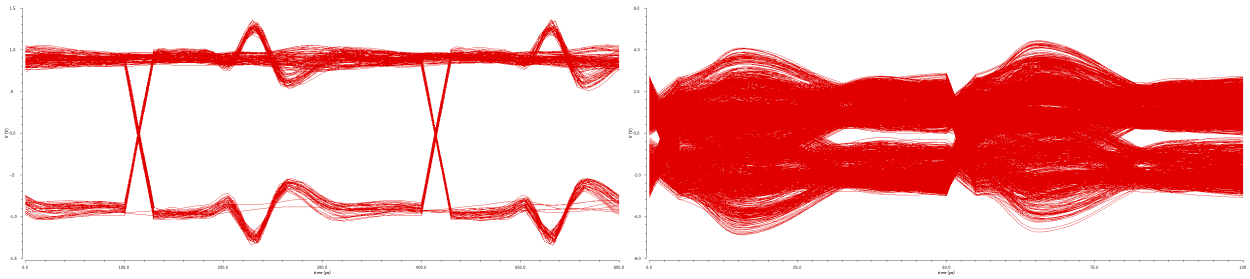
Table 6: Design parameter of PCB trace.



(a) 3 Gb/s

(b) 20 Gb/s.

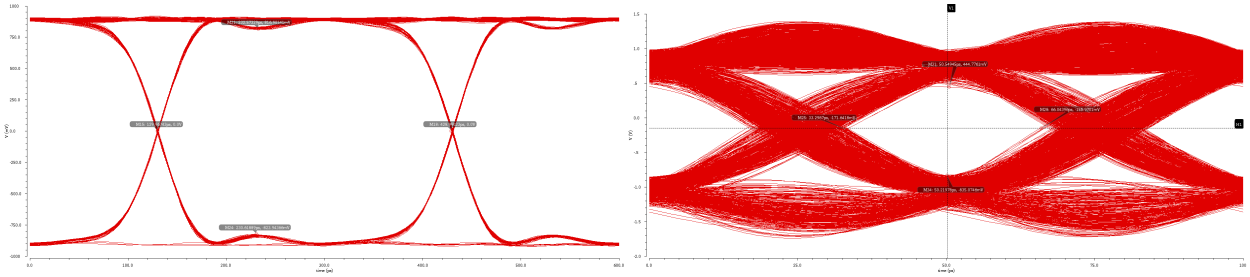
Figure 30: Simulated eye at port B with plain channel, without DFE nor FFE. Replicated from Fig. 19



(a) Simulated eye at 3Gbps at port A.
Eye width: 95% eye height: 55%.

(b) Simulated eye at 20Gbps at port A.
Eye closed.

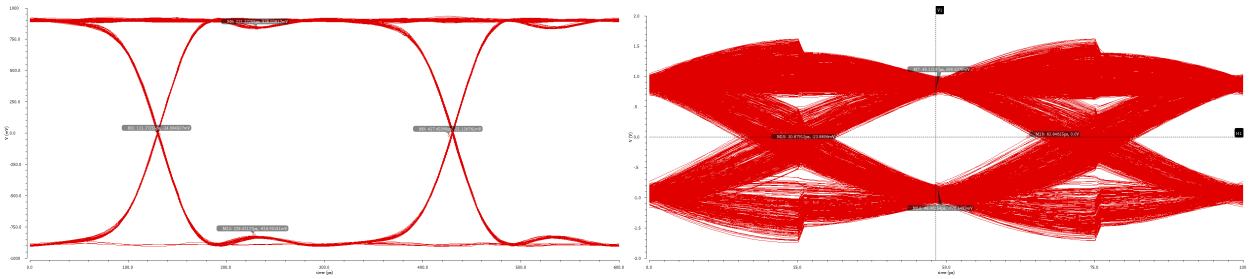
Figure 31: Simulated eye at port A.



(a) Simulated eye at 3Gbps received at port B.
Eye width: 99% eye height: 91%.

(b) Simulated eye at 20Gbps received at port B.
Eye width: 66% eye height: 71%.

Figure 32: Simulated eye at port B.



(a) Simulated eye at 3Gbps received at port C.
Eye width: 98% eye height: 92%.

(b) Simulated eye at 20Gbps received at port C.
Eye width: 66% eye height: 81%.

Figure 33: Simulated eye at port C.

7. CONCLUSION

In this paper, we designed a passive channel with total length over 12 inches. The channel consists of package-to-PCB transition using bonding wire, and top-to-bottom via transition of PCB. This channel can achieve good performance subject to 3Gbps clock rate. With carefully designed FFE and DFE, this channel can further extends to 20Gbps.

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