Mark D Bellows
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Desired Positions:

SOC Verification Engineer
Pre-Si Valid/Verif Engineer
IP Verification
Performance Modelling Engineer
Python Developer for Customer Debug Tools
System Software Validation Engineer
Applications Engineer
Memory Logic Design and Validation Engineer
IP Validation Lead
IP Verification Engineer
Pre-Silicon Verification Engineer
RTL Verification Engineer
Verification Lead
Customer Facing Engineer

Professional Profile

Experienced Computer Hardware Verification/Validation Engineer with 20+ Years Mentoring & Solving Vexing Problems. I have gained skills in Debug of SW/HW (Software (code) and Hardware (logic)) bugs, Cross-Functional Cross-Geographical Team Leadership, Developing / Implementing Tests, Training / Mentoring / Helping. I have experience in various computer languages such as C++, perl, python, VHDL, Verilog and would like to learn more. I have extensively used Linux, Unix & Windows. I like to organize people and methods and solve problems using automation and scripting.

Work History

Intel Corporation, System Validation Engineer 2014-current
International Business Machines (IBM), Advisory Engineer 1992-2014

Target Companies

- Microsoft
- AMD
- Apple
- Qualcomm
- Cadence
- Hewlett Packard
- NVIDIA
- Small - Mid Sized Companies too