MARK D BELLOWS

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Professional Summary

Experienced Computer Hardware Verification/Validation Engineer with 20+ Years Mentoring & Solving Vexing Problems

Skills

- Debug of SW/HW (Software (code) and Hardware (logic)) bugs
- Cross-Functional Team Leadership.
- Developing / Implementing Tests
- Training / Mentoring / Helping

- C++, perl, python VHDL, Verilog, FPGA programming
- Linux, Unix, Windows
- Organizer staff & technical planning and implementing validation projects
- Resolver solves problems using automation

Work History

System Validation Engineer, 09/2014 to Current

Intel Corporation – Hillsboro, OR

- Validated SOC (System on Chip) with internal & external content increasing coverage
- Operating System Validation using off-the-shelf applications
- Established Synthetic Validation using internal and external applications and methods finding 8 hardware bugs in 10 weeks
- System Bring-up using software and hardware to debug issues in record breaking time of 4 weeks these systems contain multiple cores, new functional logic blocks, memory & IO
- Tested concurrency and functionality of many units: GPU, CPU, Memory (DDR3,DDR4, LPDDR4) IPU (Image Processing Unit), GMD (Graphics, Media and Display)
- Field support of debug critical customer issues isolating critical bug at low temperatures
- Found and Triaged power management bugs
- Leading teams across geographies India, Malaysia, Israel
- Proved successful working within tight deadlines and fast-paced atmosphere
- \bullet Monitored and maintained engineering disk space reducing wasted space by 10%
- Created & established methods to reduce defects from previous known problems bugs

Advisory Engineer, 09/1992 to 04/2014

International Business Machines - Rochester, MN

- DDR3/DDR4 memory controller validation for proper function finding logic design bugs
- Virtual system modeling to improve quality modeling processor, memory and IO.
- Silicon Bring-up, lab tool for p/i/z Series, finding firmware and hardware issues.
- Flash memory testing for SSD retention and survivability
- Verification of PCI for correct function and no failures in customer product complex IO

bridge chip had only one logic bug that was fixable by software.

- Power Reduction ESD survivability analysis feeding back predicted failure mechanism for robust design
- Network Processor Design congestion control for reliability and function
- Memory Controller Design for PS3 (Sony/Toshiba/IBM) creating fastest console in market at that time - design was also flexible & used in first super computer to reach sustained 1.0 peta-flops.
- Cache/Coherency controller validation for bug removal finding many bugs in logic of complex memory interfacing unit.
- 32/64Bit FPU validation root causing problems in calculations, optimizations and internal checkers

Projects

Intel Core Gen 14 Processor — Synthetic Validation Lead (North)

Intel Consumer processor validated with new content, validating 8 different IPs, developing novel testing methods

Intel Low Power Gen 11 & Gen 9 Processors — Memory Validation Intel Consumer and Devices Processors - verifying memory controllers and subsystems.

IBM i/p/zSeries PowerPC A25, RS64-II, III, IV - cache controller validation-verification, memory controller design, network processor design, floating point unit verification

Awards

US Patents 22 granted in the areas of Memory and Networking
First Synthetic Graphic Media and Display Tests integrated two different methodologies
Presidential Volunteer Service Award Mentoring youth & teaching LEGO robotic training

Education

Masters of Science: Electrical Engineering
University of Minnesota - Minneapolis, MN
Parallel Processing/ Computer Architecture / Networks / Memory Bus Compression

Bachelors of Science: Electrical & Computer Engineering, Mathematics **Brigham Young University** - Provo, UT

Extracurricular

- Toastmasters (ACB,ALB)
- B.S.A. Wood Badge

LinkedIn

• www.linkedin.com/in/markdbellows