High Level Synthesis

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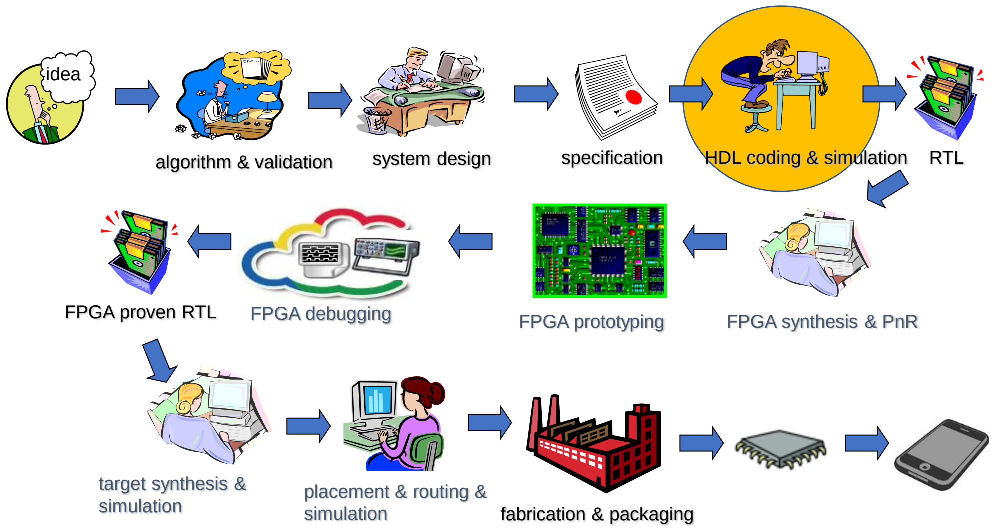
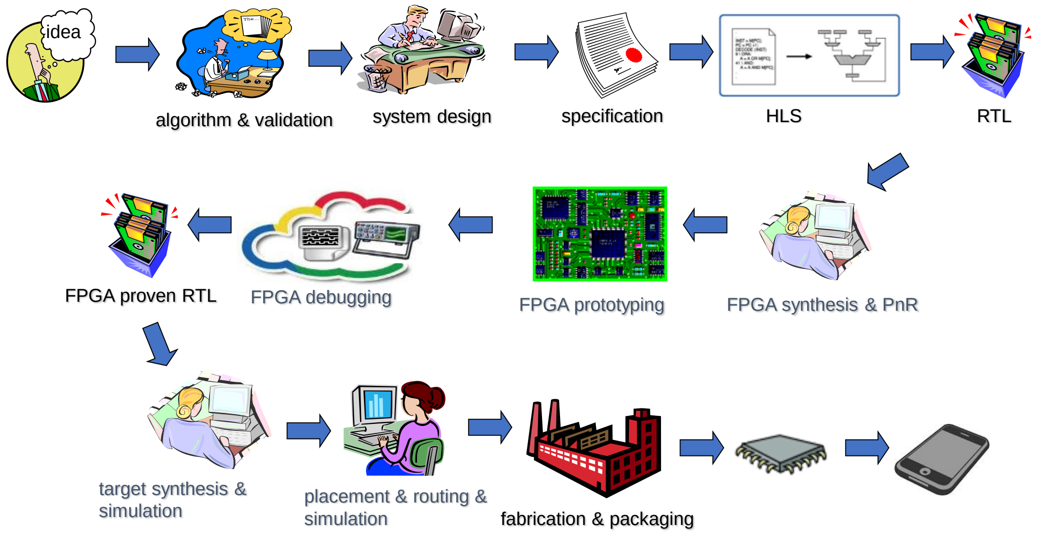
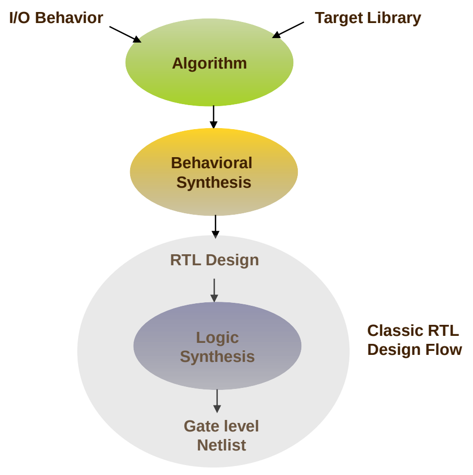


HW design flow: 하드웨어 설계흐름



Behavioral synthesis



Behavioral synthesis is an automated design process that interprets an algorithmic description of a desired behavior and creates hardware that implements that behavior. It is used as part of a behavioral design flow that promises to raise the level of abstraction of the design process.

행위수준 합성은 자동화된 설계 프로세서로써, 행위의 알고리즘 기술을 분석하여 해당 행위를 하드웨어로 구현하는 것임. 행위수준 설계흐름의 한 방법으로써 설계 프로세서의 추상화수준으로 높일 수 있는 방법이다.

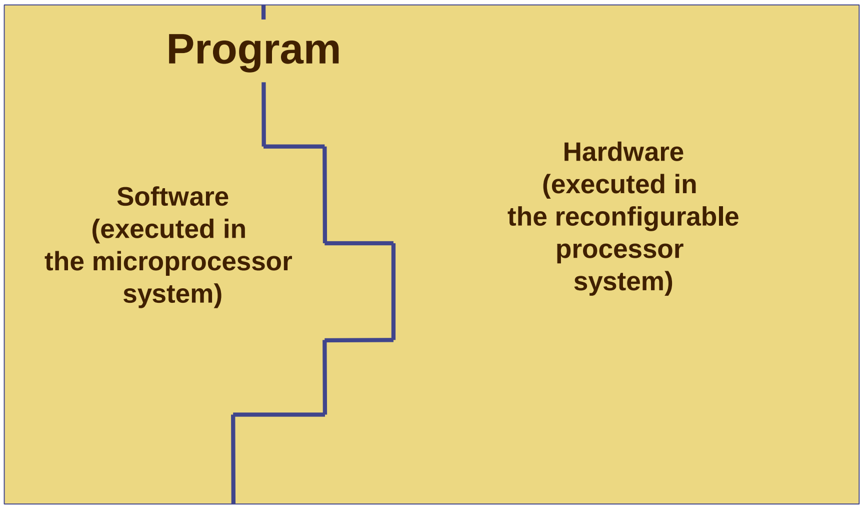
High-level design

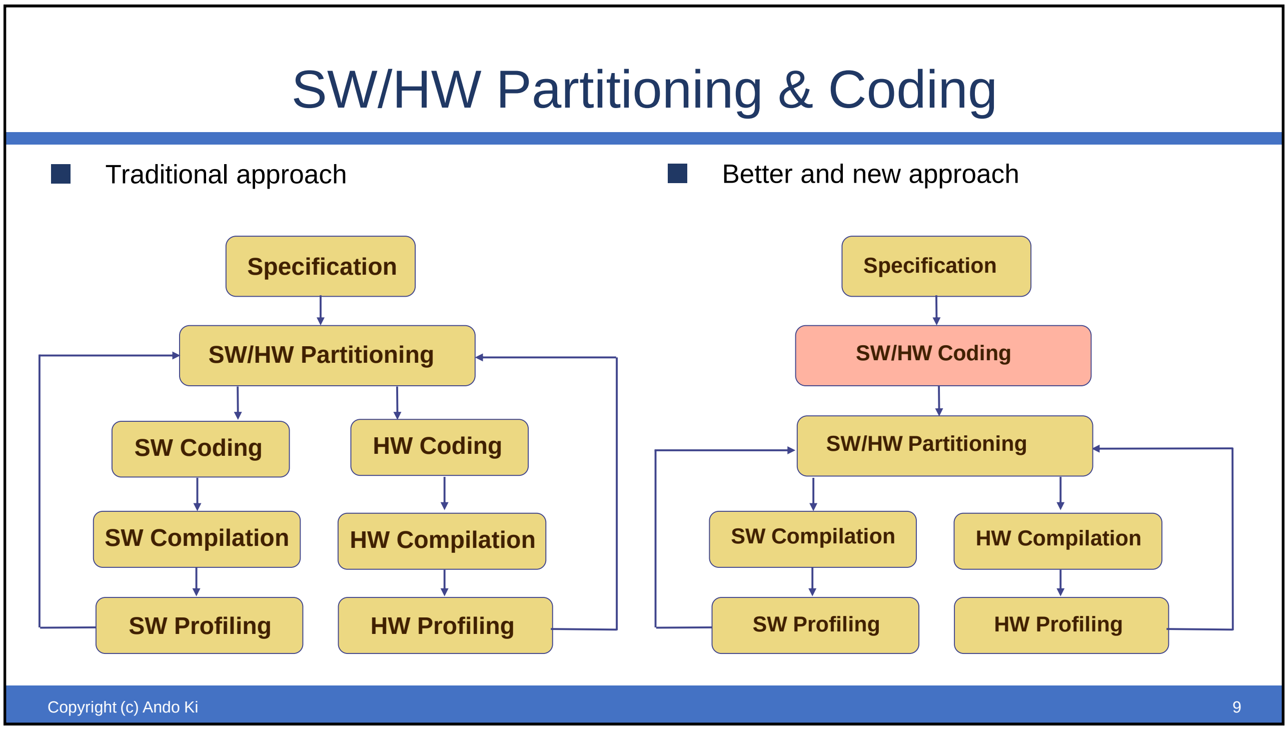
- Higher level of abstraction
  - ▶ 추상화 수준을 높게 할 필요가 있음
- Modeling complex designs
  - ▶ 복잡한 설계를 모델링 할 필요가 있음
- Reduce design efforts
  - ▶ 설계 노력을 줄이는 것이 필요함
- Fast turnaround time
  - ▶ 턴어라운드 시간(한 번 설계를 마치는 시간)을 줄일 필요가 있음
- Technology independence
  - ▶ 구현기술에 독립적일 필요가 있음
- Ease of HW/SW partitioning
  - ▶ HW/SW 분할을 쉽게할 필요가 있음

HLS: High-level synthesis

- High-level synthesis (HLS),
  - sometimes referred to as C synthesis, electronic system-level (ESL) synthesis, algorithmic synthesis, or behavioral synthesis,
  - is an automated design process that interprets an algorithmic description of a desired behavior and creates digital hardware that implements that behavior.
    - ➲ Behavioral synthesis

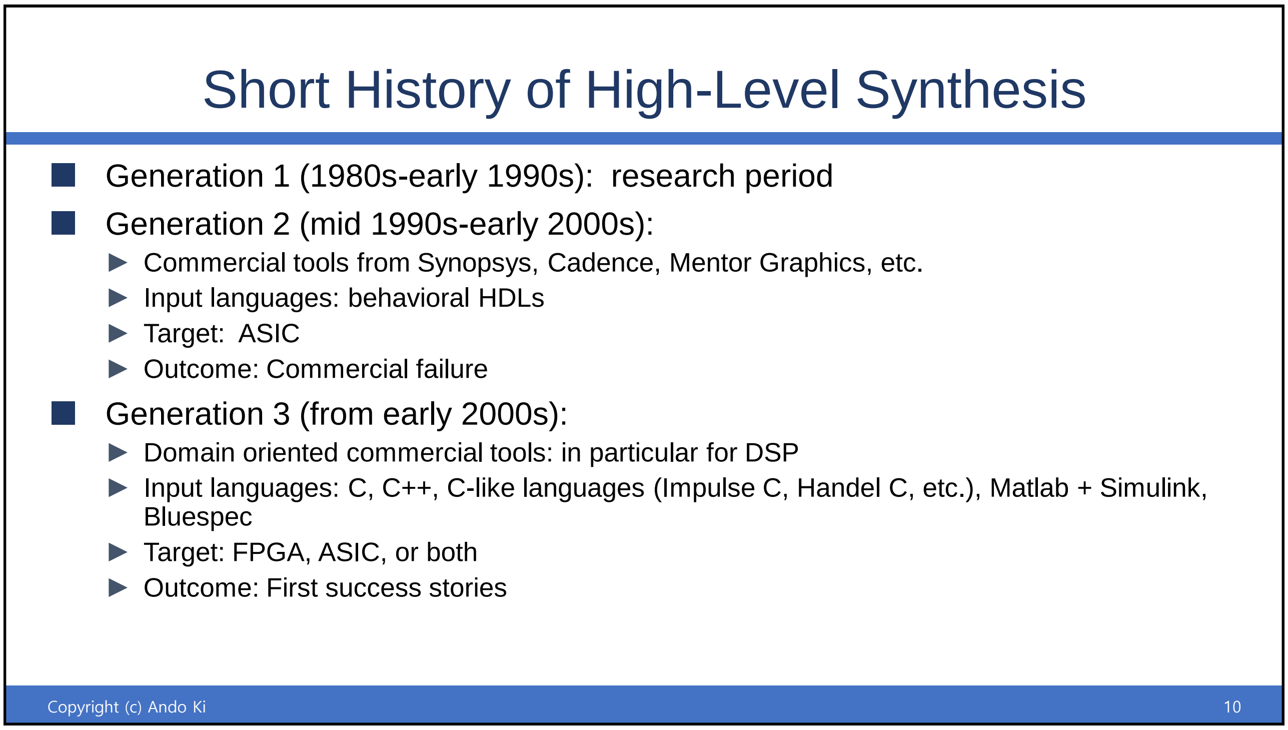
HW/SW partitioning


Program
Software (executed in the microprocessor system)
Hardware (executed in the reconfigurable processor system)



SW/HW Partitioning & Coding

- Traditional approach
- Better and new approach

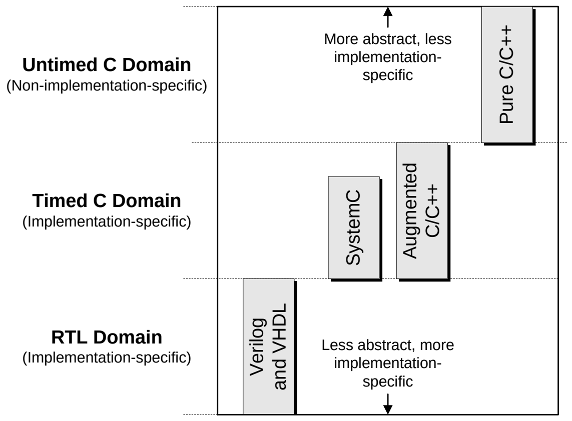


Short History of High-Level Synthesis

- Generation 1 (1980s-early 1990s): research period
- Generation 2 (mid 1990s-early 2000s):
  - Commercial tools from Synopsys, Cadence, Mentor Graphics, etc.
  - Input languages: behavioral HDLs
  - Target: ASIC
  - Outcome: Commercial failure
- Generation 3 (from early 2000s):
  - Domain oriented commercial tools: in particular for DSP
  - Input languages: C, C++, C-like languages (Impulse C, Handel C, etc.), Matlab + Simulink, Bluespec
  - Target: FPGA, ASIC, or both
  - Outcome: First success stories

Hardware-Oriented High-Level Languages

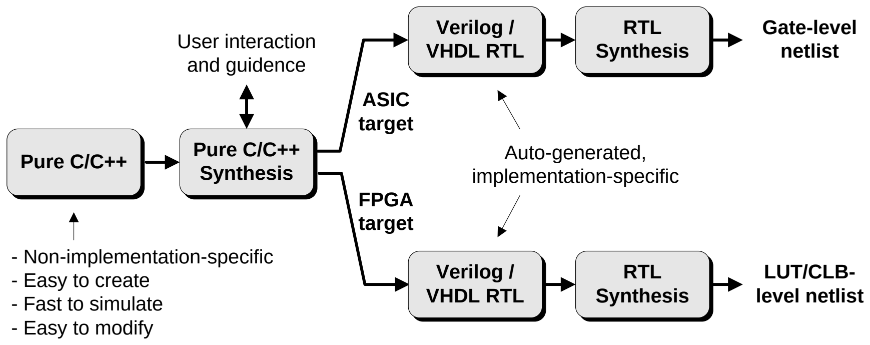
- C-Based System level languages
  - Commercial
    - Handel C -- Celoxica Ltd.
    - Impulse C -- Impulse Accelerated Technologies
    - Carte C – SRC Computers
    - SystemC -- The Open SystemC Initiative
  - Research
    - Streams-C -- Los Alamos National Laboratory
    - SA-C -- Colorado State University, University of California, Riverside, Khoral Research, Inc.
    - SpecC – University of California, Irvine and SpecC Technology Open Consortium


Untimed C Domain
(Non-implementation-specific)
Timed C Domain
(Implementation-specific)
RTL Domain
(Implementation-specific)
More abstract, less implementation-specific
Less abstract, more implementation-specific
Pure C/C++
Augmented C/C++
SystemC
Verilog and VHDL

Other High-Level Design Flows

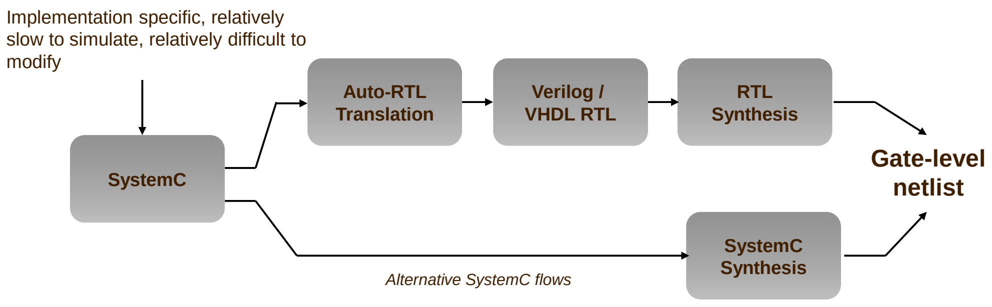
- Matlab-based
  - AccelChip DSP Synthesis -- AccelChip
  - System Generator for DSP -- Xilinx
- GUI Data-Flow based
  - Corefire -- Annapolis Microsystems
- Java-based
  - Commercial
    - Forge -- Xilinx
  - Research
    - JHDL – Brigham Young University

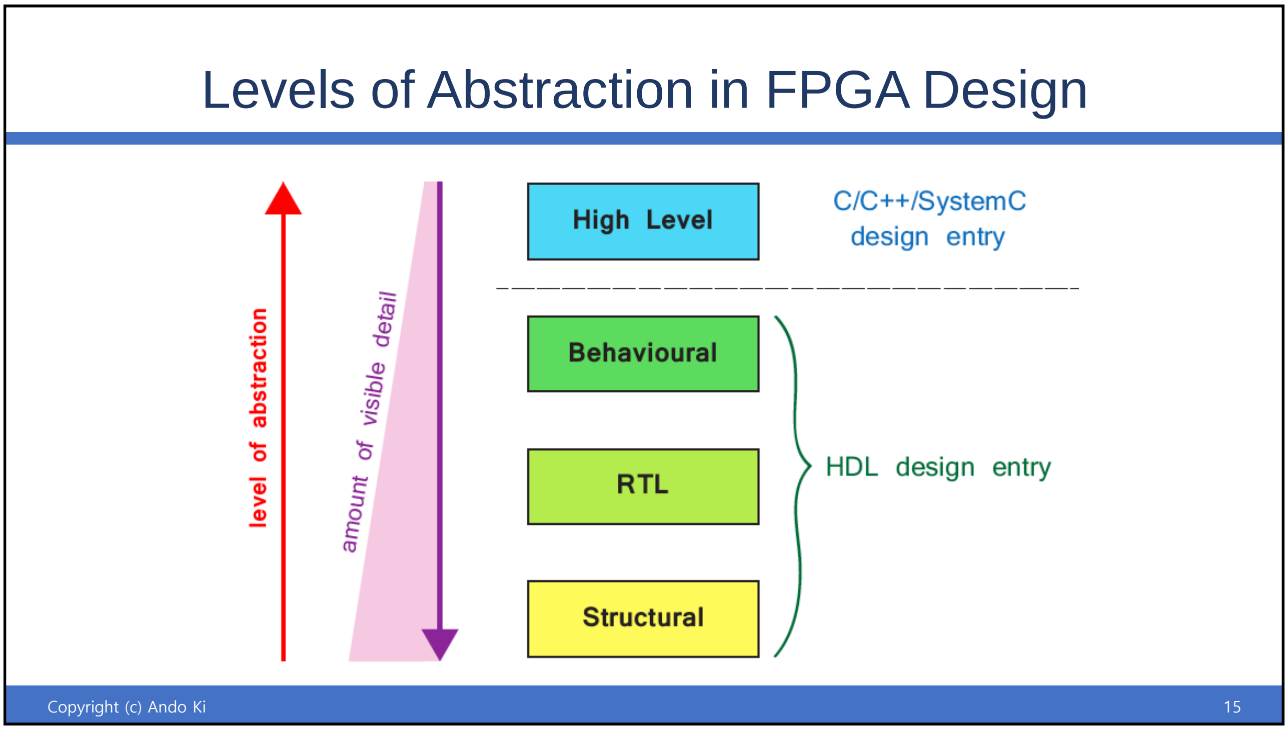
Pure Untimed C/C++ Design Flow



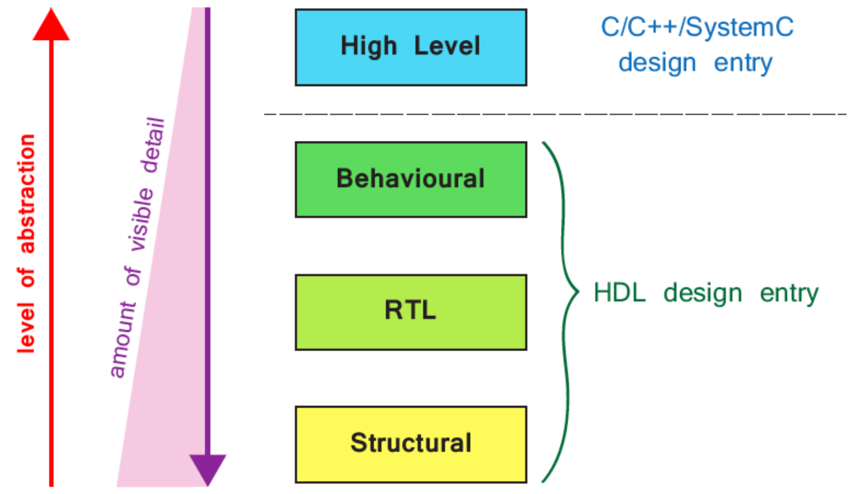
E.g., Mentor Graphics Catapult C automatically converts un-timed C/C++ descriptions into synthesizable RTL.

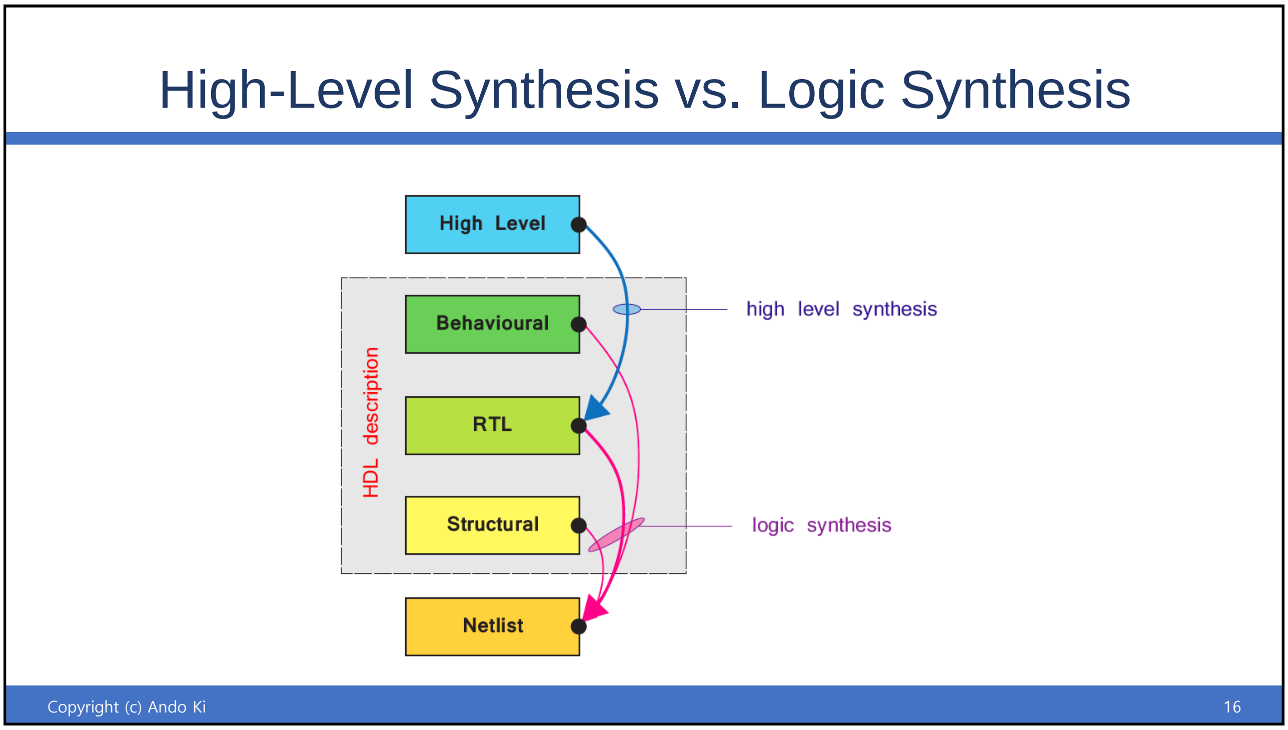
SystemC -based design-flow alternatives


Implementation specific, relatively slow to simulate, relatively difficult to modify
SystemC
Auto-RTL Translation
Verilog / VHDL RTL
RTL Synthesis
Gate-level netlist
SystemC Synthesis
Alternative SystemC flows

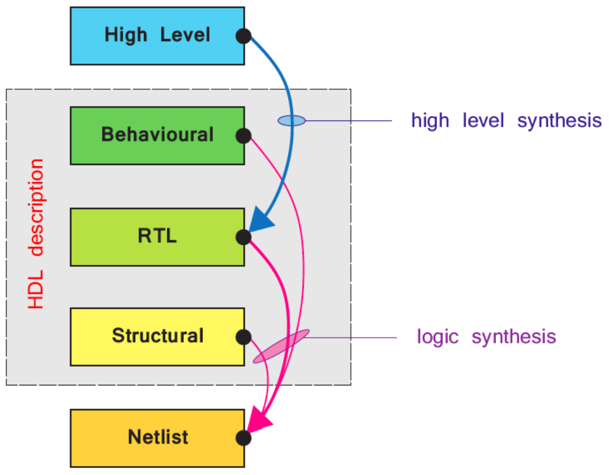


Levels of Abstraction in FPGA Design

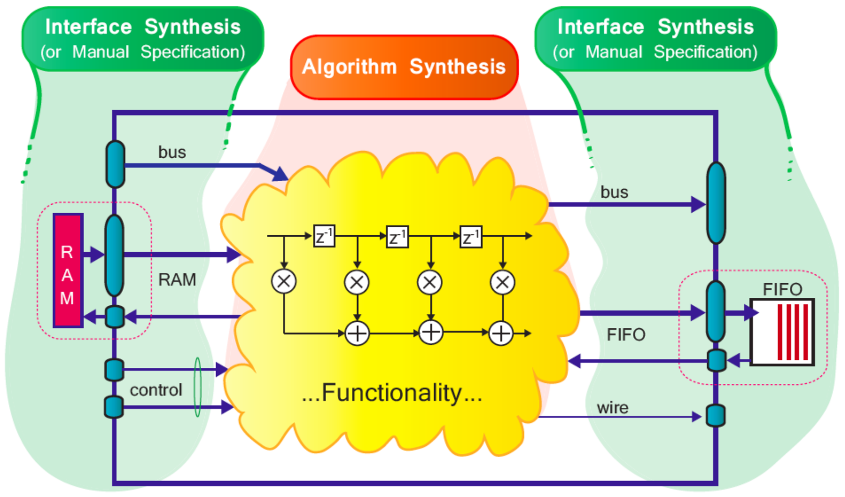




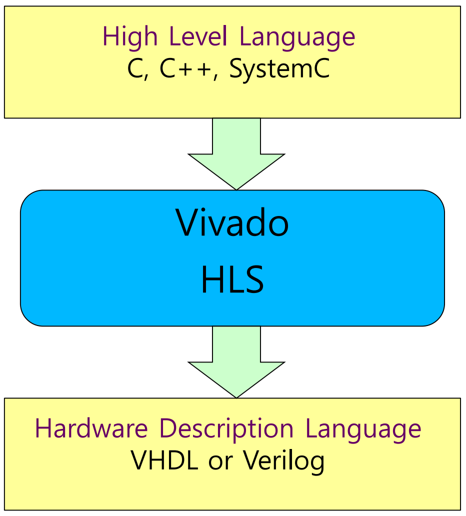
High-Level Synthesis vs. Logic Synthesis



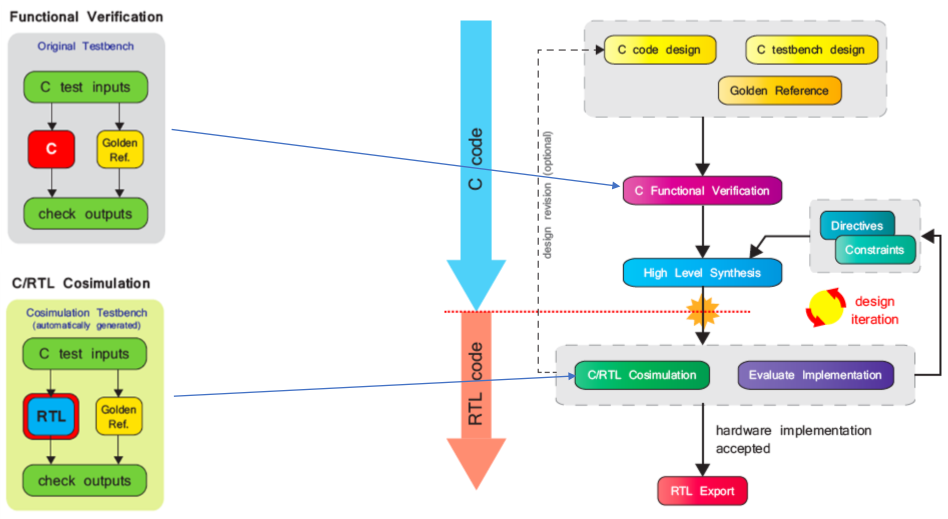
Algorithm and Interface Synthesis



Xilinx Vivado HLS



Xilinx Vivado HLS design flow



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- Vivado Design Suite User Guide, High-Level Synthesis, UG902
- Introduction to FPGA Design with Vivado High-Level Synthesis, UG998
- A Zynq Accelerator for Floating Point Matrix multiplication Designed with Vivado HLS, XAPP1170
- The Design Warrior’s Guide to FPGAs Devices, Tools, and Flows.