

# Install Vivado

2022.02.17



# Xilinx Vivado Design Suite

- Vivado is a tool we can use for writing, simulating and implementing Verilog HDL projects.
- This tutorial will explain how to install vivado, create a simple project and simulate it(windows)

# Download Vivado

- Visit Xilinx website to download vivado
  - <https://www.xilinx.com/support/download.html>
- Here, select a version and download
- This tutorial will explain using 2021.1 version
- You have to create a Xilinx account to install Vivado

 Xilinx Unified Installer 2021.1: Windows Self Extracting Web Installer

(EXE - 226.04 MB)

MD5 SUM Value : 6bc01c7518717bea1c4aefcfc90d6f1b

Download Verification 

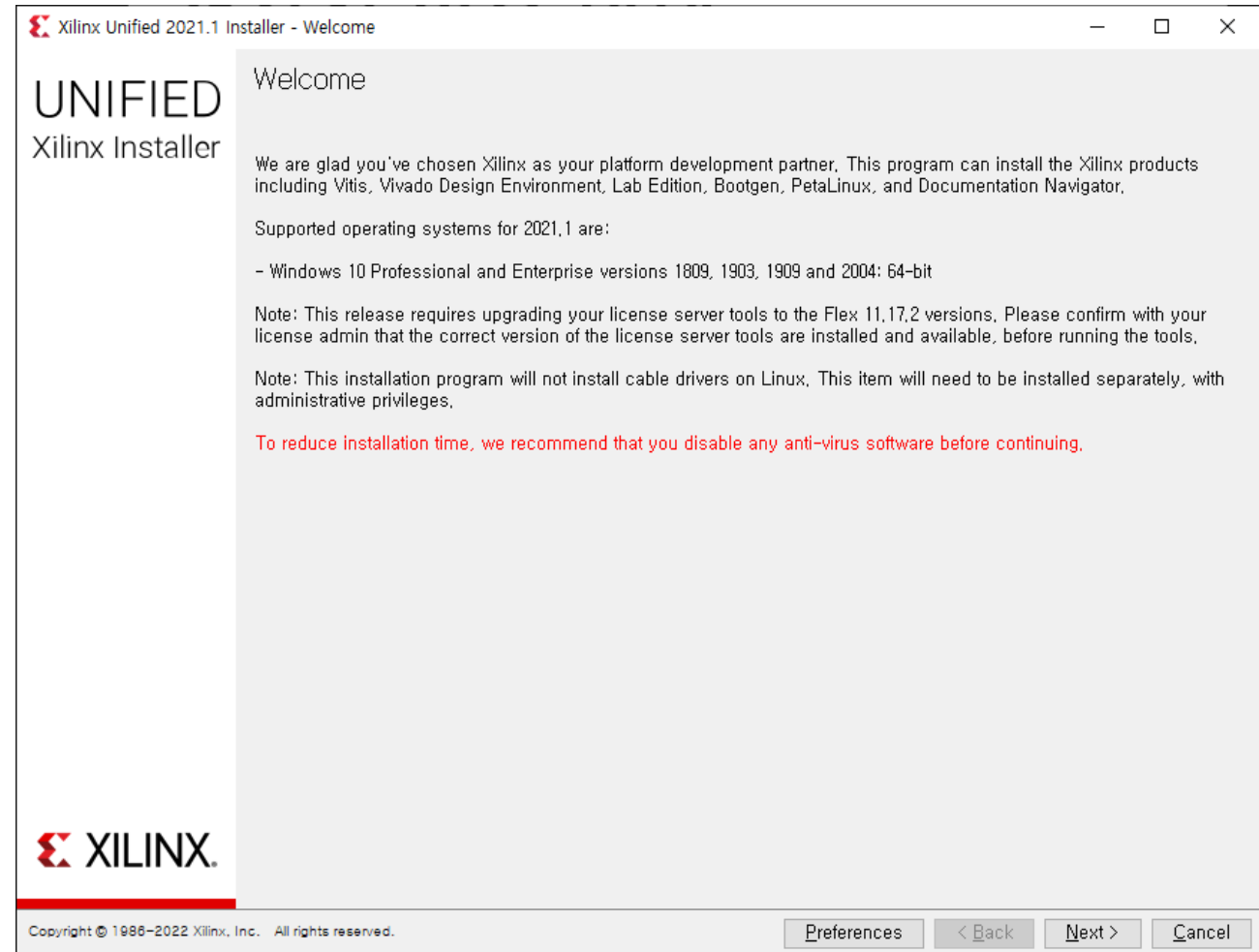
Digests

Signature

Public Key

# Xilinx Vivado Design Suite

- After downloading, run the downloaded file



# Xilinx Vivado Design Suite

- Enter your Xilinx account
- Select download and install now
- Click next

The screenshot shows the 'Xilinx Unified 2021.1 Installer - Select Install Type' window. The title bar includes the Xilinx logo and the text 'Xilinx Unified 2021.1 Installer - Select Install Type'. The window has a dark header bar with the text 'Select Install Type' and the Xilinx logo. Below the header, a message states: 'Please select install type and provide your Xilinx.com E-mail Address and password for authentication.' The main content area is divided into three sections. The first section, 'User Authentication', contains a text prompt: 'Please provide your Xilinx user account credentials to download the required files. If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).' Below this are two input fields: 'E-mail Address' and 'Password'. The second section, 'Download and Install Now', is selected with a radio button. It contains the text: 'Select your desired device and tool installation options and the installer will download and install just what is required.' The third section, 'Download Image (Install Separately)', is unselected with a radio button. It contains the text: 'The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.' At the bottom of the window, there is a footer with the text 'Copyright © 1986-2022 Xilinx, Inc. All rights reserved.' and three buttons: '< Back', 'Next >', and 'Cancel'.

Xilinx Unified 2021.1 Installer - Select Install Type

Select Install Type

Please select install type and provide your Xilinx.com E-mail Address and password for authentication.

User Authentication

Please provide your Xilinx user account credentials to download the required files.  
If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).

E-mail Address

Password

☒ Download and Install Now

Select your desired device and tool installation options and the installer will download and install just what is required.

☐ Download Image (Install Separately)

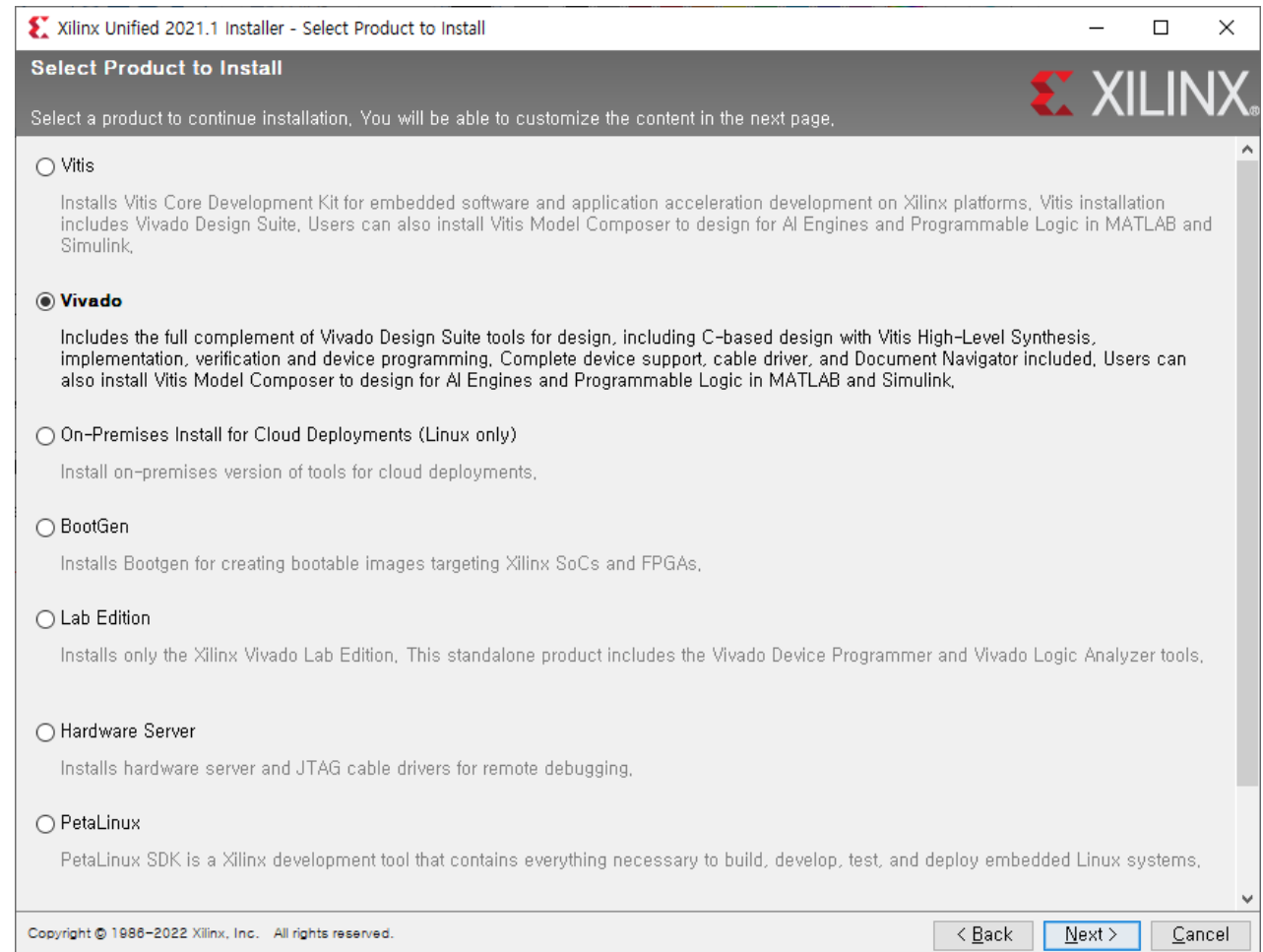
The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.

Copyright © 1986-2022 Xilinx, Inc. All rights reserved.

< Back Next > Cancel

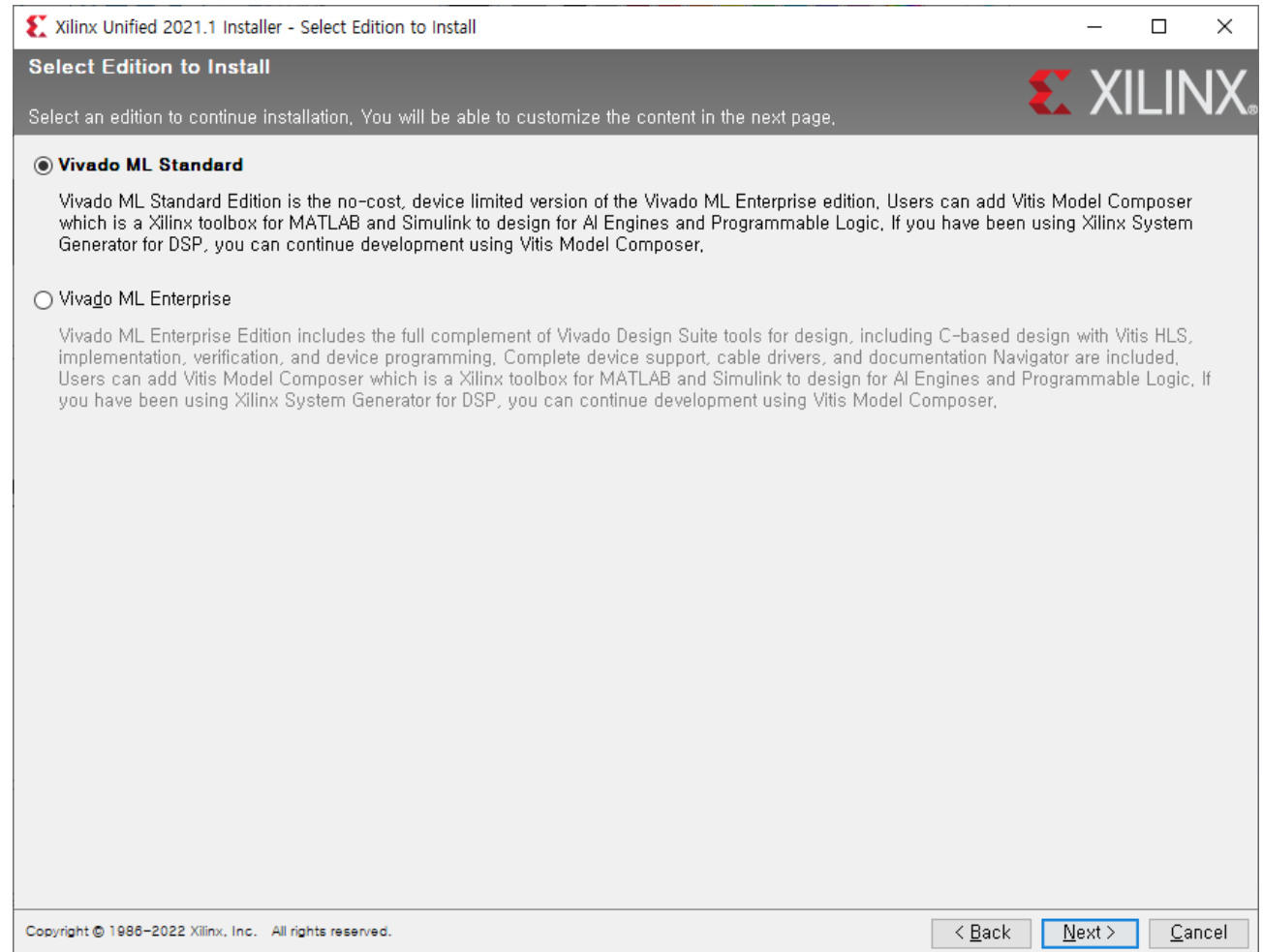
# Xilinx Vivado Design Suite

- Select Vivado, click next



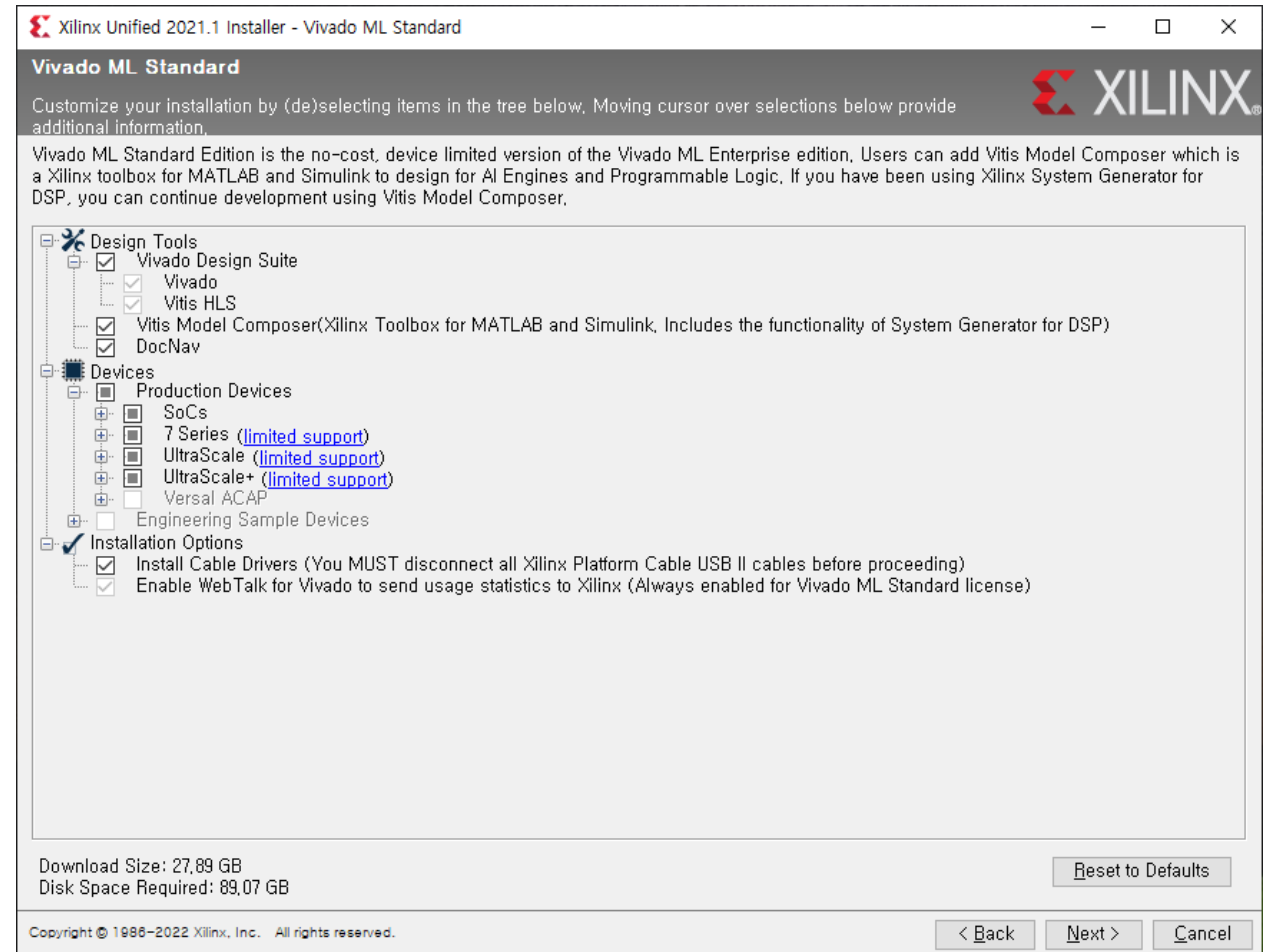
# Xilinx Vivado Design Suite

- Select Vivado ML Standard, click next



# Xilinx Vivado Design Suite

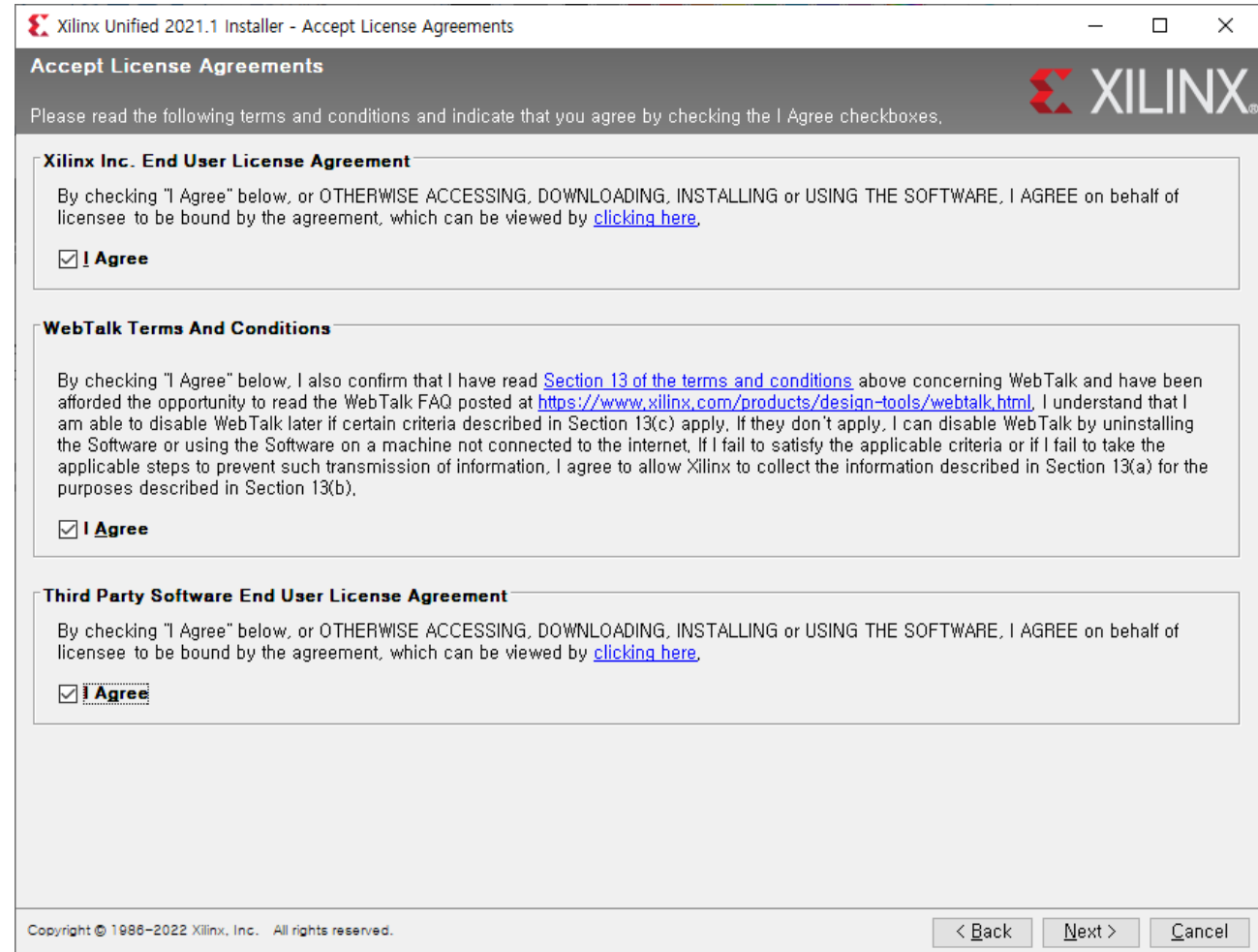
- Click next





# Xilinx Vivado Design Suite

- Select I agree, and click next



Xilinx Unified 2021.1 Installer - Accept License Agreements

**Accept License Agreements**

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

**Xilinx Inc. End User License Agreement**

By checking "I Agree" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ **I Agree**

**WebTalk Terms And Conditions**

By checking "I Agree" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

☒ **I Agree**

**Third Party Software End User License Agreement**

By checking "I Agree" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

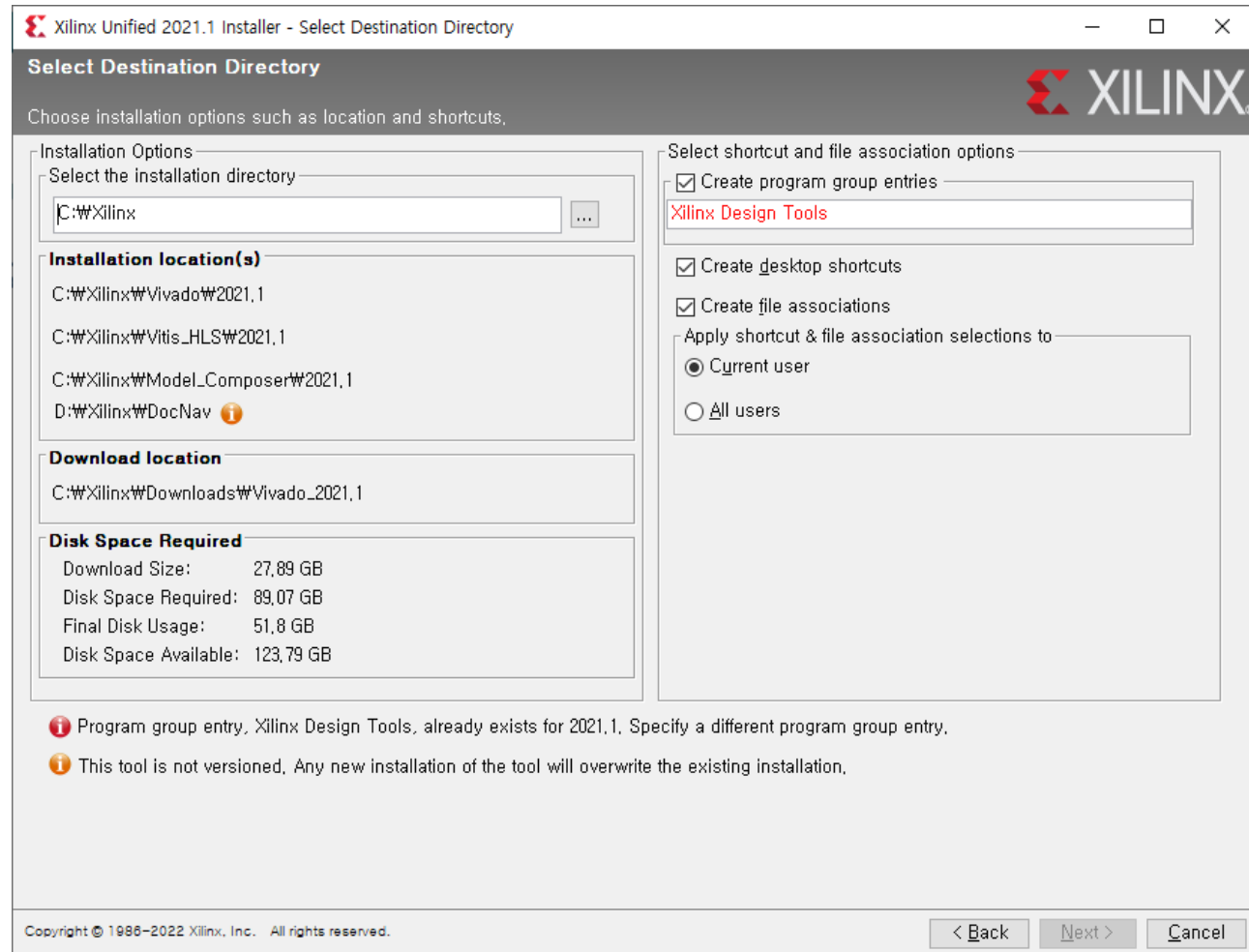
☒ **I Agree**

Copyright © 1988–2022 Xilinx, Inc. All rights reserved.

< Back Next > Cancel

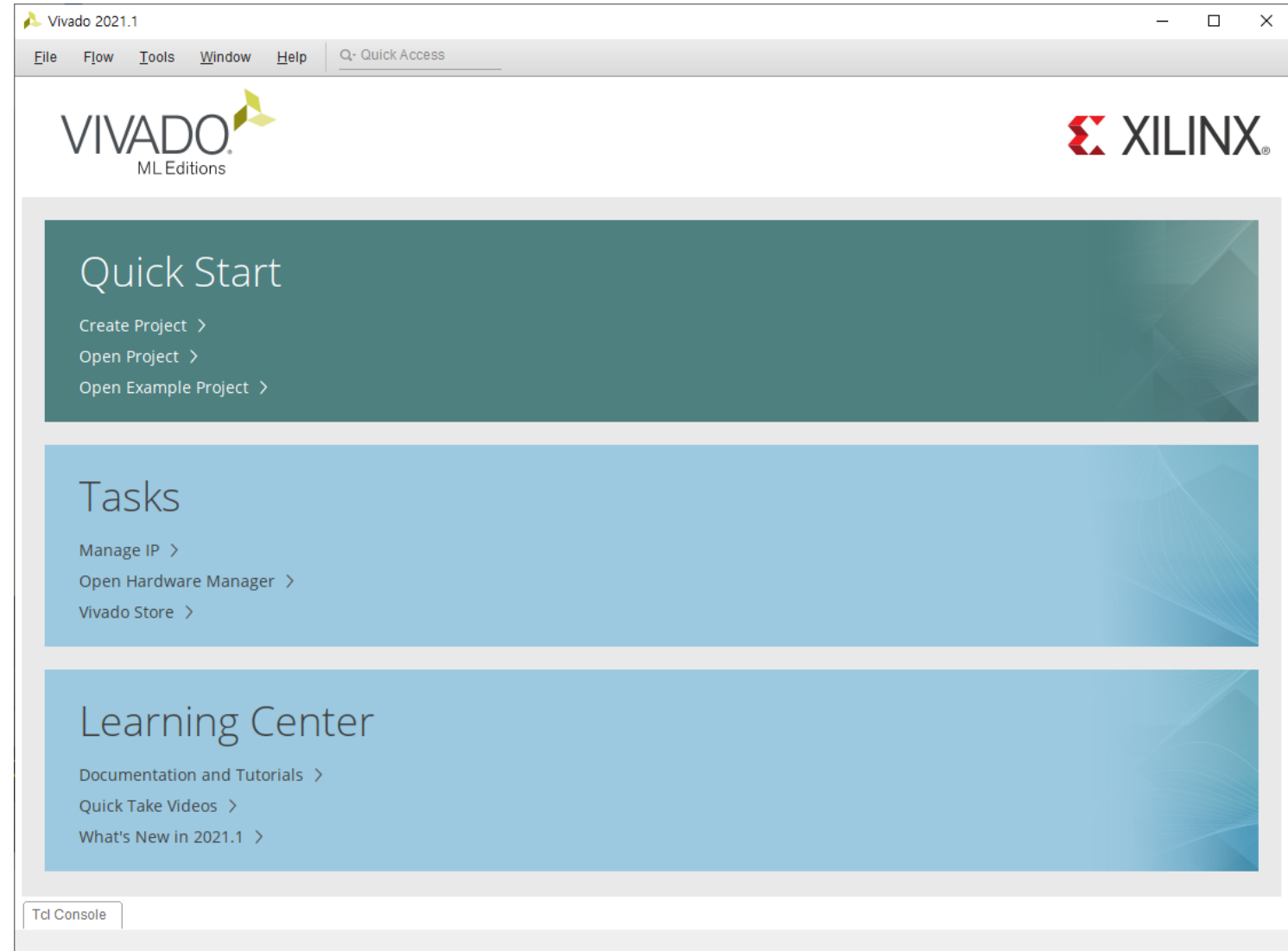
# Xilinx Vivado Design Suite

- Select installation directory, and click next
- After this, it will take quite long to finish installing



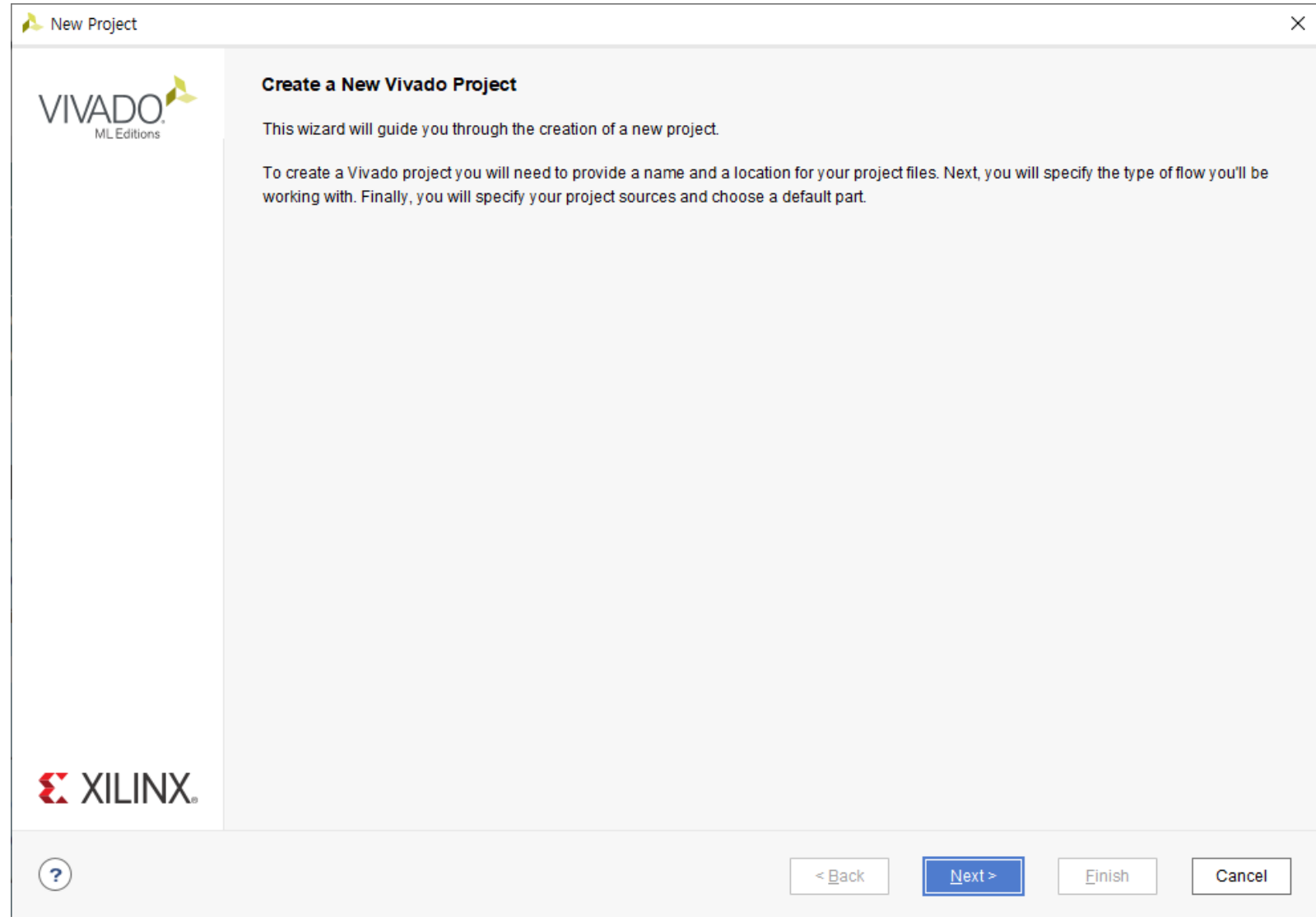
# Creating an example project

- Run Vivado
- Click Create Project



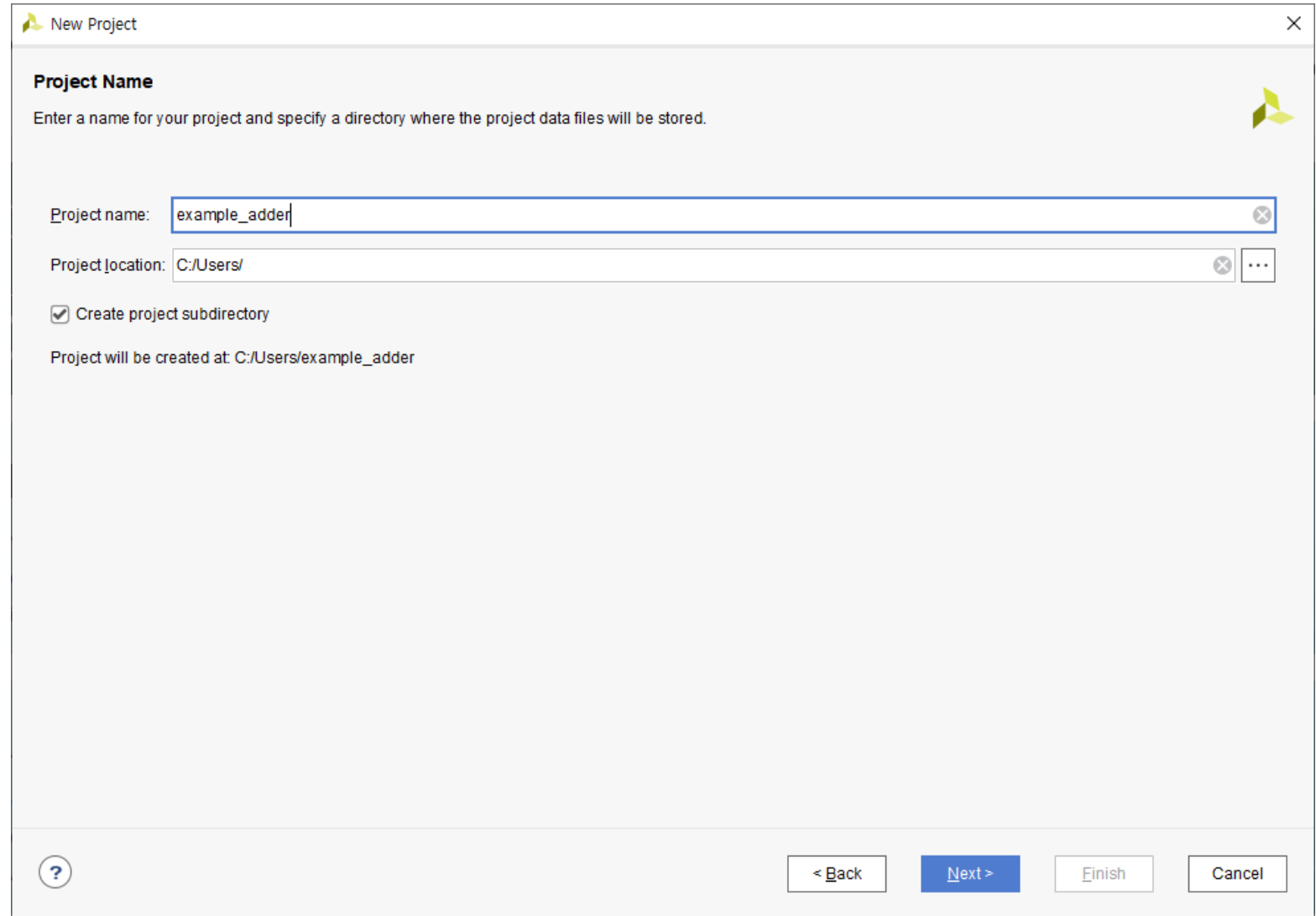
# Creating an example project

- Click next



# Creating an example project

- Select project name and location
- Click next



The screenshot shows a 'New Project' dialog box with a title bar containing a green triangle icon and a close button. The main area is titled 'Project Name' and contains the instruction: 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there are two input fields: 'Project name:' with the text 'example\_adder' and 'Project location:' with the text 'C:/Users/'. To the right of the location field is a button with three dots. Below the input fields is a checked checkbox labeled 'Create project subdirectory'. At the bottom of the main area, it says 'Project will be created at: C:/Users/example\_adder'. The bottom of the dialog box features a help icon (question mark in a circle) on the left and four buttons on the right: '< Back', 'Next >' (highlighted in blue), 'Finish', and 'Cancel'.

New Project

**Project Name**

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: example\_adder

Project location: C:/Users/

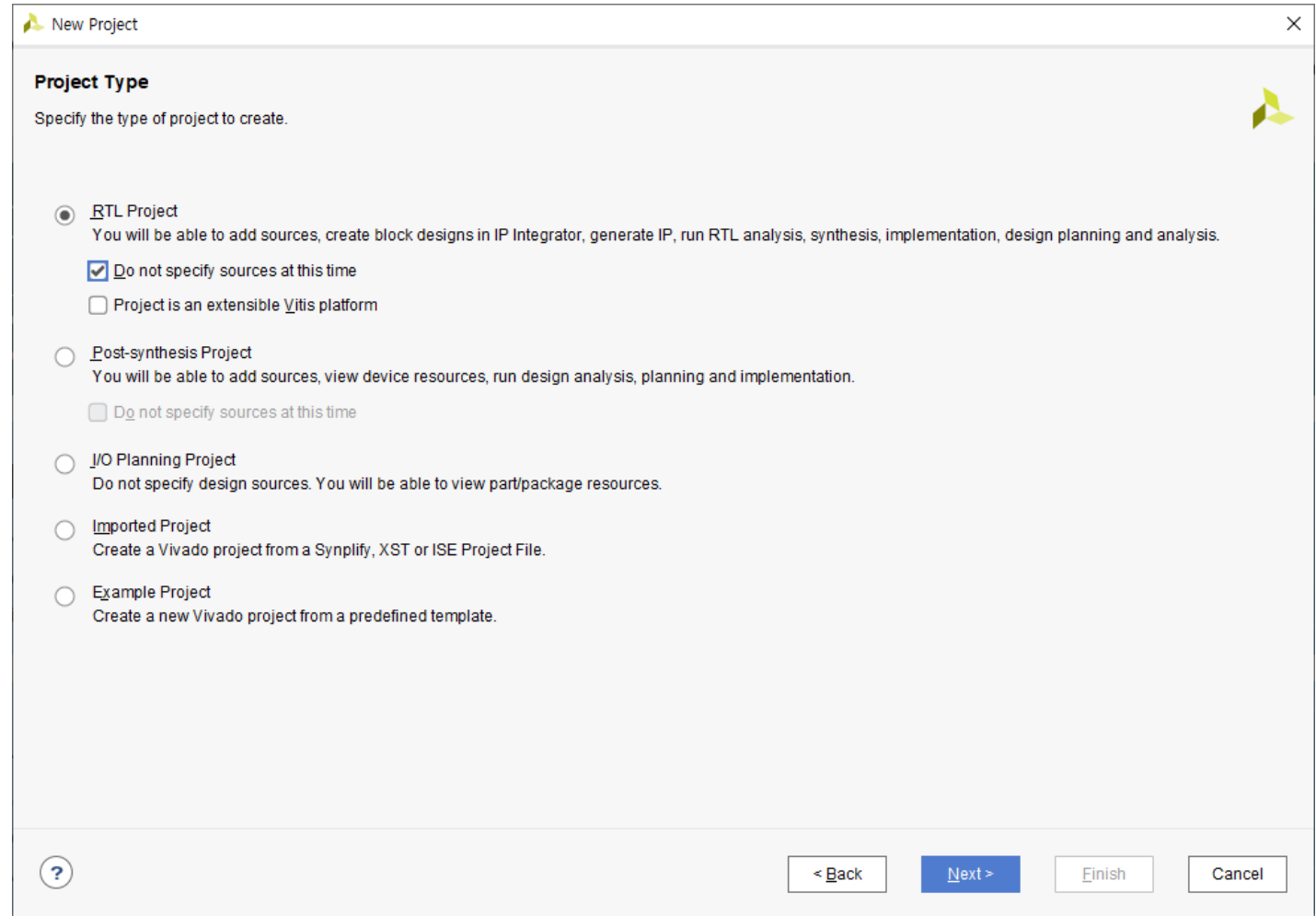
☒ Create project subdirectory

Project will be created at: C:/Users/example\_adder

? < Back Next > Finish Cancel

# Creating an example project

- Click next



**New Project**

**Project Type**  
Specify the type of project to create.


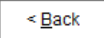
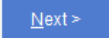
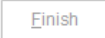
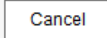
☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
☒ Do not specify sources at this time  
☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.  
☐ Do not specify sources at this time

☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**  
Create a new Vivado project from a predefined template.

# Creating an example project

- This is board selection
- For now, we will only simulate the design.
- Click next

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All

Package: All

Temperature: All

Family: All

Speed: All

Static power: All

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE
xc7vx415tffv1927-3	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-2	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-2L	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160	48	0
xc7vx485tffg1157-3	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-2	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-2L	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-1	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1158-3	1158	350	303600	607200	1030	0	2800	48	0

?

< Back

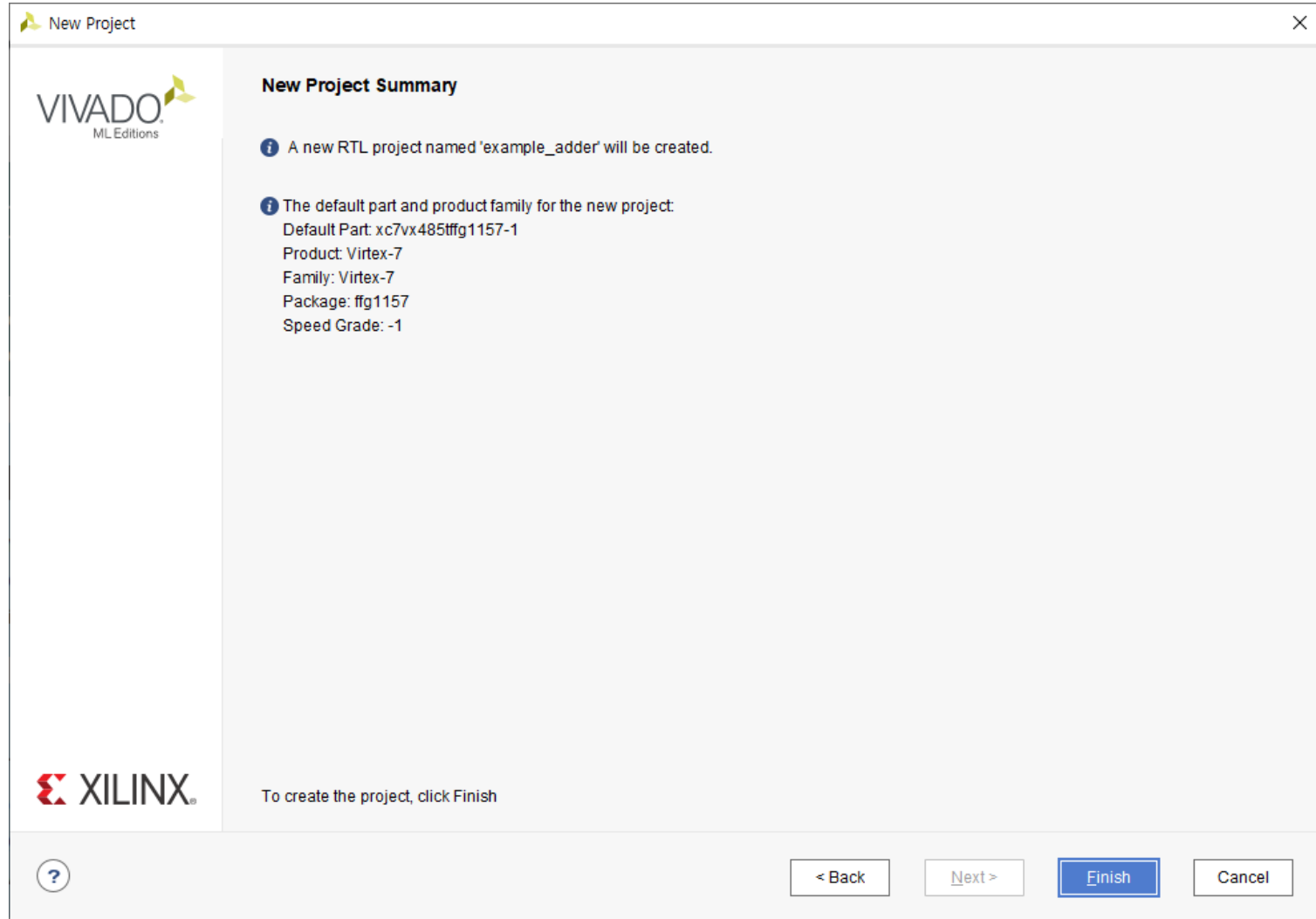
Next >

Finish

Cancel

# Creating an example project

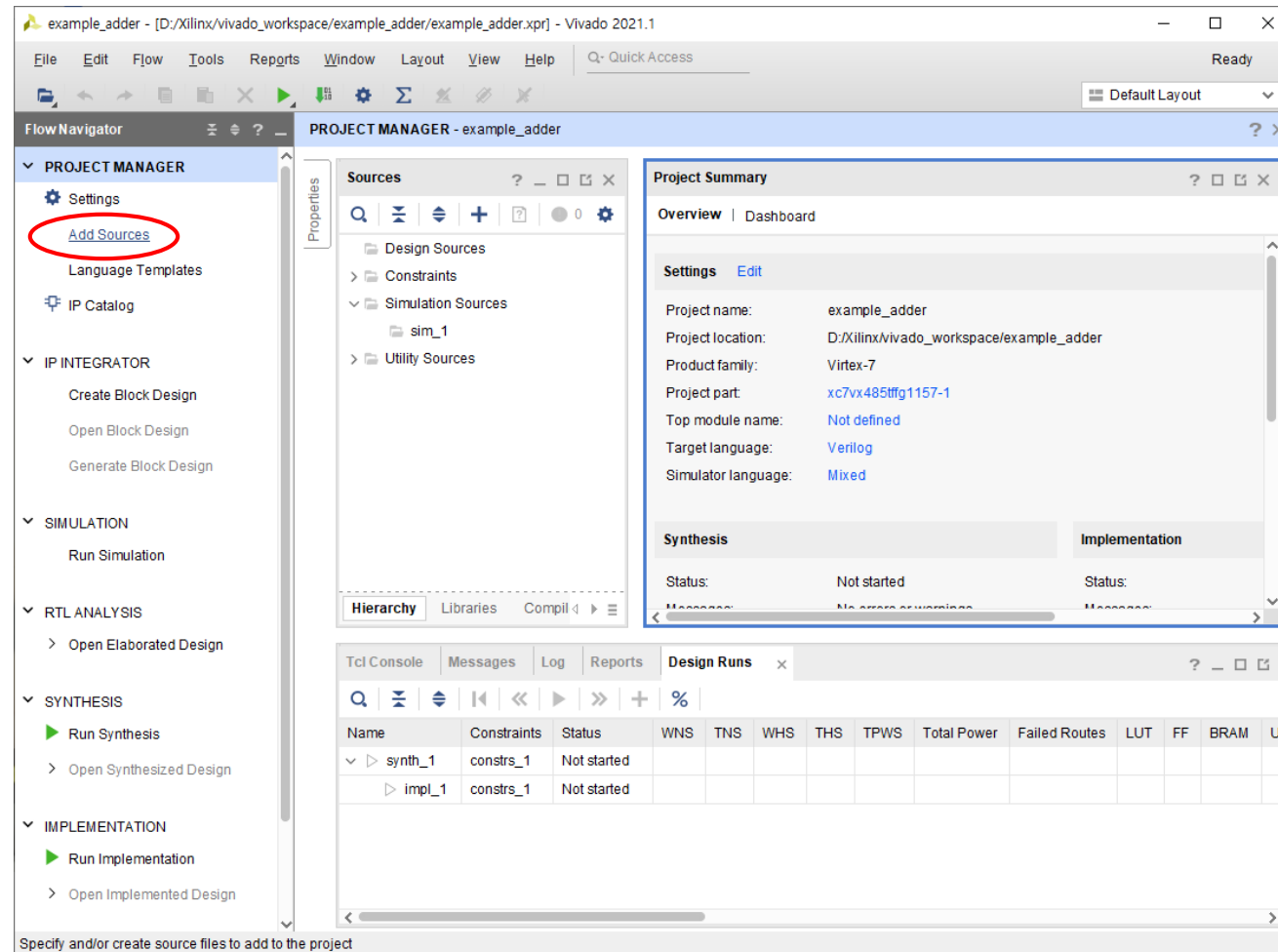
- Click finish





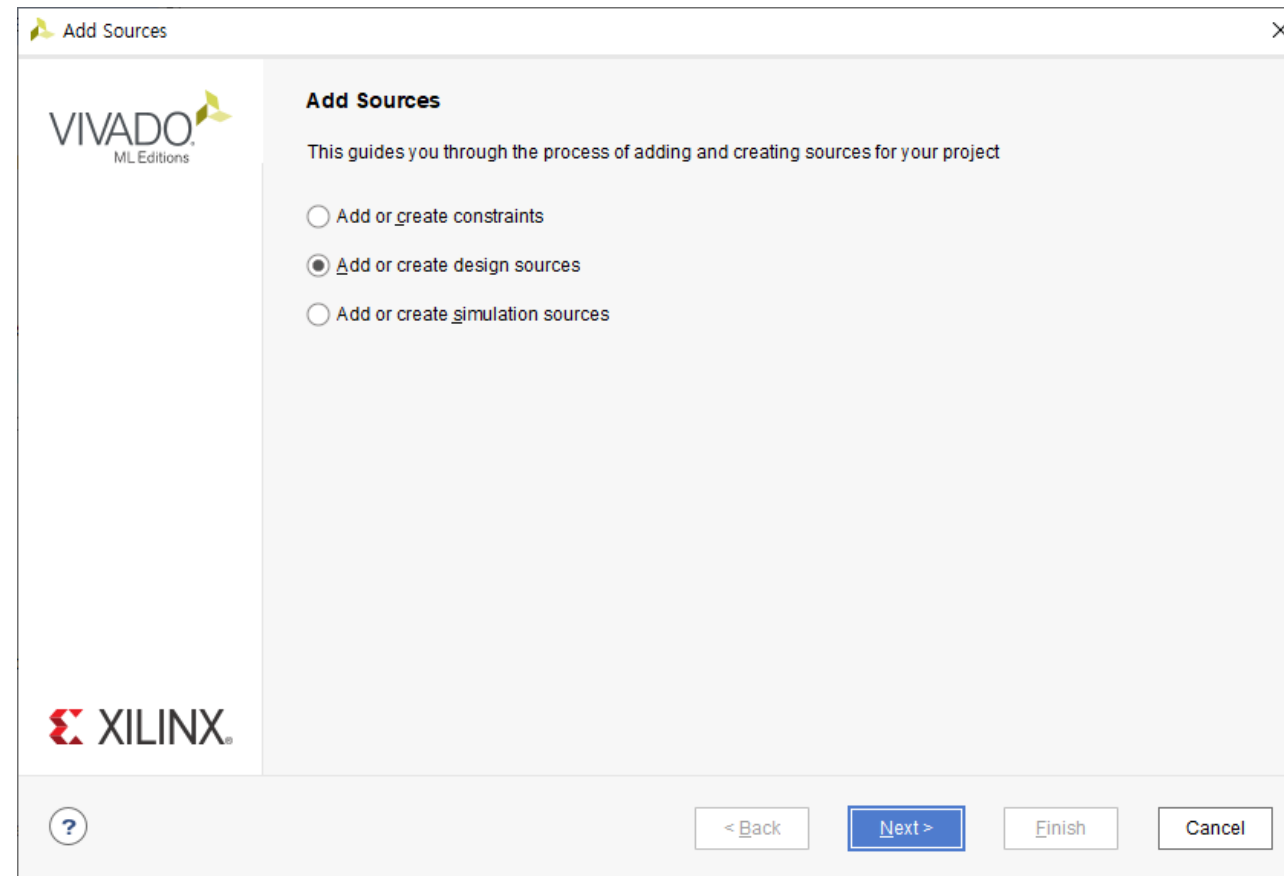
# Creating an example project

- Click add sources



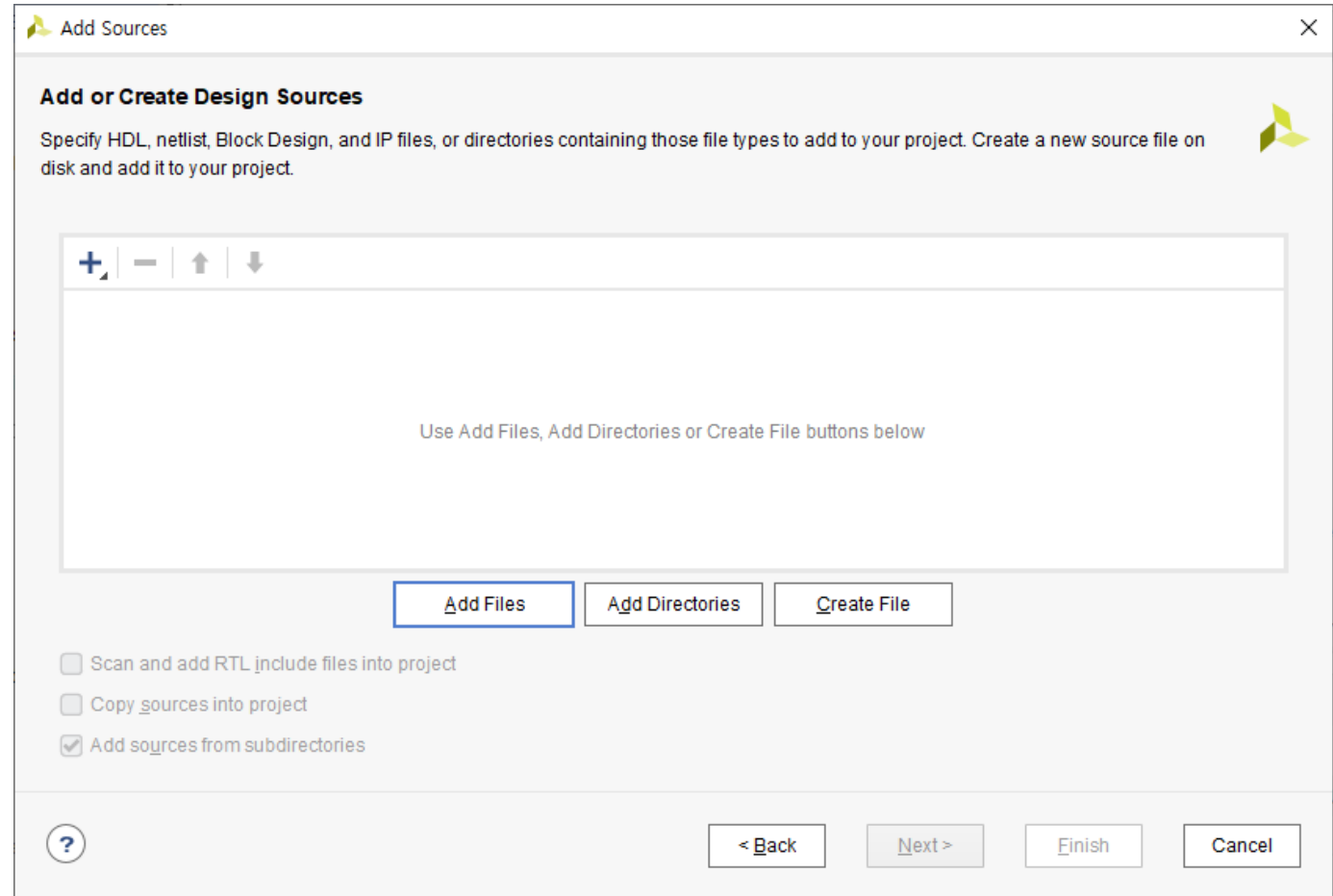
# Creating an example project

- Select Add or create design sources



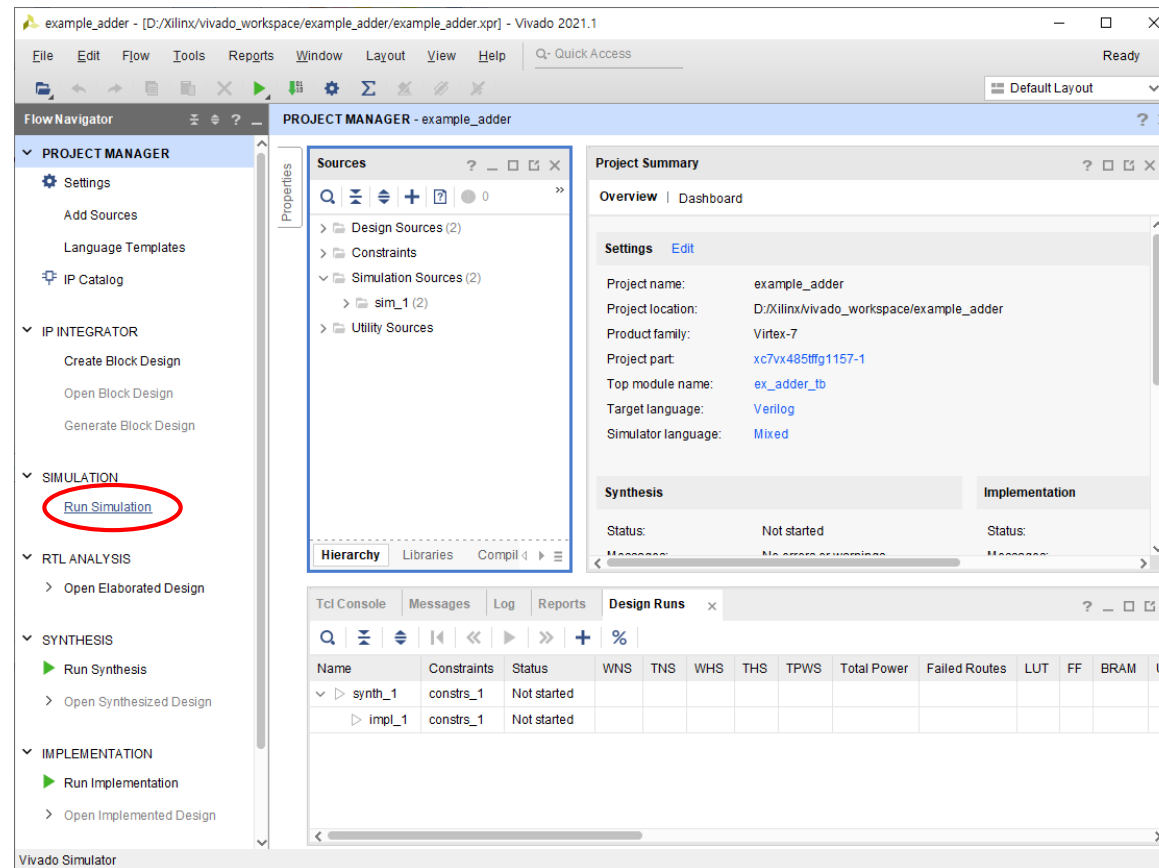
# Creating an example project

- Select Add Files
- Add the given files
  - ex\_adder.v
  - ex\_adder\_tb.v
- The example code is a simple 4-bit adder



# Creating an example project

- After adding the source files
- Click run simulation -> run behavioral simulation



# Creating an example project

- Check the simulation result

