

딥러닝 기초와 FPGA 구현

-- Deep learning from basic and implementation on FPGA --

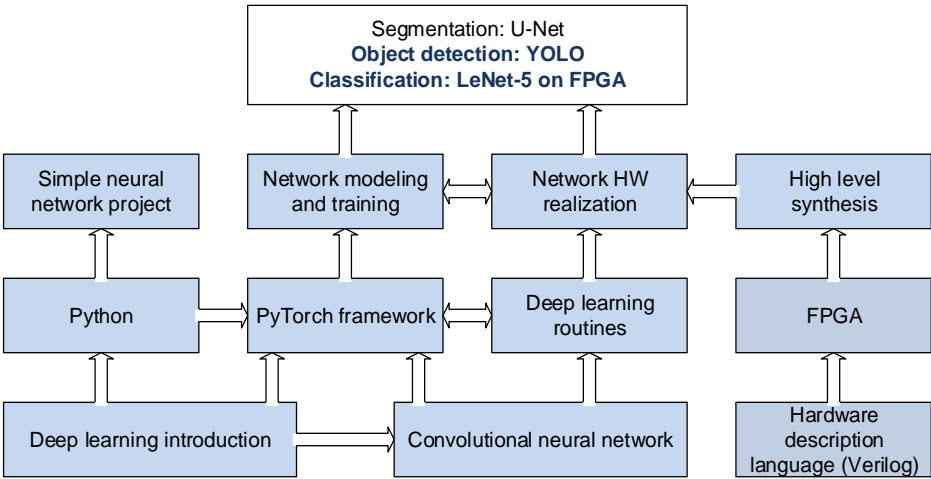
기안도

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2022년6월30일 ~ 7월1일

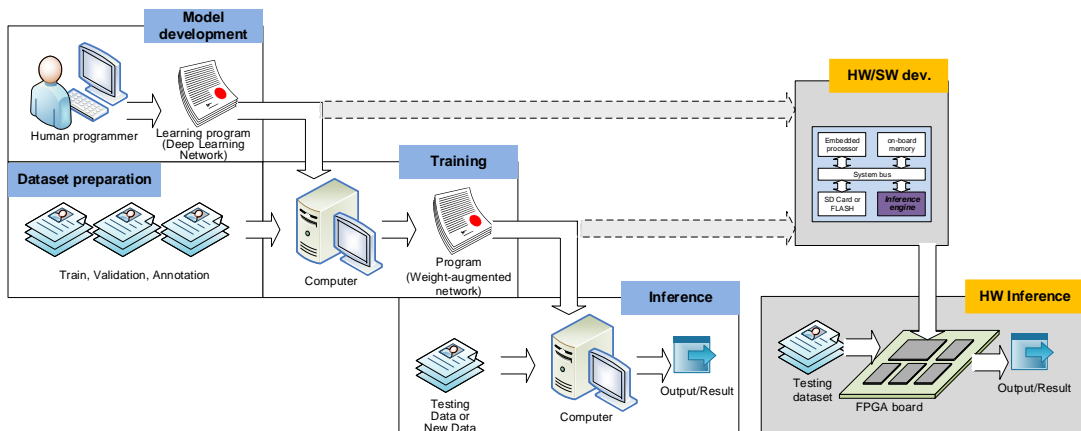
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Design flow for deep learning network



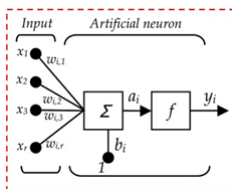
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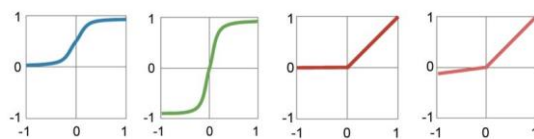
What have been covered

Neuron

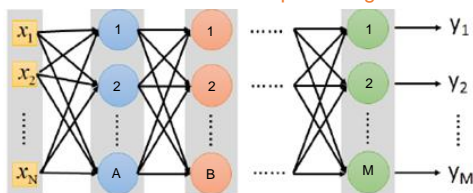


Deep-learning related topics

Activation functions



Artificial neural network: deep-learning net

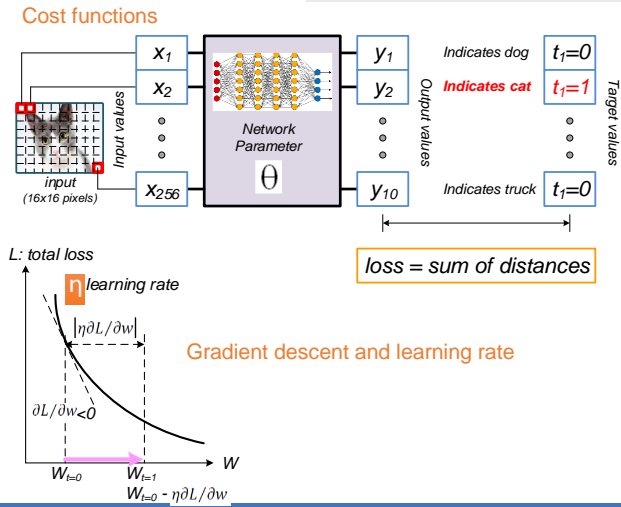


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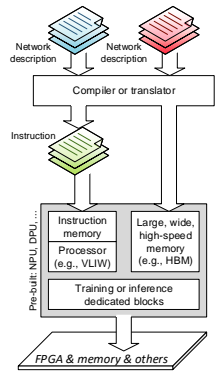
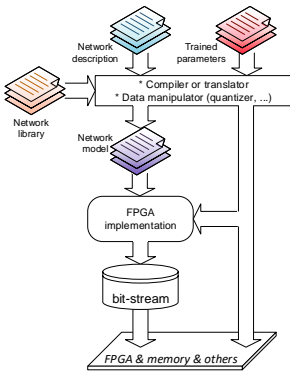
What have been covered

Deep-learning related topics

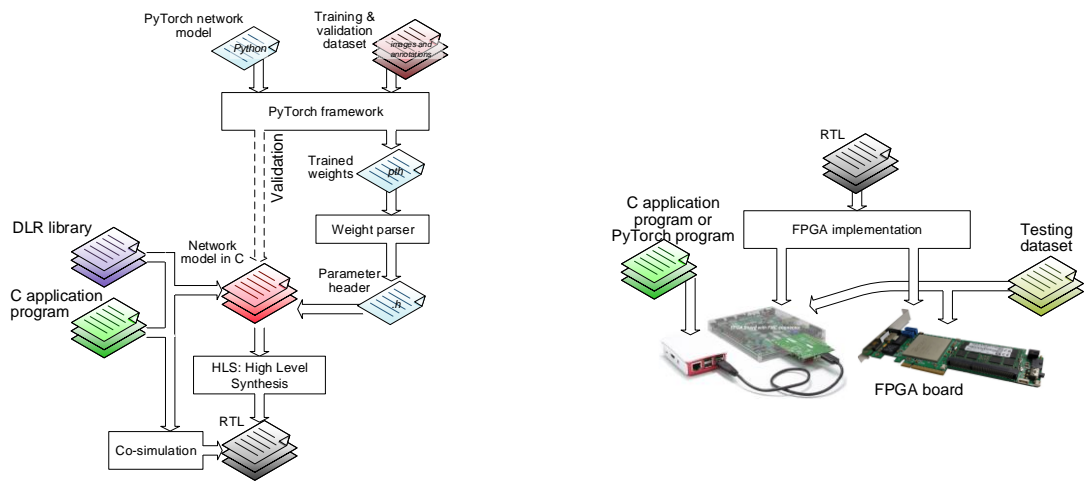


Two approaches for HW-assisted

- **Application specific**
 - ▶ RTL generating
 - ▶ Utilize neural network IP
- **Generic**
 - ▶ Fixed structure that contains programmable or configurable neural network IP



Design flow for a specific network for HW



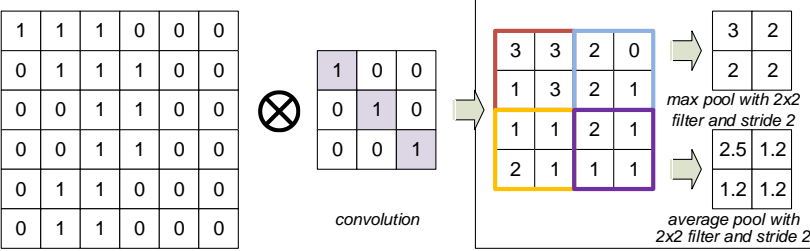
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What have been covered

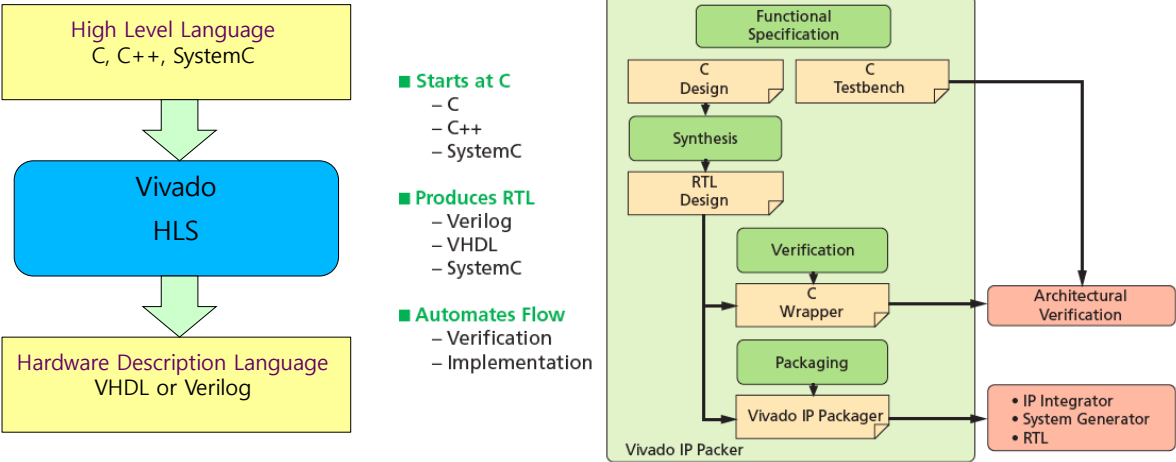
■ Convolution, Pooling



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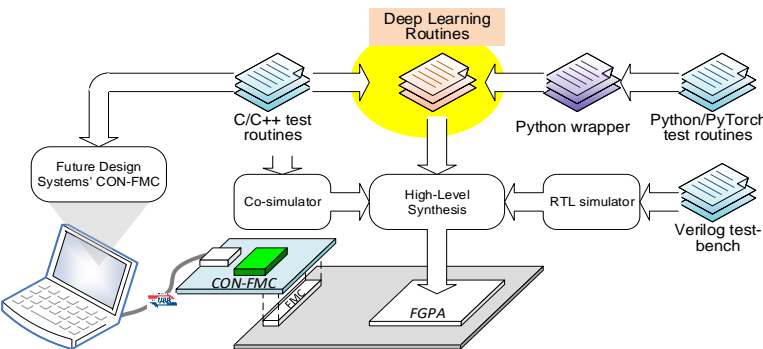
High level synthesis



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DLR: Deep Learning Routine

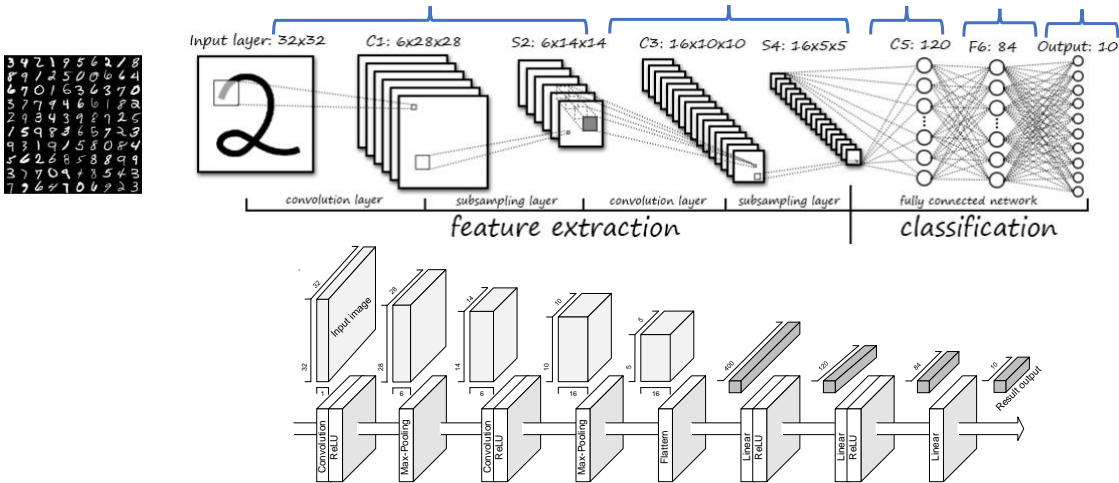
- high-level synthesizable C/C++ routines for deep learning inference network.
 - ▶ https://github.com/github-fds/Deep_Learning_Routines



Activation
▶ Click to expand this section
Concatenation
▶ Click to expand this section
Convolution
▶ Click to expand this section
Deconvolution
▶ Click to expand this section
Linear (Fully connected)
▶ Click to expand this section
Normalization
▶ Click to expand this section
Pooling
▶ Click to expand this section

LeNet-5 for MNIST

■ LeNet is one of the popular convolutional networks, and works well on digit classification tasks.

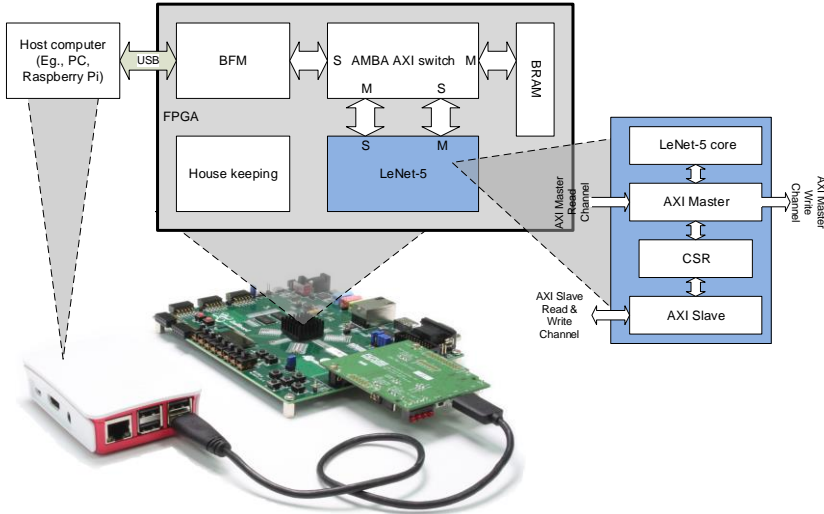


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LeNet-5 example

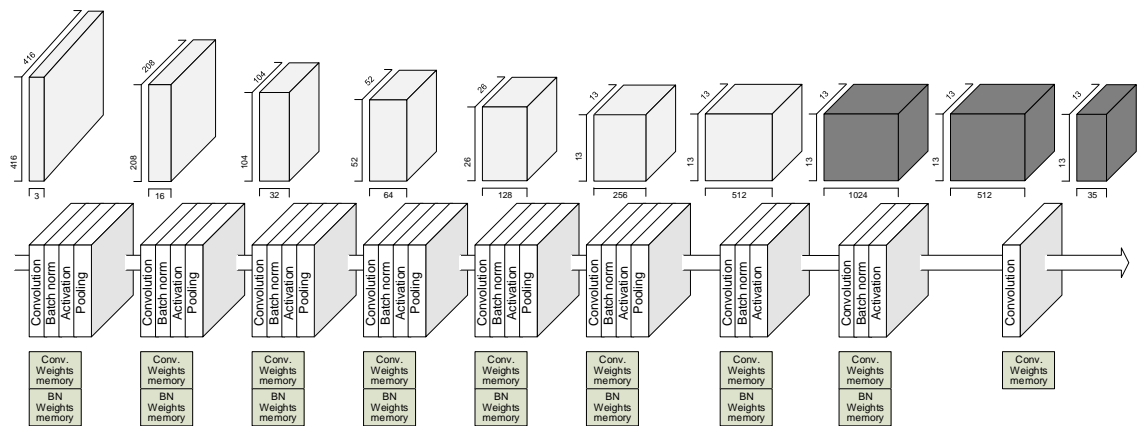


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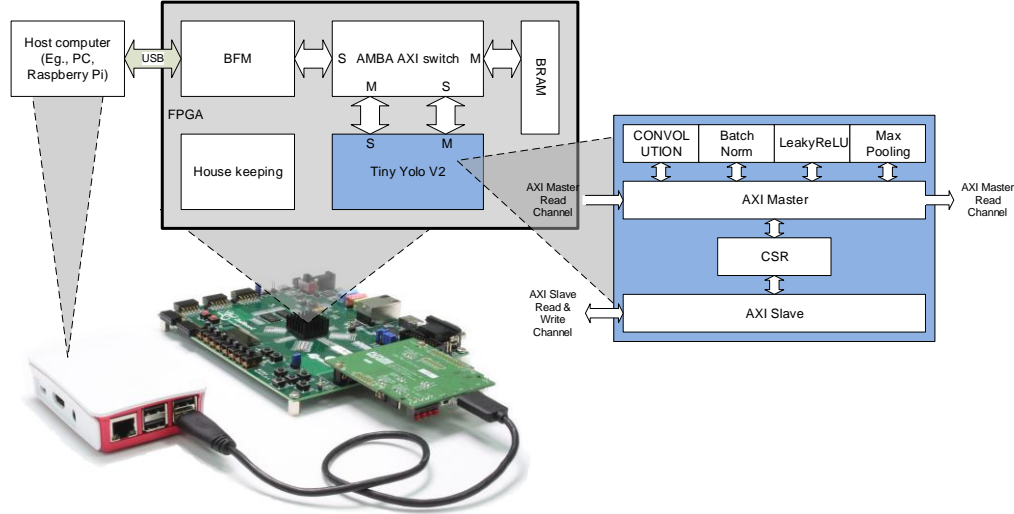
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Tiny Yolo V2



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Tiny Yolo V2 example



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